Fabrication and Characterization of Gallium Nitride based High Electron Mobility Transistors for mm-Wave Applications

Herstellung und Charakterisierung von Gallium Nitrid basierten High Electron Mobility Transistoren für mm-Wellen Anwendungen

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SUMMARY

In recent years High Electron Mobility Transistors (HEMTs) based on the nitride material system have successfully proven their potential as efficient high-power and high-frequency devices. While nitride-based HEMTs have been used commercially in the mobile communication technology for a few years, their optimization for millimeter-wave applications is still object of present research. Especially the application of nitrides as base material system for terahertz-frequency-multiplier-chains is a very promising but until now barely investigated research topic. The objective of this work is to optimize the standard process technology for the fabrication of nitride-based HEMTs of the Peter Grünberg Institute 9 (PGI-9) at the Research Center Jülich to allow for their application in the millimeter-wave regime. In order to identify performance limiting factors the influence of sub-100-nm gate lengths and the gate cross sectional structure were experimentally investigated. Furthermore T-gate processes were developed. In this context the influence of reactive ion etching with fluorine gases on the electrical properties of the used nitride material system was studied. Additionally a chlorine based dry-etch process was developed for gate-recessing purpose. Advantages and disadvantages of this chlorine-based dry etch process were compared with the advantages and disadvantages of a second gate-recess approach, which is based on sputter etching. Fully passivated HEMTs of this work achieved an extrinsic current-gain cut-off frequency of up to 60 GHz and a maximum frequency of oscillation of 125 GHz. By means of the developed chlorine-based dry etch process HEMTs were built, which achieved an extrinsic transconductance of greater than 400 mS/mm, an extrinsic maximum frequency of oscillation of 105 GHz and an extrinsic current-gain cut-off frequency of 35 GHz while having a gate length of 370 nm. As an example of a millimeter-wave application monolithically integrated oscillator structures with a nitride-HEMT as an active device were designed and fabricated. The oscillators achieved a frequency of oscillation of 39.9 GHz and an output power of 10 dBm at 13.3 GHz.

KURZFASSUNG

In den vergangenen Jahren haben High-Electron-Mobility-Transistoren (HEMTs) basierend auf dem Materialsystem der Nitride ihr Potential als effiziente Hochleistungs-Hochfrequenzbauelemente erfolgreich unter Beweis gestellt. Während auf Nitriden basierende HEMTs seit wenigen Jahren kommerziell in der Mobilfunk-Kommunikationstechnik eingesetzt werden, ist ihre Optimierung für Millimeterwellen-Anwendung noch Gegenstand aktueller Forschung. Insbesondere ist die Anwendung der Nitride als Basismaterialsystem für Terahertz-Frequenz-Vervielfacher-Ketten ein vielversprechendes, aber bisher wenig untersuchtes Forschungsthema. Diese Arbeit hat zum Ziel, die Standard-Prozess-Technologie des Peter Grünberg Instituts 9 (PGI-9) am Forschungszentrum Jülich zur Herstellung von auf Nitriden basierenden HEMTs zu optimieren, um ihren Einsatz im Millimeter-Wellenbereich zu ermöglichen. Um leistungslimitierende Faktoren zu identifizieren, wurde unter anderem der Einfluss von Gate-Längen unter 100 nm sowie die Gate-Querschnitts-Struktur untersucht. Weiterhin wurden T-Gate-Prozesse entwickelt. In diesem Zusammenhang wurde der Einfluss von Reaktivem-Ionen-Ätzen mit Fluorgasen auf die elektrischen Eigenschaften des verwendeten Nitride-Materialsystems untersucht. Des Weiteren wurde ein chlorgas-basierter Trockenätzprozess zum Zwecke eines Gate-Recess entwickelt. Vor- und Nachteile dieses chlorgas-basierten Trockenätzprozesses wurden mit den Vor- und Nachteilen eines zweiten Gate-Recess-Ansatzes verglichen, welcher auf Sputter-Ätzen basiert. Vollständig passivierte HEMTs dieser Arbeit erreichten eine extrinsische Kurzschlussstromverstärkung bis zu einer Frequenz von 60 GHz und eine extrinsische maximale Schwingfrequenz von 125 GHz. Mit Hilfe des entwickelten chlorgas-basierten Trockenätzprozesses wurden HEMTs gefertigt, welche eine extrinsische Steilheit von über 400 mS/mm, eine extrinsische maximale Schwingfrequenz von 105 GHz und eine extrinsische Kurzschlussstromverstärkung bis 35 GHz bei einer Gate-Länge von 370 nm erreichten. Als Beispiel für eine Millimeterwellenanwendung wurden monolithisch-integrierte Oszillatorstrukturen mit einem Nitride-HEMT als aktives Element entworfen und gebaut. Die Oszillatoren erreichten eine Schwingfrequenz von 39.9 GHz und eine Ausgangsleistung von 10 dBm bei 13.3 GHz.

CONTENTS

CHAPTER 1

Introduction

In the first section 1.1 of this introduction the unique properties of the nitride material in comparison to traditional semiconductors such as silicon are discussed. In this way the questions should be answered, why the nitride material system has been in the focus of intense research for more than a decade and still is today. In the subsequent section 1.2 a brief introduction to the challenging field of generating electro-magnetic radiation in the THz-spectrum is given and the potential of the nitride material system as basis for small, robust, light and cheap THz-radiation-sources working at room temperature is outlined. In the end of this introduction the research objectives and the organization of the thesis are outlined.

1.1 Why nitrides?

The basic binary compound semiconductors of the nitride material system, also referred to as nitrides, are: gallium nitride (GaN), aluminum nitride (AlN), indium nitride (InN) and boron nitride (BN), while the latter one is still immature as a semiconductor material [1]. The nitride material system covers a broad range of band gap energies, corresponding to an optical spectrum reaching from infrared (0.8 eV for InN) to ultra violet (6.2 eV for AlN). The benefits for optoelectronic applications is obvious because the nitrides cover the whole optical spectrum and they are direct band gap materials in their basic configurations [1]. The blue Light Emitting Diode (LED), arguably the greatest optoelectronic advance of the past 25 years [2], nowadays entirely relies on the nitride material system in the commercial sector, what explains the dominance of the nitrides on today's optoelectronic market. State-of-the-art white LEDs, which base on blue LEDs plus phosphor, achieve an efficiency of around 250 lm/W and hence they outperform the classical light bulb (≈ 16 lm/W) and fluorescent tubes (≈ 100 lm/W) by far, additionally benefiting from an increased longevity in comparison to compact fluorescent lights [2, 3].

But also for electronic applications the wide tuning range of the band gap energies of the nitrides, achieved by changing the material compositions, is beneficial as it allows for high bulk breakdown voltages on the one hand and for low effective mass and high mobility on the other hand [1]. Especially the feature of a wide band-gap semiconductor has set the nitride electronics in the focus of an intense research for more than a decade. Table 1.1 compares inherent material properties of bulk GaN to silicon (Si), gallium arsenide (GaAs), silicon carbide (SiC) and diamond [4].

Bulk GaN exhibits about the same electron mobility μ_n and thermal conductivity Θ as silicon. But the saturation velocity v_{sat} is 2.5 times higher than in silicon and the critical electric field E_{cr}, beyond which breakdown occurs, is more than ten times higher in the case of GaN than for silicon. The high E_{cr} enables high voltage operation [5] making the GaN-based Field Effect Transistor (FET) a promising candidate for the next generation of power electronic switches [6].

	Si	GaAs	SiC	GaN	diamond
band gap E_g (eV)	1.1	1.4	3.3	3.4	5.5
permittivity ϵ_r	11.8	13.1	10	9.0	5.5
electron mobility μ_n ($cm^2\ V^{-1}\ s^{-1}$)	1350	8500	700	1200	1900
saturation velocity v_{sat} (10^7 cm/s)	1.0	1.0	2.0	2.5	2.7
critical electric field E_{cr} (MV/cm)	0.3	0.4	3.0	3.3	5.6
thermal conductivity Θ ($W\ K^{-1}\ m^{-1}$)	150	43	330	130	2000
$JFoM/JFoM_{Si}$	1.0	1.3	20.0	27.5	50.4
$BFoM/BFoM_{Si}$	1.0	14.4	11.9	20.0	82.0

Table 1.1: Material properties of Si, GaAs, SiC, GaN and diamond and their Johnson's Figure of Merit (JFoM) and Baliga's Figure of Merit (BFoM), both normalized to the corresponding values for silicon, in analogy to references [4, 5].

To reveal the potential, a specific semiconductor material system has for electronic device applications in principle, it is instructive to evaluate certain figures of merit. A useful figure of merit bases solely on inherent material parameters, but stresses those parameters which are expected to be the limit of the ultimate device performance within this material system. A famous figure of merit is Johnson's Figure of Merit (JFoM) which is defined as $(v_{sat} \cdot E_{cr})/(2\pi)$ and describes the ultimate limit regarding the power-gain and the high-frequency performance a transistor can achieve in a certain semiconductor material [7]. Values of the JFoM normalized to the one of silicon $JFoM_{Si}$ are also listed in table 1.1. Additionally Baliga's Figure of Merit (BFoM) was evaluated for each material system and the normalized values with respect to silicon are listed in the bottom row of table 1.1. The BFoM is defined as $\epsilon_r \cdot \mu_n \cdot {E_g}^3$ and is useful to identify suitable materials for power switching applications [8]. Both figures of merit, the JFoM and the BFoM, identify GaN as excellent material for high-power and high-frequency applications, clearly superior over the traditional semiconductors Si and GaAs.

Indeed, in the last years the GaN material system in combination with the High Electron Mobility Transistor (HEMT) as the device type of choice has shown record output power densities of more than 10 W/mm at 40 GHz [9] which is almost one order of magnitude higher than in any other semiconductor technology at these frequencies [10]. Additionally amplifiers based on GaN HEMTs generally feature a high Power Added Efficiency (PAE) due to high operating voltages, what allows to reduce the cooling and heat sinking efforts for Radio Frequency (RF)-amplifiers and hence allows to reduce weight and related costs [5]. Consequently, nitride electronics are employed for mobile base stations of the third and fourth generation, like for instance the Worldwide Interoperability for Microwave Access (WiMAX) base station based on GaN HEMT technology, presented by Fujitsu electronics in 2008 [11, 12].

Because of their high-power and high-frequency capabilities RF-circuits based on nitride transistors are interesting and attractive candidates for replacing classical RF-power-amplifiers and sources based on Traveling-Wave Tube (TWT) concepts also referred to as tubes as a short term denotation. The reason for this replacement is that RF-circuits based on solid-state devices feature low production cost, small size and weight and high reliability in comparison to the traditional tube-sources [13].

Due to some excellent Direct Current (DC)-characteristics, like current densities in excess of 2 A/mm, a sub-threshold slope of 68 mV/decade and an I_{on}/I_{off} ratio of $> 10^7$, which were achieved by nitride HEMTs during the last years, nitride-based electronics may also

be considered to augment today's highly integrated, Si-based digital electronic [14]. But so far the outstanding domains of the nitrides are the field of optoelectronics and the field of high-power and high-frequency electronics. Especially the strong economic perspective for the nitride optoelectronic market [2] is seen as a leverage for the remainder nitride electronic industry and research [5].

One of the best ways to conclude this first introducing section was found in the outlook given by R. Quay in 2008 [1]: "... III-N opto-electronics will challenge the light bulbs, while III-N electronics will challenge the electronic equivalent, the tubes.".

1.2 Nitride electronics and THz-generation

Electromagnetic waves with a frequency in the range of 300 GHz to 3 THz, also referred to as THz-radiation [15], exhibit some interesting properties: They readily pervade plastic, paper and textiles, but are strongly absorbed by water and reflected by metal. The wavelength of THz-radiation is in the range of micrometer to millimeter. The photon energy associated with THz-radiation achieves a few meV at a maximum, hence electromagnetic waves in the frequency range of 300 GHz to 3 THz are regarded as non-ionizing. Due to these properties THz-radiation is considered for many different fields of applications, such as: communication, radio astronomy, biology and medical science, molecule spectroscopy, material analysis and industrial applications as well as security technology [16, 17]. To enter the above mentioned fields of applications on a broad commercial basis, compact, robust and cheap sensors and sources are required [16, 17], while the most pressing component technology development is still seen in the area of sources [15].

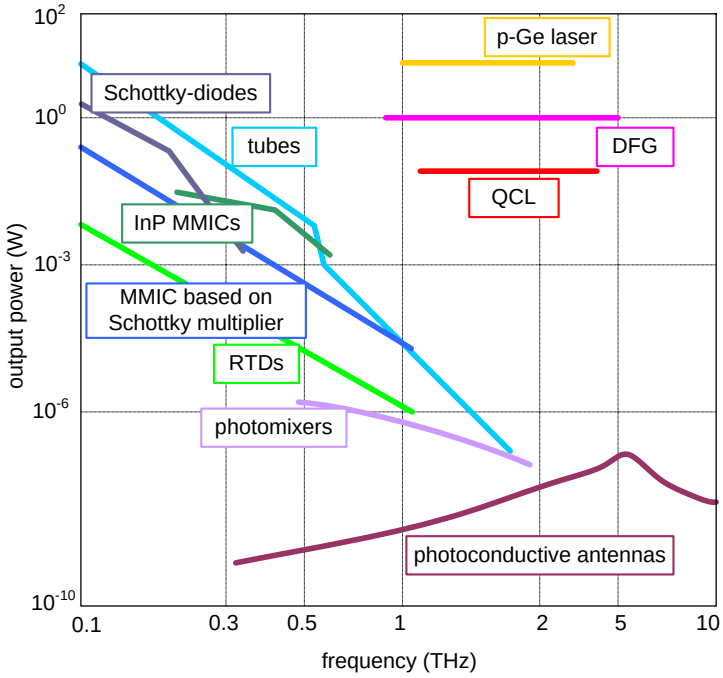

Figure 1.1: Overview of various THz-sources and the related output powers as a function of frequency in analogy to references [16, 18].

Figure 1.1 shows a combined and reduced overview of various THz-sources and the related output powers as a function of frequency in analogy to references [16, 18]. Although figure 1.1 shows the output powers for various source types, a complete overview is not given at this stage. But figure 1.1 provides enough information to show the general situation and the variety of approaches to create electro-magnetic radiation around a frequency of 1 THz. Also the output power-frequency dependencies of the various source types may have been to be modified in the light of an up-to-date literature research. Nevertheless, the big picture drawn in figure 1.1 is not expected to be much different, if it was drawn on the basis of a more detailed and larger data set.

According to figure 1.1 the frequency regime below 1 THz is governed by sources based on tubes and on electronic RF-circuits like indium phosphide (InP) Monolithic Microwave Integrated Circuit (MMIC)s or other RF-circuits employing a Schottky-diode [19] or a Resonant Tunneling Diode (RTD) as active device. The frequency regime above 1 THz is dominated by sources which base on optical technology like p-Ge laser, Quantum Cascade Laser (QCL) or Difference Frequency Generation (DFG). Only the approaches of photo-mixing and photoconductive antennas cover a broad spectrum around 1 THz and thus they successfully bridge the THz-technology gap.

Photo-mixing and photoconductive antennas are today's most commercially successful techniques and base on down-conversion from the optical regime or on femto-second pulse-techniques, respectively [15]. Their disadvantages are relative low output powers of less than 10^{-5}W and their need for power-hungry lasers which counteracts the objective of compact, light and cheap THz-source.

High output powers of hundreds of mW in the upper THz-regime can be achieved by using QCL and p-Ge lasers. A disadvantage of these types of THz-sources is that they require cryogenic temperatures, if emission in the THz-band is focused. In the case of p-Ge lasers high magnetic fields of about 1 T have to be applied in addition [20, 21]. For wavelengths of 5 μm and 8.5 μm high optical output powers at and above room temperature were achieved [22]. Also advances toward a silicon-based THz-laser were made during the last years [23, 24]. But for the THz-band one of the highest operating temperatures of a QCL is 164 K [25]. The lowest frequency of operation achieved so far is about 1.39 THz [18].

The approach of DFG is a very interesting approach when high-power optical sources working at room temperature are focused. DFG bases on mixing two coherent infrared laser beams in nonlinear optical crystals such as GaSe, $ZnGeP_2$ and GaP [26]. Additionally a design of shoe-box size seems to be feasible [26] making this approach the most promising one of all optical sources if a high-power, compact and light THz-source working at room temperature is desired.

Tubes like the klystron, the carcinotron, which is also denoted as Backward-Wave Oscillator (BWO), the magnetron and the gyrotron offer the highest power and tuning range at sub-millimeter wave length [15] so far. Output powers may be as high as 200 kW continuous-wave at 106 GHz or 120 kW pulsed at 375 GHz [27] showing that the curve, which is associated to tubes in figure 1.1, underestimates their power-frequency dependence. At 1 THz carcinotrons can deliver more than 1 mW of output power [15]. The disadvantage of tubes is their need for high operating voltages of typical several kV and high magnetic fields of about 1 T [15, 20], both making these sources bulky and costly.

THz-sources based on solid-state devices seem to be the most promising approach if a compact and light design working at room-temperature is desired. The basic operation principle is successive up-conversion of an RF-signal by frequency multipliers in a so-called

THz-multiplier-chain. As active components two-terminal devices like Schottky-diodes and RTDs and/or three-terminal devices like the HEMT or the Heterojunction Bipolar Transistor (HBT) may be considered. Signal generation up to a frequency of 2.7 THz was achieved by the approach of a THz-multiplier-chain [15]. But THz-multiplier-chains generally suffer from a strong power-frequency roll-off as depicted in figure 1.1, which is caused by resistive and reactive losses [15]. Consequently only low output powers are achieved by up-conversion at the upper THz-spectrum, e.g. 21 μW peak power at 1.64 THz at room temperature [28]. In a sum the available power of THz-radiation which can be achieved by a THz-multiplier-chain, is limited by three factors:

1. The maximum power which can be delivered by the first stage, i.e. the drive stage of the chain.
2. The power handling capabilities of the subsequent multiplier-stages.
3. The overall efficiency of up-conversion.

Especially the power handling capabilities of the first few stages of a THz-multiplier-chain are seen as a constraint [15], which can be beefed by adding multiple devices in series [29]. A sufficiently high power at the drive stage of 100 mW at 100 GHz can be achieved by using GaAs-based HEMT power amplifier technology [30]. The initial power of about 100 mW at 100 GHz may be increased by employing an InP HEMT technology leaving the task for the builders of subsequent multiplier stages to harness this power and design chips which can handle it without burn-out [30].

Consequently active devices based on the nitride material system are considered as attractive candidates for building a THz-multiplier-chain, because they are generally regarded as efficient high-power and high-frequency devices as discussed in section 1.1 of this introduction. Or to put it in other words: To overcome the fundamental challenge of the power handling capability of the first stages of a THz-multiplier-chain, the semiconductor material of choice should exhibit the highest JFoM, i.e. the highest power-frequency limit based solely on material properties. Accordant to table 1.1, this is diamond. From a practical perspective the material of choice is GaN.

Also if a more concrete example is considered, the choice of GaN as a basis for THz-multiplier-chain is promising: The first stage of THz-multiplier-chain, presently employed as local-oscillator in the Herschel Space Observatory [31], is fed with an input signal with an RF-power of approximately 100 mW at $94-106$ GHz. The whole chain delivers 100 μW at 1.2 THz at room temperature [32] meanwhile fulfilling the strict requirements regarding reliability, size and weight for space equipment. Considering that today's amplifiers based on GaN are able to deliver output powers of 842 mW at 88 GHz with a PAE of 14.7% [33], the potential of a GaN-based RF-source as a first stage of a THz-multiplier-chain becomes obvious.

1.3 Research objectives

As discussed in the introducing sections 1.1 and 1.2 of this work nitride-based electronics have a large potential to improve the output power and efficiency of THz-multiplier-chains. The potential is seen as initial motivation for this work which involves two major tasks:

1. Starting from the standard GaN-HEMT technology of the Peter Grünberg Institute 9 (PGI-9) at the Research Center Jülich, this technology should be optimized in order

to obtain HEMTs whose RF-performance allows using them for mm-wave applications, i.e. applications targeting a frequency regime above 30 GHz. The focus is set on the development of a T-gate process and the development of an appropriate recess procedure.

2. A monolithically integrated GaN-HEMT-oscillator should be designed and build as a first investigation with respect to its potential application as driving stage of a THz-multiplier-chain.

1.4 Organization of the thesis

This thesis is organized as follows:

In chapters 2,3 and 4 some fundamentals of the nitride material system, the HEMT and the definition of high-frequency figures of merit are outlined, respectively. The objective of these chapters is to provide a theoretical basis for the subsequent interpretation and discussion of the results obtained during this work.

Chapter 5 starts with a detailed literature research and discusses strategies for the improvement of the RF-performance of GaN-HEMTs.

Chapters 6 and 7 are dedicated to the technology and experimental results of the T-gate processes and the recessing procedures of this work, respectively.

In chapter 8 the design and the experimental results of GaN-HEMT-oscillators of this work are outlined.

Chapter 9 concludes this work by summarizing the major results.

Appendix contains in-detail information which is not given in the main chapters of this work for the sake of clarity.

CHAPTER 2

Nitride Particularities

The objective of this chapter is to provide a brief overview of some particularities of the III-N material system in comparison to other semiconductor materials. One major difference in comparison to the AlGaAs/GaAs material system is the effect of polarization doping which allows the formation of a Two-Dimensional Electron Gas (2DEG) at AlGaN/GaN heterojunctions without the need for intentional barrier doping. Another particularity to be mentioned is the pronounced sensitivity of the 2DEG of AlGaN/GaN heterostructures to surface trapping effects which leads to the virtual gate effect. Although the information provided in this chapter generally applies to nitrides in many aspects, the focus is set on the AlGaN/GaN heterojunction.

2.1 Polarization doping

At room temperature GaN, AlN, and InN crystals are found in the wurtzite structure. In thin films GaN and InN can also be found in the zincblende structure as depicted in figure 2.1 while for AlN no stable zincblende phase has been achieved so far [1]. However, for today's electronic applications the crystal structure of choice is the wurtzite crystal structure throughout. The hexagonal geometry of the wurtzite structure lacks a centric symmetry (cf. figure 2.2), what is a prerequisite for piezoelectric effects to occur in a crystal. The non-centrosymmetric wurtzite structure in combination with a pronounced ionic character of the crystal binding lead to strong polarization effects in the III-nitride semiconductors. These strong polarization effects are an important particularity of the III-nitride material system, because the absolute values of the piezoelectric constants of the nitride semiconductors are ten times higher than in conventional III-V semiconductor and II-VI compounds [1, 34].

Because polarization effects strongly influence the interfaces of the III-nitride semiconductors, the control of the polarization mechanism is as important as the control of doping profiles in the silicon Complementary Metal Oxide Semiconductor (CMOS) technology [1]. This is also true in the sense that by means of polarization engineering an electron channel can be formed at the AlGaN/GaN heterojunction without any intentional doping of the nitride semiconductor. Changing the amount of free channel electrons by controlling the polarization fields in the adjacent semiconductor layers is referred to as polarization doping.

The typical growth direction for nitrides is along the c-axis of the wurtzite structure as depicted in figure 2.2. GaN layers can either be grown Ga-face or N-face [35]. For Ga-face-grown material the (0001) crystal axis is perpendicular to the semiconductor surface and points from substrate to the surface. For N-face-grown material the (0001) crystal axis of the wurtzite structure is also perpendicular to the surface but it is orientated from surface to substrate. Whether Ga-face or N-face growth occurs strongly depends on the applied growth technique, presents of a nucleation layer and/or the specific growth parameter [35, 36].

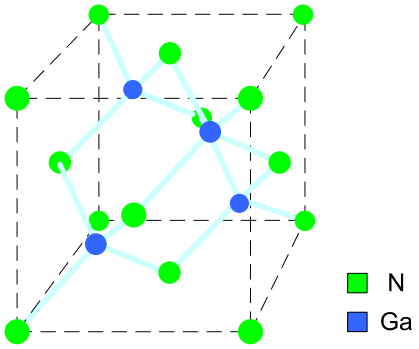

Figure 2.1: Zinkblende crystal structure.

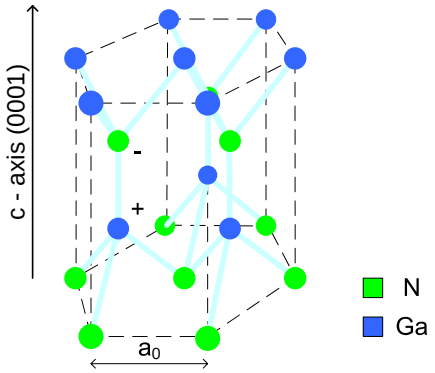

Figure 2.2: Wurtzite crystal structure.

Two polarization effects have to be considered in the nitride material system: spontaneous and piezoelectric polarization. Both polarization effects are comparable to each other regarding their strength and neglecting either of the two components leads to inaccuracies when determining the electrical properties of the nitride semiconductor [37].

2.1.1 Spontaneous Polarization

The spontaneous polarization $\boldsymbol{P}_{sp}$ occurs along the c-axis of the wurtzite structure as shown in figure 2.2 and originates from the non-centro-symmetric structure of the wurtzite crystal. If the direction of polarization vector $\boldsymbol{P}$ is defined to be the (0001) direction, the values of P_{sp} for all three binary compounds are negative (cf. table A.1 in the appendix). Hence for a Ga-face layer structure the polarization vector points from surface toward the substrate.

The value of the spontaneous polarization P_{sp} depends on the composition of the nitride semiconductor. For example, the value of the piezoelectric polarization of the ternary $Al_xGa_{1-x}N$ compound can be approximated by (2.1) [1].

$$P_{sp,Al_xGa_{1-x}N} = (-0.052 \cdot x - 0.029)\, C/m^2 \tag{2.1}$$

So for all compositions the polarization points in the $(000\bar{1})$ direction while the highest spontaneous polarization is achieved for pure AlN with a value of $-0.081\, C/m^2$.

2.1.2 Piezoelectric Polarization

In addition to the spontaneous polarization the piezoelectric polarization has to be considered if the semiconductor layer of interest is subjected to strain. The origin of the piezoelectric polarization is a displacement of the Ga-sub-lattice to the N-sub-lattice caused by mechanical stretching and bending. The relation between mechanical deformation and electrical polarization is established by the piezoelectric constants. Values of the piezoelectric constants e_{13} and e_{33}, which are of relevance in this section, are listed in appendix A.2 for the binary III-N compounds. The value of piezoelectric polarization P_{pz} along the c-axis is given by (2.2) [35].

$$P_{pz} = 2 \cdot \frac{a - a_0}{a_0} \left(e_{31} - e_{33} \cdot \frac{C_{13}}{C_{33}} \right) \tag{2.2}$$

C_{13} and C_{33} denote the elastic constants. The parameter a denotes the length along the hexagonal edge while a_0 represents the length of this edge in the unstrained crystal as depicted in figure 2.2. Values for C_{13}, C_{33} and a_0 of the binary compounds are also listed in appendix A.2.

The corresponding values for the ternary compound nitrides are typically found by linear interpolation of the values of the binary compounds [35, 1]. For $Al_xGa_{1-x}N$ the term $(e_{31} - e_{33} \cdot C_{13}/C_{33})$ is always negative over the whole range of compositions. Thus, according to (2.2) the piezoelectric polarization is negative for tensile ($a > a_0$) and positive for compressive strained $Al_xGa_{1-x}N$ barriers [35]. Therefore spontaneous and piezoelectric polarization of $Al_xGa_{1-x}N$ point in the $(000\bar{1})$ direction, if the layer is subjected to tensile strain, and hence both add up to the total polarization in a constructive way. If the $Al_xGa_{1-x}N$ layer is subjected to compressive strain, $\boldsymbol{P}_{pz}$ will counteract $\boldsymbol{P}_{sp}$.

2.2 AlGaN/GaN heterojunction and channel formation

Two conditions have to be fulfilled to form an electron channel at a nitride heterojunction [1]:

1. A fixed positive interface charge must be present at the interface based on the overall polarization.
2. The band gap of the semiconductor, to where the electrons are driven, must be smaller than the band gap of the other layer.

In this work only the single AlGaN/GaN heterojunction is of interest. Its situation is depicted in figure 2.3. Because the growth of an AlGaN barrier layer on a relaxed GaN buffer layer causes tensile strain in the AlGaN layer there is also a piezoelectric component to the total polarization of the barrier layer. The net interface charge at the AlGaN/GaN heterojunction σ_{int} is the difference of the two adjacent polarizations and hence given by (2.3). Because $P_{sp,GaN} - (P_{sp,AlGaN} + P_{pz,AlGaN}) > 0$ the first condition is fulfilled.

$$\sigma_{int} = P_{sp,GaN} - (P_{sp,AlGaN} + P_{pz,AlGaN}) \tag{2.3}$$

Also the second condition is fulfilled as GaN exhibits a lower band gap than AlGaN ternary compound. At the AlGaN/GaN interface the conduction band E_c builds a notch referred to as quantum well, whose shape can be considered as triangular in a good approximation [38]. Figure 2.4 shows a sketch of the conduction band structure for a Ga-face grown AlGaN/GaN heterojunction [39]. As depicted in figure 2.4 the notch of the conduction band reaches below the Fermi-potential E_f. Thus the electrons which are attracted by the positive, but fixed, interface charge σ_{int} will settle in the quantum well and form a 2DEG. Because the 2DEG formation occurs without applying an external voltage, the resulting transistor structure is a normally-on device, also referred to as Depletion-mode (D-mode) device (cf. chapter 3).

Because the material used for many experiments of this work features an AlN spacer layer between the AlGaN barrier and the GaN buffer layer, the resulting conduction band

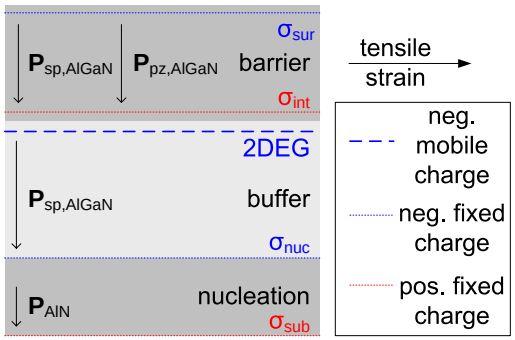

Figure 2.3: Spontaneous polarization, piezoelectric polarization, fixed interface charges and 2DEG of a AlGaN/GaN heterostructure, grown Ga-face, according to references [36, 35].

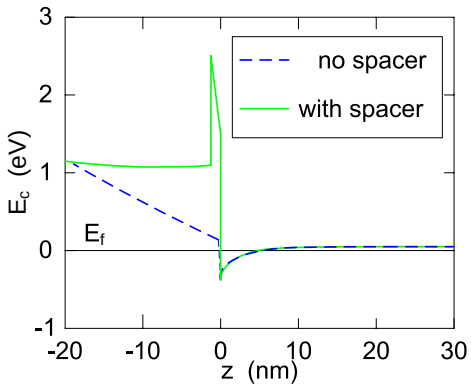

Figure 2.4: Sketch of the conduction band structure of a Ga-face grown AlGaN/GaN heterojunction with and without an AlN spacer layer according to [39].

structure is also drawn in figure 2.4. Compared to the AlGaN/GaN heterostructure with the same Al mole fraction the heterostructure with the AlN spacer layer provides a better confinement of the channel electrons due to the peak in the conduction band structure as shown in figure 2.4. Because the AlN spacer suppresses the carrier penetration from the channel into the AlGaN barrier, the electron transport is less prone to alloy disorder and/or interface roughness scattering. The result is an improved mobility for structures with a spacer layer [40, 41, 42, 43]. Additionally the insertion of an AlN spacer layer may increases the sheet carrier concentration due to the strong polarization-induced charge caused by the large lattice mismatch between AlN and GaN [44]. In this way sheet carrier concentrations of up to $5 \cdot 10^{13}\,\mathrm{cm}^{-2}$ have been achieved in AlN/GaN heterojunctions [45]. By choosing the AlN spacer thickness to be 1.63 nm the potential energy in the AlGaN barrier layer is not expected to vary with distance [46] and stays constant at about 1.1 eV as sketched in fig. 2.4. So with the help of an AlN spacer the sheet carrier concentration n_s becomes less dependent on the AlGaN barrier thickness [39]. A potential drawback caused by the introduction of an AlN spacer layer may be long-term reliability problems originated from the strong built-in electrical field [39].

2.3 Trapping effects and virtual gate effect

A semiconductor typically exhibits a certain density of defects which disturb the ideal lattice structure of the crystal. Defects are caused by atomic dislocations, interstitials and incorporation of impurities while the latter one is referred to as doping if the incorporation happens on purpose. Especially the semiconductor surface has a high density of defect states due to the abrupt disruption of crystalline lattice structure. Accordingly, also heterojunctions and interfaces are potential locations of defects due to the mismatch in lattice constants of the two adjacent crystals. Defect states may be charged and discharged during generation and recombination processes in the semiconductor, leading to temporarily ionized impurities. The process of charging and discharging of defect and surface states is also referred as trapping, the associated states are referred to as trap states.

In the GaN material system the surface states and/or defects play an much more important role on device performance than in other III-V compounds like GaAs due to the high polarization-induced charges in the III-N compounds [1, 39] and the effect of polarization doping as described in section 2.1. Possible locations of defects in the GaN material system are depicted in figure 2.5 and listed below according to reference [1]:

1. Surface traps at the source and drain access region [47, 48, 49, 50, 51].
2. Barrier bulk traps [50].
3. Traps at the barrier-buffer interface [52].
4. Buffer bulk traps [48, 53].
5. Traps at the nucleation-buffer and nucleation-substrate interface.

Defects located close to the channel are expected to have a stronger impact on device performance than traps in the vicinity of the substrate and the nucleation layer [54]. Especially the surface and the buffer traps and their impact on microwave power performance were subject of intense research in the last decade [55, 56, 51]. This intense research was motivated by the observation that many AlGaN/GaN HEMTs only achieved RF output powers which were less than it was expected on basis of their DC-characteristic [39]. Surface [50] and buffer traps [56, 48] were found to cause the drain current under non-static conditions to lag behind its corresponding static values and thus leading to the observed RF-DC dispersion in microwave performance.

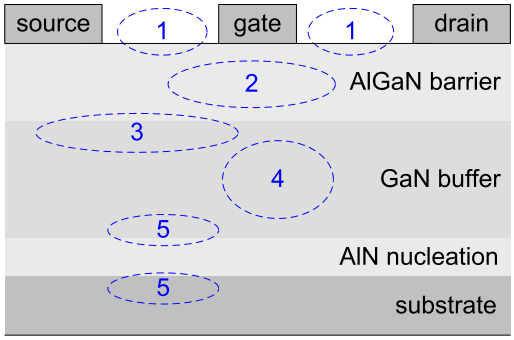

Figure 2.5: Possible location of defects and traps for AlGaN/GaN HEMTs in analogy to references [54, 1].

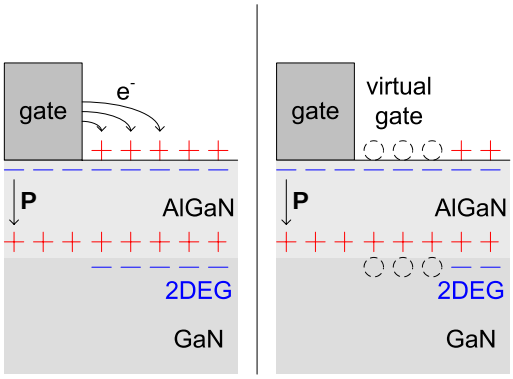

Figure 2.6: Trapping effects in the gate-drain access region leading to the virtual gate according to reference [49].

An important trapping phenomenon for AlGaN/GaN HEMTs is the so-called virtual gate effect [49]. As discussed in section 2.1 the negative channel charge of the 2DEG is caused by a net positive interface charge σ_{int} at the AlGaN/GaN junction. Consequently, a negative polarization charge σ_{sur} settles near the surface as depicted in figure 2.3. These negative polarization charges again are compensated to achieve charge neutrality by donor like surface states which are considered to be the origin of the free channel charge [57]. However, in the presence of high electric fields gate electrons reach the surface and neutralize the donor states as shown in figure 2.6. The trapping of gate electrons reduces the channel charge and eventually depletes it [47], i.e. acting as a virtual gate. In this way the gate depletion region is clearly extended beyond the actual dimensions of the gate metalization.

The virtual gate effect can have tremendous impact on device performance because it might well spread up to a micron across the semiconductor surface [58]. Beside this increase of effective gate length, a bias-dependent drain resistance can be expected under operational conditions [59], severely degrading the RF-performance [60].

2.4 Summary

In this chapter two particularities of nitride electronics, the effect of polarization doping and the virtual gate effect as a special surface trapping mechanism, are described. Both effects strongly determine the behavior and performance of nitride electronics. Especially the dispersion and trapping effects like the virtual gate effect will have a detrimental impact on the RF-performance and the microwave power performance of nitride HEMTs, if their negative impact is not reduced by appropriate surface treatments and/or material growth.

CHAPTER 3

High Electron Mobility Transistor

This chapter should provide an overview of the basic operation principles of the HEMT.

3.1 Names and history

The basic concept of the HEMT was introduced 1978 by Dingle et al. [61]. In their concept Dingle et al. describe how electrons from remote donors located in a higher band gap material are transferred to an adjacent lower gap material. Both adjacent semiconductors form a heterojunction with a triangular well at its interface, which confines the electrons in 2DEG. Because the 2DEG is separated from the ionized donors this technique significantly reduces ionized impurity scattering and thus results in a high electron mobility and saturation velocity. Because the technique of Dingle et al. is also referred to as modulation doping the HEMT is also called Modulation Doped Field Effect Transistor (MODFET). Focusing on the 2DEG the designation Two-Dimensional-Electron-Gas Field Effect Transistor (TEGFET) is also convenient. Other labellings are Separately-Doped-Field Effect Transistor (SEDFET) or Selectively Doped Heterojunction Transistor (SDHT) or just Heterojunction Field Effect Transistor (HFET). If the barrier layer, e.g. made of AlGaAs, is undoped the resulting structure is comparable to a MOS structure and the resulting FET maybe referred to as Heterostructure Insulated Gate Field Effect Transistor (HIGFET) [62]. The first working HEMT was presented by Mimura et al. in 1980 [63]. In 1994 the first AlGaN/GaN HEMT was shown by Khan et al. [64].

3.2 Charge control model

The charge control model describes the behavior of charge in the HEMT as a function of an externally applied field from the gate electrode [65]. The gate electrode in contact with the barrier layer of the material stack builds a Schottky-diode. By the means of this Schottky-barrier the 2DEG sheet charge concentration n_s can be effectively controlled by a variation of the gate potential V_G [66] what is schematically depicted in fig.3.1. If the barrier layer is doped the reverse-biased Schottky-diode forms a space charge region within the barrier layer [67]. In this way the depleted barrier is not able to conduct charge in parallel to the 2DEG channel and hence the formation of a parasitic Metal Semiconductor Field Effect Transistor (MESFET) is avoided. If proper HEMT operation is achieved, the barrier layer forms an insulator between the gate electrode and the channel. Thus the basic operation principles of a HEMT resemble those of a silicon Metal Oxide Semiconductor Field Effect Transistor (MOSFET) [65], where the barrier layer corresponds to the oxide in this analogy.

Generally the n_s-V_G dependence of a FET is non-linear [69] due to the dependence of the Fermi-potential E_f on the sheet carrier concentration n_s [66]. These nonlinearities in the n_s versus V_G dependence of a FET show up strongly in the characteristics of the

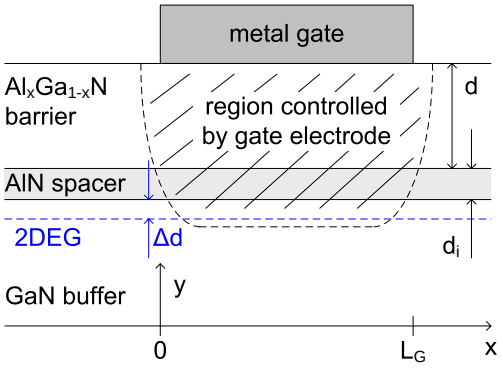

Figure 3.1: Cross-section of a HEMT gate stack with the accordant vertical dimensions.

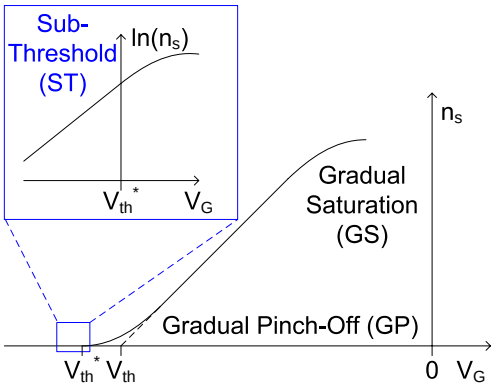

Figure 3.2: Gate controlled charges in a HEMT and related nonlinearities according to reference [68].

device, making elaborated charge control models necessary in order to simulate the FET accurately [68]. According to reference [68] three n_s-V_G nonlinearities have to be considered in the case of a HEMT, schematically illustrated in figure 3.2. These nonlinearities are referred to as Gradual Pinch-off (GP), Gradual Saturation (GS) and the Sub-Threshold behavior (ST), where the GS nonlinearity is unique to HEMTs and not present in other FETs [68].

However, commonly a simple n_s-V_G dependence as given by (3.1) is assumed [66, 65, 70, 39].

$$n_s(V_G) = \frac{\epsilon}{e \cdot (d + d_i + \Delta d)}(V_G - V_{th}) \tag{3.1}$$

$$c_0 = \frac{\epsilon}{d + d_i + \Delta d} \tag{3.2}$$

The elementary charge constant is given by e, d is the barrier layer thickness and d_i is the thickness of the spacer layer. ϵ represents the average dielectric constant of the barrier and spacer layer. Δd is the mean distance of the 2DEG from the heterojunction, also referred to as effective thickness of the 2DEG [71]. Δd has its origin from the fact that the Fermi-level is a function of the gate potential [72]. Typically Δd is about 6.8 nm to 8 nm for heterojunctions in the GaAs material system [72, 70] and 2 nm to 4 nm in the case of GaN [39]. As Δd is only a slowly varying function of n_s [66] the channel capacitance per unit area c_0, given by (3.2), depends only weakly on n_s. Hence (3.1) establishes an approximately linear relationship between n_s and V_G, which is the basis for the derivation of the basic HEMT equations.

3.3 Charge transport

In addition to the charge control model a description of the electron transport in the channel as a function of the applied electric field E is needed in order to model the behavior of the device. In general the steady-state electron transport in a FET is described by three main quantities [73, 74]: the low-field mobility μ_n, the peak velocity v_{peak} and the saturation velocity v_{sat}, which determines the electron velocity at very high electric

fields. In addition to the dependence on the applied electric field the carrier velocity is a strong function of the sheet carrier concentration n_s, the temperature T and the particular scattering mechanisms, which apply. For the nitride semiconductors GaN, AlN and InN phonon scattering is considered as the most important scattering mechanism [75] at room temperature. For low n_s impurity scattering and piezoacoustic scattering has to be considered while for high n_s interface roughness scattering is expected to cause a degradation in mobility [35].

The resulting steady-state electron velocity as function of the applied field $v(E)$ can be determined by the means of Monte Carlo simulations. On the basis of Monte Carlo simulations Farahmand et al. [76] developed a $v(E)$ model for binary and ternary wurtzite-phase nitrides given by (3.3).

$$v(E) = \frac{\mu_n \cdot E + v_{sat} \cdot \left(\frac{E}{E_c}\right)^{n_1}}{1 + a \cdot \left(\frac{E}{E_c}\right)^{n_2} + \left(\frac{E}{E_c}\right)^{n_1}} \tag{3.3}$$

μ_n denotes the low-field mobility which depends on temperature T and the doping density [76]. The parameter E_c, a, n_1 and n_2 are listed for various material compositions in reference [76]. The variable E denotes the magnitude of the electric field in the channel direction, i.e. the x-direction as indicated in figure 3.1. Figure 3.3 depicts the mobility profiles for GaN, InN, and AlN according to (3.3) with parameters taken from reference [76]. InN achieves a steady-state peak velocity of about $3.2 \cdot 10^7$ cm/s at about 65 kV/cm. The steady-state peak velocity of GaN is achieved at about 220 kV/cm and is about $2.9 \cdot 10^7$ cm/s. AlN reaches a steady-state peak velocity of about $2.3 \cdot 10^7$ cm/s at a critical field of about 430 kV/cm. Similar $v(E)$-profiles are obtained by another group [77, 75]. One major difference between references [77, 75] and reference [76] is that the steady-state peak velocity of GaN is expected to occur at a lower electrical field, i.e. 140 kV/cm instead of 220 kV/cm.

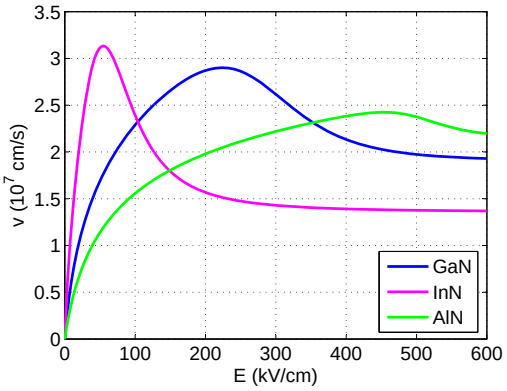

Figure 3.3: Electron drift velocity for GaN, InN and AlN at 300 K [76].

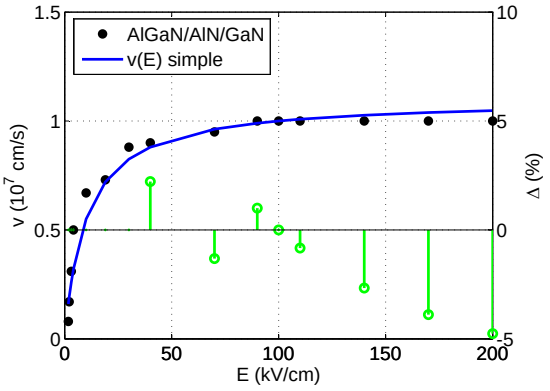

Figure 3.4: Simple $v(E)$-profile (3.4) and experimental data for AlGaN/AlN/GaN channel [78]. Δ denotes the relative error, plotted for $E > 40$ kV/cm.

For the derivation of analytical equations describing the basic HEMT behavior the $v(E)$-model according to (3.3) is not suitable. Hence a simplified model is assumed for the derivation [66, 72, 79] and it is given by equations (3.4) and (3.5).

$$v(E) = \frac{\mu_n E}{1 + E/E_c} \tag{3.4}$$

$$v_{sat} = \mu_n \cdot E_c \tag{3.5}$$

In the simple $v(E)$-model (3.4) the parameter E_c denotes the critical field at which the carrier velocity v attains half its saturation value. The simple $v(E)$-model does not approximate velocity-field profiles with a pronounced peak velocity v_{peak} as depicted in figure 3.3 well. However, for device modeling the charge transport at the AlGaN/GaN heterojunction [80, 81, 82] or AlGaN/AlN/GaN [83, 78] is of relevance if the HEMT as device type is focused. Figure 3.4 shows experimental data for the electron velocity as a function of applied electric field E taken from reference [78]. Additionally the simple $v(E)$-model is plotted in figure for $\mu_n = 1100\,\mathrm{cm}^2/\mathrm{Vs}$ and $v_{sat} = 1.1 \cdot 10^7\,\mathrm{cm/s}$. The resulting parameter E_c is $10\,\mathrm{kV/cm}$. The simple $v(E)$-model approximates the experimental data [78] well as for $E > 40\,\mathrm{kV/cm}$ the relative error does not exceed 5 percent.

The aforementioned steady-state electron transport is expected to dominate the performance of devices with dimensions greater than $0.2\,\mu\mathrm{m}$ [75]. Electron velocities up to $10 \cdot 10^7\,\mathrm{cm/s}$ are predicted for transient electron transport, also referred to as velocity overshoot effects. But so far the experimental data according to literature lack observed velocity overshoot effects in nitride HEMTs [84]. Discrepancies between experimental data and prediction on basis of simulation are attributed to two major sources [75]: uncertainty in the material properties and uncertainties in the underlying physics. Lower than expected device performance may be attributed to off-equilibrium phonons or so called hot phonons [78, 83]. Self-heating of the device causes an increase in lattice temperature and consequently degrade the electron transport properties [85].

3.4 Basic equations of DC operation

For the derivation of the basic HEMT equations a linear n_s-V_G relation ship according to (3.1) is assumed. Additionally it is assumed that the velocity of the carriers is independent of n_s and V_G and can be described according to a simple field-dependent-mobility model, given by (3.4). Furthermore the contribution of the gate leakage current to the drain current I_D is neglected so that I_D equals the source current. Let $V(x)$ denote the channel potential with the x coordinate as indicated in figure 3.1, the expressions (3.6) and (3.7) are derived for the drain current I_D.

$$I_D = e \cdot n_s(V_{GS}) \cdot v(E) \cdot W \tag{3.6}$$

$$= \frac{\mu_n c_0 W \cdot (V_{GS} - V_{th} - V(x)) \cdot \frac{dV(x)}{dx}}{1 + \frac{1}{E_c}\frac{dV(x)}{dx}} \tag{3.7}$$

L_G and W denote the gate length and the total gate width, respectively. The channel charge is conserved due to the lack of generation and recombination processes. Under DC operation, i.e. steady state conditions, there is no time dependence of the channel charge and hence charge conservation and the continuity equation imply a constant I_D along the x axis, i.e. $\frac{\partial I_D(x)}{\partial x} = 0$ [72]. Hence integration of (3.7) from $x = 0$ to $x = L_G$ reveals (3.8):

$$I_D\left(1+\frac{V_{DS}}{L_G E_c}\right)=\mu_n c_0 \frac{W}{L_G}\left((V_{GS}-V_{th})V_{DS}-\frac{{V_{DS}}^2}{2}\right) \tag{3.8}$$

3.4.1 Saturation drain current

When the drain current saturates due to the saturation of the carrier velocity, I_D becomes constant, i.e. $\frac{dI_D}{dV_{DS}}=0$. Setting the derivative $\frac{dI_D}{dV_{DS}}$ to zero reveals the expression for the drain-source voltage for which I_D saturates as given by (3.9) [66, 79].

$$V_{DS,sat}=\sqrt{(L_G E_c)^2+2(L_G E_c)(V_{GS}-V_{th})}-(L_G E_c) \tag{3.9}$$

With (3.8) and (3.9) the expression for the saturated drain current $I_{D,sat}$ is obtained.

$$I_{D,sat}=\frac{\mu_n c_0 W}{L_G}\cdot\frac{(L_G E_c)^2}{2}\left(\sqrt{1+\frac{2(V_{GS}-V_{th})}{(L_G E_c)}}-1\right)^2 \tag{3.10}$$

$$=\begin{cases}\dfrac{\mu_n c_0 W}{2L_G}\cdot(V_{GS}-V_{th})^2 & \text{, long-channel } (L_G E_c\to\infty)\\[2ex] v_{sat}c_0 W\cdot(V_{GS}-V_{th}) & \text{, short-channel } ((V_{GS}-V_{th})\gg L_G E_c)\end{cases} \tag{3.11}$$

Typical V_{th} values for normally-off AlGaN/GaN HEMTs are in the range of $-10\,\mathrm{V}$ [86] to $-0.14\,\mathrm{V}$ [87] depending on barrier thickness and composition. L_G might be as low as $30\,\mathrm{nm}$ [88]. E_c might be considered to be $10\,\mathrm{kV/cm}$ according to the discussion in section 3.3.

3.4.2 Transconductance

The intrinsic mutual transconductance under drain current saturation $g_{m,sat}=\frac{\partial I_{D,sat}}{\partial V_{GS}}$ is

$$g_{m,sat}=\frac{\mu_n c_0 W}{L_G}\cdot(L_G E_c)\cdot\left(1-\left(1+\frac{2(V_{GS}-V_{th})}{(L_G E_c)}\right)^{-1/2}\right) \tag{3.12}$$

$$=\begin{cases}\dfrac{\mu_n c_0 W}{L_G}\cdot(V_{GS}-V_{th}) & \text{, long-channel } (L_G E_c\to\infty)\\[2ex] v_{sat}c_0 W & \text{, short-channel } ((V_{GS}-V_{th})\gg L_G E_c)\end{cases} \tag{3.13}$$

3.4.3 Gate capacitance and transit time parameter

Let Q_{CH} denote the channel carrier stored charge then the gate capacitance can be defined as $C_{GS}=\partial Q_{CH}/\partial V_{GS}$. A detailed analysis in [66] reveals (3.14) for C_{GS} under saturation condition.

$$C_{GS} = \begin{cases} \frac{2}{3} c_0 L_G W & \text{, long-channel } (L_G E_c \to \infty) \\ c_0 L_{G,eff} W & \text{, short-channel } ((V_{GS} - V_{th}) \gg L_G E_c) \end{cases} \tag{3.14}$$

$L_{G,eff} = L_G + L_{GD}$ and hence $L_{G,eff}$ considers any channel region of length L_{GD} next to the gate metalization toward the drain side, which is still influenced by the electrical field of the gate electrode. L_{GD} itself is be assumed to be proportional to the gate-channel separation $(d + d_i + \Delta d)$ [89].

The introduction of the quantity Q_{CH} leads to the definition of the intrinsic transit time parameter τ_t given by (3.15)

$$\tau_t = \frac{\partial Q_{CH}}{\partial I_D} = \frac{\partial Q_{CH}/\partial V_{GS}}{\partial I_D/\partial V_{GS}} = \frac{C_{GS}}{g_m} \tag{3.15}$$

For short channel devices for which velocity saturation occurs throughout the channel including the external region L_{GD} the parameter τ_t becomes:

$$\tau_t = \frac{C_{GS}}{g_{m,sat}} = \frac{c_0 L_{G,eff} W}{v_{sat} \cdot c_0 \cdot W} = \frac{L_{G,eff}}{v_{sat}} \tag{3.16}$$

Hence τ_t represents the average time the charge needs to pass the effective gate length, i.e. the average transit time [65]. A quantity which is directly related to the transit time parameter τ_t is the intrinsic transit frequency $f_\tau = \frac{1}{2\pi\tau_t} = \frac{v_{sat}}{2\pi L_{G,eff}}$ [90].

The saturated velocity model for short channel devices according to (3.16) is a borderline case which assumes that all electrons under the gate travel at saturation velocity v_{sat}. If this most efficient mode of operation could by achieved the drain current I_D would equal $\frac{v_{sat}}{L_G} \cdot Q_{SV}$ where Q_{SV} denotes the channel charge moving according to the saturation velocity model, i.e. moving with v_{sat}. Since v_{sat} is an upper limit for the electron velocity there is also some charge moving at lower velocity and hence current continuity requires that an additional charge $Q_{\Delta GC}$ has to be modulated. $Q_{\Delta GC}$ achieves its maximum at the source side of the gate as here is low electric field region in comparison to the high electric field region at the drain side of the gate. Additionally parasitic charge in the barrier layer Q_{BL} might also be modulated by the in the gate electrode. The modulated excess charges $Q_{\Delta GC}$ and Q_{BL} degrades the performance of the HEMT which is typically accounted for by the introduction of a factor $\eta \leq 1$ called Modulation Efficiency (ME) defined by (3.17) [91, 70, 92].

$$\eta = \frac{\partial Q_{SV}}{\partial (Q_{SV} + Q_{\Delta GC} + Q_{BL})} \tag{3.17}$$

Hence the ideal expression for the intrinsic transit frequency f_τ can be augmented by the introduction of the ME leading to (3.18).

$$f_\tau = \left(\frac{v_{sat}}{2\pi L_{G,eff}} \right) \cdot \eta \tag{3.18}$$

3.5 Access resistances and their influences on DC parameters

So far (3.6) to (3.16) of this chapter are only related to the intrinsic device, because the source and drain access resistances are not considered. But the current flow through the access region causes voltage drops and hence the voltages at the intrinsic device differ from those externally applied at the metal contact pads.

Figure 3.5 shows the current flow from the intrinsic device though the source access region to the metal pad which builds the source contact. Two resistances contribute to the total source contact resistance R_S. The first contribution is the semiconductor material between ohmic contact and intrinsic device. Its contribution is $R_\square \cdot \frac{d_{SG}}{W}$ where $R_\square$ is the sheet resistance of the semiconductor and d_{SG} is the distance between source contact and the intrinsic device. The second contribution originates from the contact resistance R_c itself. For the determination of R_c the metal-semiconductor junction may be modeled by a single transmission line structure as shown in figure 3.5 if metal layer, semiconductor layer and interface are considered to be homogeneous.

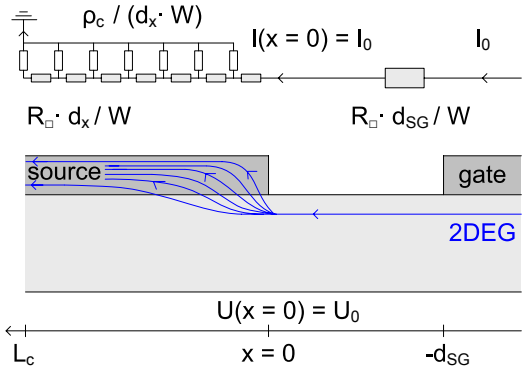

Figure 3.5: Schematic cross-sectional view of the ohmic contact and the access region. A single TLM structure is depicted as equivalent circuit.

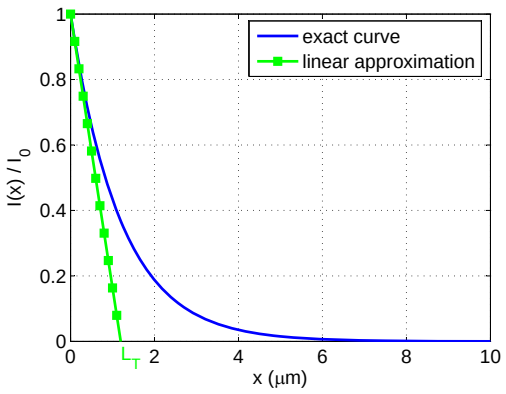

Figure 3.6: Current flow under a ohmic contact metalization. $R_\square = 350\,\Omega$, $\rho_c = 5.0 \cdot 10^{-6}\,\Omega\cdot\text{cm}^2$, $L_c = 10\,\mu\text{m}$ are assumed.

Applying the single Transmission Line Model (TLM) the current under the ohmic contact as a function of x, i.e. $I(x)$, can be described by (3.19) [93],

$$I(x) = I_0 \cdot cosh(\gamma \cdot x) - \frac{U_0}{\sqrt{R_\square\,\rho_c}} \cdot W \cdot sinh(\gamma \cdot x) \tag{3.19}$$

where the real constant $\gamma = \sqrt{\frac{R_\square}{\rho_c}}$ corresponds to the propagation constant of RF-transmission line models. The parameter ρ_c denotes specific contact resistance. In figure 3.6 the normalized current $I(x)/I_0$ is plotted as a function of x for typical material parameters. Additionally the linear approximation for $I(x)/I_0$ for $x = 0$ is plotted in figure 3.6. The linear approximation of $I(x)/I_0$ intersects the x axis at $L_T = \frac{1}{coth(\gamma \cdot L_c)\cdot\gamma}$, where L_T is the characteristic transfer length. In a distance of $3 \cdot L_T$ from the origin about 95 % of the current have commutated from the semiconductor to the ohmic metalization, as depicted in figure 3.6.

The contact resistance R_c itself is defined as input resistance to the TLM structure, i.e. $R_c = \frac{U_0}{I_0}$. Considering that the current flowing in x-direction through the semiconductor

has to be zero at the end of the ohmic metalization, i.e. $I(x = L_c) = 0$, the contact resistance R_c is given by (3.20)

$$R_c = \frac{\sqrt{R_\square \, \rho_c}}{W} \cdot coth(\gamma \cdot L_c) \tag{3.20}$$

By choosing L_c sufficiently large, e.g. $L_c > 3 \cdot L_T$, the contact resistance R_c becomes independent from L_c and depends only on the width W. With $coth(\gamma \cdot L_c) \approx 1$ for $\gamma \cdot L_c \gg 1$ a simple form for R_c is given by (3.21).

$$R_c \cdot W = \sqrt{R_\square \cdot \rho_c} = \frac{\rho_c}{L_T} \tag{3.21}$$

Consequently the total source resistance R_S for a HEMT under DC operation is given by (3.22)

$$R_S = R_c + R_\square \cdot \frac{d_{SG}}{W} = \frac{1}{W}(\sqrt{R_\square \cdot \rho_c} + R_\square \cdot d_{SG}) \tag{3.22}$$

with analog considerations for the drain resistance R_D. If velocity saturation effect in the semiconductor region can be neglected [94], R_S and R_D are linear ohmic resistors which are only dependent on the width W and the material/contact properties according to (3.22).

The impact of R_S and R_D on the DC behavior is typically accounted for by (3.23) and (3.24).

$$V_{GS,ext} = V_{GS} + R_S \cdot I_D \tag{3.23}$$

$$V_{DS,ext} = V_{DS} + (R_S + R_D) \cdot I_D \tag{3.24}$$

Insertion of (3.23) and (3.24) to 3.8 results in a quadratic equation in I_D which can be solved numerically in order to study the impact of R_S and R_D on the output characteristic. Figure 3.7 shows a typical output characteristic of a HEMT and the influence of the access resistances on it. While an increase in R_S causes an increase in the on-resistance and a reduction in the maximum drain current, the resistance R_D has only impact on the on-resistance, but not the maximum drain current.

It follows from (3.23) and (3.24) that the extrinsic DC transconductance $g_{m,ext}$ is given by (3.25)

$$g_{m,ext} = \frac{g_m}{1 + g_m \cdot R_S + g_d \cdot (R_S + R_D)} \tag{3.25}$$

$$\approx \frac{g_m}{1 + g_m \cdot R_S} \tag{3.26}$$

with $g_m = \frac{\partial I_D}{\partial V_{GS}}$ as intrinsic mutual transconductance and $g_d = \frac{\partial I_D}{\partial V_{DS}}$ as intrinsic drain transconductance [72]. Typically $g_d \gg (R_S + R_D)^{-1}$ is assumed and the simple expression (3.26) is commonly used [95, 94, 96]. The impact of a non-zero source resistance on the

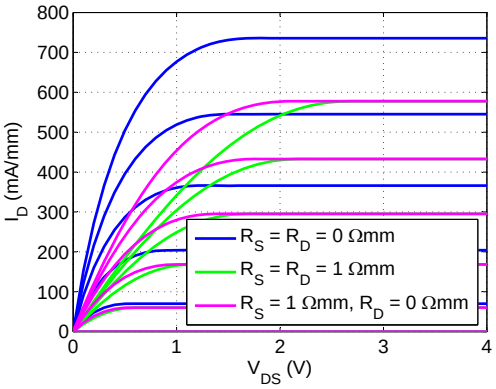

Figure 3.7: Ideal output characteristic under the influence of access resistances R_S and R_D.

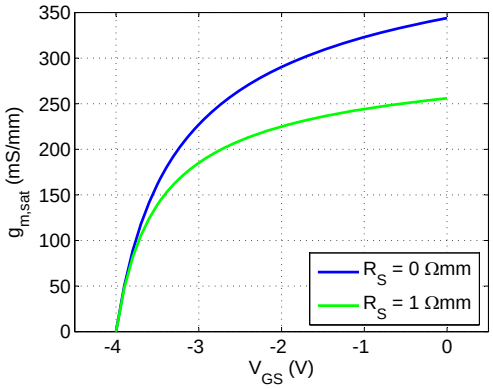

Figure 3.8: Influence of the source resistance R_S on the transconductance under saturation condition.

transconductance is depicted in figure 3.8. As can been seen in figure 3.8 the source access resistance R_S reduces the transconductance in comparison to its intrinsic value.

It is important to note that R_S also affects the extrinsic gate-source capacitance $C_{GS,ext} = \frac{\partial Q_{CH}}{\partial V_{GS,ext}}$ such that $C_{GS,ext} = \frac{C_{GS}}{(1+g_m \cdot R_S)}$ [90, 66, 69, 95]. Hence a change in the extrinsic transit time $\tau_{t,ext} = \frac{C_{GS,ext}}{g_{m,ext}} = \frac{C_{GS}}{g_m}$ is not expected in the context of this model if R_S is altered. This is because the described model neglects the feedback mechanism caused by the gate-drain capacitance. A model which accounts for the gate-drain capacitance is described in section 5.3.

3.6 Small signal Y-parameter

The DC current-voltage dependencies discussed in 3.4 characterize the HEMT as nonlinear device. Hence in circuit applications, where the transistors terminal voltages toggle between two extreme values, the transistor characteristics change drastically during the transient. But if the voltage changes represent only small perturbation in the vicinity of a fixed bias point (V_{GS},V_{DS}), the current response is a linear combination of these small voltage changes according in a first order approximation, given in (3.27).

$$I_D(V_{GS} + \tilde{v}_{gs}, V_{DS} + \tilde{v}_{ds}) \approx I_D(V_{GS}, V_{DS}) + \frac{\partial I_D}{\partial V_{GS}} \cdot \tilde{v}_{gs} + \frac{\partial I_D}{\partial V_{DS}} \cdot \tilde{v}_{ds} \tag{3.27}$$

Sinusoidal perturbations of the applied voltages are of particular interest, i.e. $\tilde{v}_{gs} = v_{gs} \cdot e^{j\omega t}$ and $\tilde{v}_{ds} = v_{gs} \cdot e^{j\omega t}$ with v_{gs} and v_{ds} as complex phasors and ω as radian frequency being equal to $2\pi \cdot f$.

Modeling the HEMT as two-terminal device with the gate and source electrode being port 1 and the drain and source electrode being port 2 the small-signal sinusoidal relationship between the current and voltage phasors at the ports are given by (3.28).

$$\begin{bmatrix} i_g \\ i_d \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} v_{gs} \\ v_{ds} \end{bmatrix} \tag{3.28}$$

i_g and i_d are the phasors of the sinusoidal small-signal gate current and drain current, respectively. Y_{mn} with $m, n \in (1,2)$ in (3.28) denote the small-signal Y-parameter for the common source configuration of the HEMT.

In contrast to the discussion of the DC operation of a HEMT in 3.4 a full time dependent, i.e. non-static, analysis of the HEMT is challenging. Even if the following assumptions regarding the device operation are made:

- Free channel charge is conserved and hence continuity equation holds, i.e. no combination or recombination processes.
- Simplified charge control model according to (3.2) is valid.
- Current flow is governed by the drift equation with a constant mobility μ_n, i.e. velocity saturation is neglected.

the analysis already results in a second-order nonlinear partial differential equation which can only by solved numerically [72]. Nevertheless, if a harmonic time dependence is assumed an analytical solution is possible and given in [72]. If higher order terms of the solution are neglected the small-signal Y-parameter for the common source configuration can be found to be:

$$Y_{11,qs} \approx j\omega(C_{gs} + C_{gd}) \tag{3.29}$$
$$Y_{12,qs} \approx -j\omega C_{gd} \tag{3.30}$$
$$Y_{21,qs} \approx g_m - j\omega C_{dg} \tag{3.31}$$
$$Y_{22,qs} \approx g_d + j\omega(C_{gd} + C_{sd}) \tag{3.32}$$

The values of the capacitances C_{gs}, C_{gd}, C_{dg} and C_{sd} can be determined from a quasi-static analysis [72] and hence (3.29) to (3.32) are also referred to as quasi-static Y-parameter. Considering higher order terms of the analytical solution presented in [72] in order to increase the accuracy of the small-signal model reveals:

$$Y_{11} + Y_{12} \approx \left(R_i + \frac{1}{j\omega C_{gs}} \right)^{-1} \tag{3.33}$$
$$-Y_{12} \approx j\omega C_{gd} \tag{3.34}$$
$$Y_{22} + Y_{12} \approx g_d + j\omega C_{sd} \tag{3.35}$$
$$Y_{21} - Y_{12} \approx g_m(1 + j\omega\tau) \tag{3.36}$$

The important difference between the quasi-static model ((3.29) to (3.32)) and the more accurate one given by (3.33) to (3.36) is the introduction of the element R_i, referred to as channel resistance. Equations (3.33) to (3.36) are the basis for the intrinsic small-signal equivalent circuit shown in figure 3.9. This intrinsic small-signal equivalent circuit can also be found in [97, 98, 99, 60, 100] while the dependence $g_m(\tau)$ varies upon the different publications.

In order to model the environment of the device the intrinsic small-signal equivalent circuit it is extended by a parasitic Z- and Y-shell [101, 102] which are also shown in figure 3.9. The elements of the parasitic Z- and Y-shell are referred to as extrinsic elements and are

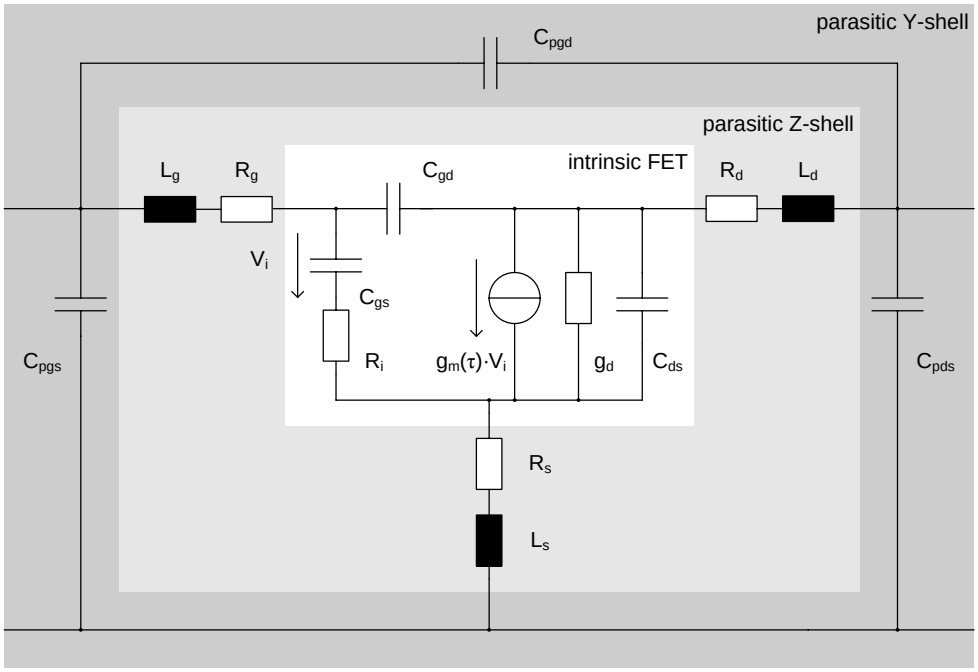

Figure 3.9: Small-signal equivalent circuit of a FET.

generally considered to be independent of the applied bias condition. As shown in figure 3.10 the capacitances C_{pgs}, C_{pds} and C_{pgd} are associated with the pad metalization. Their values can be obtained from an electrostatic analysis [72] and they range in the order of a few fF to about 30 fF for typical pad layouts [101, 103, 92].

Generally the elements of the intrinsic part are considered to be bias-dependent in contrast to the extrinsic elements which are considered to be bias-independent [39, 98, 104]. However, it should be emphasized that especially the values of R_s and R_d in the small-signal model might well be bias-dependent due to velocity saturation effects in the extrinsic device [94]. In this sense a simple linear model for access resistances of a HEMT as discussed in 3.5 might not be adequate [94] and the differential source and drain access resistance R_s and R_d have to be considered instead [103]. In a consequence the widely used Cold-FET/Hot-FET extraction method, which determines the extrinsic elements of the small-signal model at zero drain bias, has to be reconsidered [99]. This is especially true for HEMTs in the AlGaN/GaN material system as in this case the Cold-FET-values for R_s and R_d might dramatically differ from those values determined under operating bias [105, 60], as also discussed in chapter 2 of this work.

3.7 Summary

This chapter discusses the basic models which govern the DC and small-signal behavior of a HEMT. By the means of the presented models the HEMT behavior and characteristics can be linked to the specific device geometry like for instance gate length L_G and to the material parameters like the saturation velocity v_{sat}. Beside the simple description of fundamental

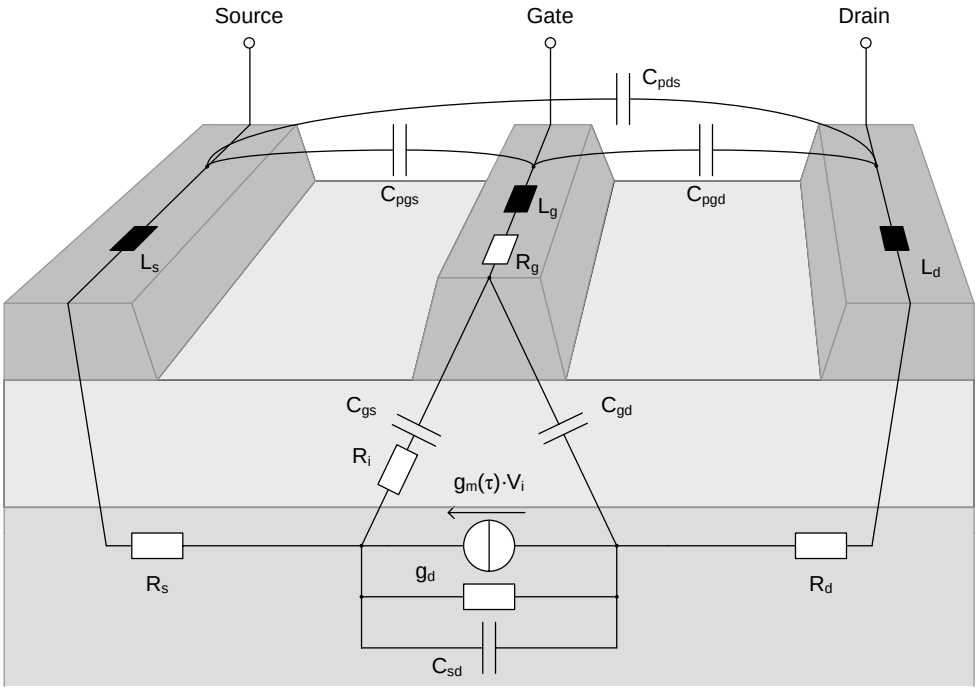

Figure 3.10: Lumped elements of the small-signal equivalent circuit associated to the cross-sectional structure of a HEMT.

device behavior the specific assumptions made for each model are emphasized in this chapter. In this way it is possible to discuss limits of application of the presented models. Although the models presented may be augmented to model the device performance more accurately they provide a helpful starting point to give first order estimates on the impact of the various design parameters on the device performance.

CHAPTER 4

High-Frequency Figure of Merits

The high-frequency performance of a device embedded in a circuit environment can be as dependent on the circuit environment as on the device itself [65]. Therefore an appropriate high-frequency figure of merit should be inherent to the device and not an artifact of its environment. Thus a device figure of merit should abstract from the specific circuit environment to a reasonable degree and it should be invariant to some changes in the circuit environment [106]. Typically high-frequency transistors are characterized by different power gains which are obtained from network-analyzer measurements. Different assumptions about the circuit environment, in which the device might be embedded, lead to different definitions of power gains and as a consequence to different high-frequency figures of merit. This chapter outlines the relevant figures of merit by which a transistor can be characterized regarding its high frequency properties. The focus is set on the two most commonly used high-frequency figures of merit, which are the current-gain cut-off frequency f_T and the maximum frequency of oscillation f_{max}.

4.1 Characterization of two-port networks by scattering-parameters

Field effect transistors are generally considered as three-terminal[1] devices [107] with the terminals gate (G), source (S) and drain (D). If the FET is biased in a common source configuration then the resulting terminal pairs gate-source and drain-source build a two-port network. Two-port networks are unambiguously described by 2×2 matrix of network parameters (cf. e.g. [108]). Commonly the network parameters are given as admittance-parameters (Y-parameters), impedance-parameters (Z-parameters) or Hybrid-parameters (H-parameters).

In order to determine a set of Y-parameters or Z-parameters, by measurement one port of the network has to be terminated with an short or an open, respectively. But in practice a port can not be shunted properly with an open or an short at high-frequencies. For example, the measurement of the complex Y-parameters is only applicable up to 100 MHz [109]. The measurement of the Scattering-parameters (S-parameters) does not require open or short terminations and therefore they are nowadays commonly utilized for the high-frequency characterization of two-port networks [27]. In the case of scattering parameters the ports of a network are shunted with a reference impedance.

The case of a two-port is depicted in figure 4.1 with the reference impedances Z_{01} and Z_{02}. Typically $Z_{01} = Z_{02} = Z_0 = 50\,\Omega$ is chosen, but the definition of scattering parameters generally allows for an arbitrary complex impedance Z_0. The Device Under Test (DUT) is stimulated with incident power waves $a_{m=1,2}$ and the reflected waves $b_{n=1,2}$ are observed. The corresponding S-parameters are defined as $S_{n1} = \frac{b_n}{a_1}|_{a_2=0}$ and $S_{n2} = \frac{b_n}{a_2}|_{a_1=0}$ with $n = 1, 2$. Network-parameters and S-parameters are strictly related to certain reference

[1] For integrated MOSFETs the bulk terminal has to be considered as a fourth terminal

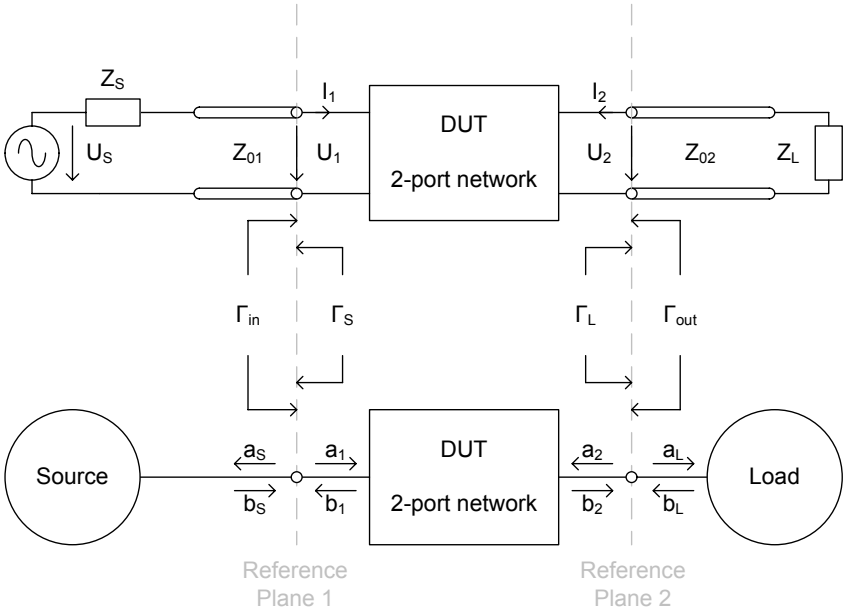

Figure 4.1: Small-signal equivalent circuit of a FET.

planes which define the device boundaries and separate it from its environment. Network-parameters and S-parameters are unambiguously related to each other. The relations between S-parameters and Y-parameters and S-parameters and Z-parameters for a N-port network are given by (4.1) and (4.2) [110].

$$\bar{\boldsymbol{Y}} = (\boldsymbol{E} - \boldsymbol{S})(\boldsymbol{E} + \boldsymbol{S})^{-1} \qquad \boldsymbol{S} = (\boldsymbol{E} - \bar{\boldsymbol{Y}})(\boldsymbol{E} + \bar{\boldsymbol{Y}})^{-1} \qquad \bar{\boldsymbol{Y}}, \boldsymbol{S} \in \mathbb{C}^{N \times N} \tag{4.1}$$

$$\bar{\boldsymbol{Z}} = (\boldsymbol{E} + \boldsymbol{S})(\boldsymbol{E} - \boldsymbol{S})^{-1} \qquad \boldsymbol{S} = (\bar{\boldsymbol{Z}} - \boldsymbol{E})(\bar{\boldsymbol{Z}} + \boldsymbol{E})^{-1} \qquad \bar{\boldsymbol{Z}}, \boldsymbol{S} \in \mathbb{C}^{N \times N} \tag{4.2}$$

The matrix $\boldsymbol{S}$ denotes the scattering-matrix containing the S-parameters $S_{m,n}$ with $m, n = 1 \ldots N$. $\boldsymbol{E}$ is the corresponding unity matrix. The matrices $\bar{\boldsymbol{Y}}$ and $\bar{\boldsymbol{Z}}$ denote the normalized admittance- and impedance-matrix, respectively. The normalized Y-parameters are related to the Y-parameters by $\bar{Y}_{mn} = \sqrt{Z_{0m}}\sqrt{Z_{0n}}\, Y_{mn}$ with Z_{0n} as reference impedance of the n-th port. In analogy $\bar{Z}_{mn} = \sqrt{Z_{0m}}^{-1}\sqrt{Z_{0n}}^{-1} Z_{mn}$ relates the normalized Z-parameters to the Z-parameters.

The H-parameters are usually only defined for a 2-port network. Hence the unambiguous relation between H-parameters and S-parameters lacks a general N-port-expression as in the case of Y- and Z-parameters (cf. (4.1) and (4.2)). Therefore the relevant relations between S-parameters and H-parameters are listed in table 4.1. H_{mn} with $m, n = 1, 2$ denote the H-parameters whereas $\bar{H}_{mn}$ denote the normalized parameters.

4.2 Stability of a two-port network

The Maximum Stable Gain (MSG) and the Maximum Available Gain (MAG) are two common figures of merit to characterize a device regarding its high-frequency properties [27]. But the definition of MSG and MAG is strongly related to the stability factor K after J. M. Rollet [111]. Therefore it is necessary to define the stability of a two-port network

Table 4.1: Relation between S-parameters and H-parameters for a two-port network.

$\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \quad \longleftrightarrow \quad \begin{pmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{pmatrix}$		
$S_{11} = \frac{(\bar{H}_{11}-1)(\bar{H}_{22}+1)-\bar{H}_{12}\bar{H}_{21}}{(\bar{H}_{11}+1)(\bar{H}_{22}+1)-\bar{H}_{12}\bar{H}_{21}}$	$\bar{H}_{11} = \frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}$	$\bar{H}_{11} = \frac{1}{Z_{01}} H_{11}$
$S_{12} = \frac{2\bar{H}_{12}}{(\bar{H}_{11}+1)(\bar{H}_{22}+1)-\bar{H}_{12}\bar{H}_{21}}$	$\bar{H}_{12} = \frac{2S_{12}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}$	$\bar{H}_{12} = \frac{\sqrt{Z_{02}}}{\sqrt{Z_{01}}} H_{12}$
$S_{21} = \frac{-2\bar{H}_{21}}{(\bar{H}_{11}+1)(\bar{H}_{22}+1)-\bar{H}_{12}\bar{H}_{21}}$	$\bar{H}_{21} = \frac{-2S_{12}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}$	$\bar{H}_{21} = \frac{\sqrt{Z_{02}}}{\sqrt{Z_{01}}} H_{21}$
$S_{22} = \frac{(\bar{H}_{11}+1)(1-\bar{H}_{22})+\bar{H}_{12}\bar{H}_{21}}{(\bar{H}_{11}+1)(\bar{H}_{22}+1)-\bar{H}_{12}\bar{H}_{21}}$	$\bar{H}_{22} = \frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}$	$\bar{H}_{22} = Z_{02} H_{22}$

in advance. A linear two-port network, as depicted in figure 4.1, is called unconditionally stable if the input-admittance Y_{in} and the output-admittance Y_{out} are passive, if the output and input port are shunted with any passive output load Y_L or Y_S, respectively. So the condition for a linear two-port network to be unconditionally stable is given by [112]

$$\bigvee Y_S, Y_L \qquad \text{with} \quad Re\{Y_S\}, Re\{Y_L\} > 0 \tag{4.3}$$

$$\Longrightarrow \qquad Re\{Y_{in}\} = Re\left\{Y_{11} - \frac{Y_{21}Y_{12}}{Y_{22}+Y_L}\right\} > 0 \tag{4.4}$$

$$\Longrightarrow \qquad Re\{Y_{out}\} = Re\left\{Y_{22} - \frac{Y_{21}Y_{12}}{Y_{11}+Y_S}\right\} > 0 \tag{4.5}$$

The conditions (4.3) to (4.4) are necessary and sufficient for the unconditional stability of a linear two-port network, if a special class of networks, i.e. reciprocal with negative resistances, is excluded from the set of linear two-ports [113, 109]. Especially the conditions are valid in case of linear two-port representing three-terminal devices, which is the relevant case in this thesis.

It is more convenient to discuss the stability in terms of S-parameters. Considering that the relation between a reflection coefficient Γ_i is related to the corresponding normalized admittance $\bar{Y}_i$ by $\Gamma_i = (1-\bar{Y}_i)(1+\bar{Y}_i)^{-1}$, which is the bilinear transform defining the Smith-Chart, the condition for unconditional stability in terms of S-parameters are [109]:

$$\bigvee \Gamma_S, \Gamma_L \qquad \text{with} \quad |\Gamma_S|, |\Gamma_L| < 1 \tag{4.6}$$

$$\Longrightarrow \qquad |\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{4.7}$$

$$\Longrightarrow \qquad |\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{4.8}$$

The conditions (4.6) to (4.8) express that any incident wave a_i at port one or port two causes a corresponding reflected wave b_i at the same port which is less or equal in magnitude than $|a_i|$, no matter what shunt is chosen for the termination of the other port. In the case a unilateral two-port device, i.e. $S_{12} = 0$, the conditions for $|\Gamma_{in}|$ and $|\Gamma_{out}|$ simplify to $|\Gamma_{in}| < |S_{11}|$ and $|\Gamma_{out}| < |S_{22}|$.

It may be shown, e.g. in [112], that the conditions for unconditional stability (4.4) and (4.5) are met if the conditions (4.9) and (4.10) are met.

$$K(\boldsymbol{Y}) = \frac{2Re\{Y_{11}\}Re\{Y_{22}\} - Re\{Y_{21}Y_{12}\}}{|Y_{21}Y_{12}|} > 1 \tag{4.9}$$

$$Re\{Y_{11}\} > 0 \quad \text{and} \quad Re\{Y_{22}\} > 0 \tag{4.10}$$

The factor K of (4.9) is called the Rollet stability factor. Its invariants to certain two-port modification are discussed in reference [111] by Rollet. Due to its invariants the Rollet stability factor K does not just define the boundary between unconditional and conditional stability but may be seen as more fundamental property of a linear two-port in the same sense as Mason's U is an inherent two-port figure of merit (cf. section 4.5). Although the presented considerations regarding linear two-port stability might lead to slightly different definitions of stability factors, like for instance the Stern stability factor, the Rollet stability factor K is the one which is nowadays commonly and almost exclusively used [109]. The analog criteria to (4.9) to (4.10) in terms of the more common S-parameters are given by (4.11) to (4.12) [114, 115, 113].

$$K(\boldsymbol{S}) = \frac{1 - |S_{11}| - |S_{22}| + |\Delta|^2}{2|S_{21}S_{12}|} > 1 \tag{4.11}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{4.12}$$

4.3 Power gain definitions

The various gain definitions basically differ from each other in that sense that some definitions refer to the absorbed power of a network port, but especially the most relevant definitions, like the MAG, refer to the available power of the source $P_{S,av}$ or the available power of one of the two network ports, i.e. $P_{1,av}$ or $P_{2,av}$, respectively. So it is necessary for the definition of several high-frequency gains to define the available power of a high-frequency source in advance [107], what is done in appendix A.1.

4.3.1 Operating power gain

The operating power gain G as function of the S-parameters is defined by (4.13) [27, 112].

$$\begin{aligned} G &= \frac{\text{transferred power from port 2 to the load}}{\text{transferred power from the source to port 1}} = \frac{P_L}{P_1} \\ &= \frac{1}{1-|\Gamma_{in}|^2}\,|S_{21}|^2\,\frac{1-|\Gamma_L|^2}{|1-\Gamma_L S_{22}|^2} \end{aligned} \tag{4.13}$$

The operating power gain depends only the S-parameters of the amplifier and the load, characterized by the reflection coefficient Γ_L. How well an amplifier-load combination makes use of available source power $P_{S,ab}$ is not indicated by operating power gain. In this way one might think of an amplifier-load combination with a certain G which delivers less power to the load than it would be achieved by the means of directly matching the load to the source. Therefore it is meaningful to relate a power gain definition to the available power of a source as it is done for the transducer power gain definition in the following.

4.3.2 Transducer power gain

The transducer power gain G_T is defined as (4.14) [27, 112].

$$\begin{aligned} G_T &= \frac{\text{transferred power from port 2 to the load}}{\text{available power of the source}} = \frac{P_L}{P_{S,av}} \\ &= \frac{1-|\Gamma_S|^2}{|1-\Gamma_{in}\Gamma_S|^2}\,|S_{21}|^2\,\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \end{aligned} \tag{4.14}$$

Although the definition G_T is related to the $P_{S,av}$ this does not imply that in the definition of G_T the matching condition $\Gamma_S = \Gamma_{in}{}^*$ is fulfilled. In the special case, where the matching condition is satisfied, the transducer power gain G_T equals the operating power gain G [27].

4.3.3 Unilateral transducer power gain

The transducer power gain G_T becomes the unilateral power gain G_{TU}, if in (4.14) the feedback from port 2 to port 1 is neglected by setting $S_{12} = 0$. Hence the definition of the unilateral transducer power gain is given by (4.15) [39].

$$G_{TU} = \left.\frac{P_L}{P_{S,av}}\right|_{S_{12}=0} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}\,|S_{21}|^2\,\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{4.15}$$

4.3.4 Available power gain

The available power gain G_A is defined by (4.16) [27, 112]

$$G_A = \frac{\text{available power of port 2}}{\text{available power of the source}} = \frac{P_{2,av}}{P_{S,av}} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}\,|S_{21}|^2\,\frac{1}{1-|\Gamma_{out}|^2} \tag{4.16}$$

The G_A equals G_{TU} if the load and port 2 are accidentally matched. All the gain definitions G, G_T, G_{TU} and G_A consider the environment of active two-port network. Hence they are only conditionally useful to characterize a device regarding its high frequency properties, but important in the field of amplifier design. Nevertheless, their definition directly lead to the definition of the maximum unilateral transducer power gain $G_{TU,max}$ and the maximum available gain MAG, which solely depend on the S-parameters of the active two-port and hence are important high-frequency figures of merit for device characterization.

4.3.5 Maximum unilateral transducer power gain

The maximum unilateral transducer power gain $G_{TU,max}$ is derived from the definition of G_{TU} by the assumption that the source and the load are matched to the unilateral two-port. Hence the definition of the $G_{TU,max}$ is defined by (4.17) [39].

$$G_{TU,max} = G_{TU}|_{\Gamma_S=S_{11}{}^*,\Gamma_L=S_{22}{}^*} = \frac{1}{1-|S_{11}|^2}\,|S_{21}|^2\,\frac{1}{1-|S_{22}|^2} \tag{4.17}$$

The $G_{TU,max}$ is barely used as high-frequency figure of merit in literature. However, because $G_{TU,max}$ solely depends on the S-parameters, it is also a useful quantity to characterize a device with respect to its high-frequency properties and hence it is listed in this chapter for the sake of completeness.

4.4 Maximum stable gain and maximum available gain

The MAG originates from the available power gain G_A if it is additionally assumed that the source reflection factor Γ_S is matched to the port 1 reflection factor Γ_1. In this case the source and the load reflection factors are optimally chosen and are referred to as $\Gamma_{S,opt}$ and $\Gamma_{L,opt}$. But only if the two-port network is unconditionally stable (cf. section 4.2) input and output can be matched to the source and load simultaneously [112]. Hence the MAG is only defined for $|K| > 1$ [27]. This is way it is common to express the MAG as a function of K.

$$\text{MAG} = G_A|_{\Gamma_S=\Gamma_{S,opt},\Gamma_L=\Gamma_{L,opt}} = \left|\frac{S_{21}}{S_{12}}\right|\,(K-\sqrt{K^2-1}) \tag{4.18}$$

At the boundary of stability the MAG becomes the maximum stable gain MSG.

$$\text{MSG} = \text{MAG}|_{K=1} = \left|\frac{S_{21}}{S_{12}}\right| \tag{4.19}$$

Because K only depends on the S-parameters, MAG and MSG do and therefore they are typical quantities to characterize a device regarding its high frequency properties. Fig 4.2 shows the various relevant gains as function of frequency for a HEMT build in this work.

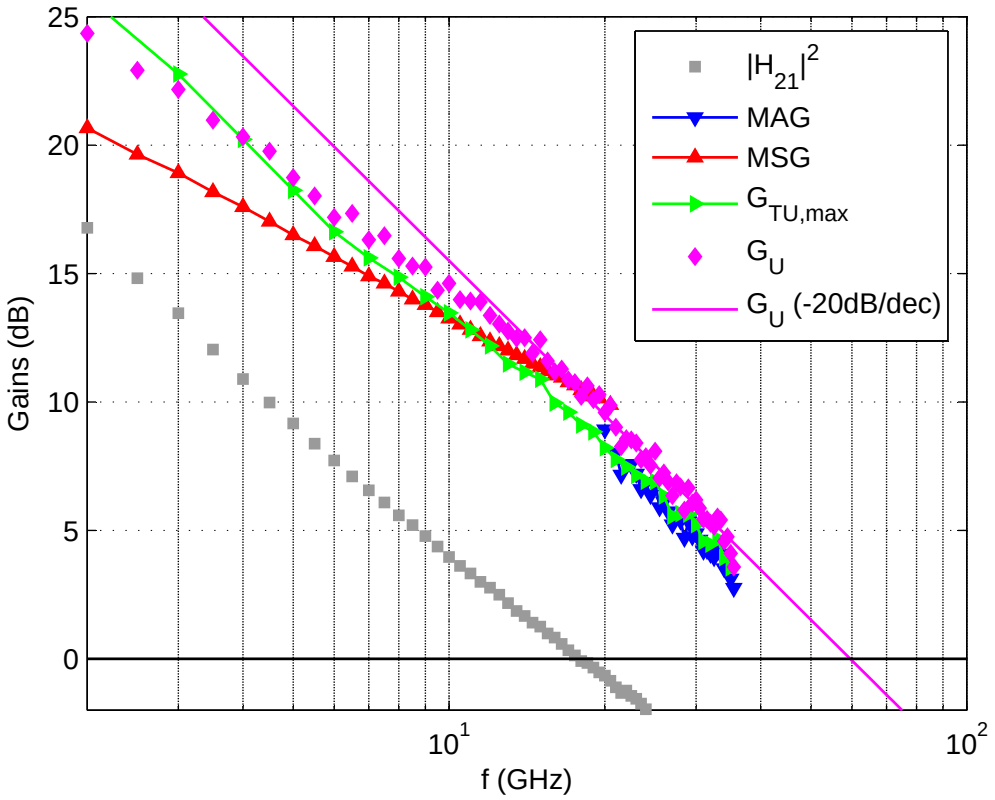

Figure 4.2: High frequency power gains for a AlGaN/GaN HEMT processed in this work.

4.5 Unilateral power gain and maximum frequency of oscillation

In this section the unilateral power gain G_U is defined and its origin as fundamental parameter of a linear two-port is discussed. The definition of G_U directly leads to the definition of the maximum frequency of oscillation f_{max}.

4.5.1 Unilateral power gain

In his 1954 publication [116] S. J. Mason discussed that the quantity $U = U(\boldsymbol{Z})$, defined by (4.20) and also referred to as G_U in this work, is invariant to lossless reciprocal four-port embeddings of the linear two-port network which may be described by a impedance matrix $\boldsymbol{Z}$ [106].

$$G_U = \frac{|Z_{12} - Z_{21}|^2}{4(Re\{Z_{11}\}Re\{Z_{22}\} - Re\{Z_{12}\}Re\{Z_{21}\})} = \frac{|det(\boldsymbol{Z} - \boldsymbol{Z}^T)|}{det(\boldsymbol{Z} + \boldsymbol{Z}^*)} \quad (4.20)$$

It is possible to transform an active two-port network characterized by $\boldsymbol{Z}$ into a unilateral two-port network $\boldsymbol{Z}'$ by the means of a lossless reciprocal four-port embedding. According to the definition of G_{TU} in section 4.3 unilateralization is achieved if $Z'_{12} = 0$. Due to the invariance of Mason's U the quantity $U(\boldsymbol{Z})$ equals $U(\boldsymbol{Z}')$. In this sense Mason's U is a figure of merit intrinsic to the device as it is Rollet's K. Because the quantity U equals the MAG of the unilateralized two-port network, i.e. $U(\boldsymbol{Z}) = MAG(\boldsymbol{Z}')$ [27], $MAG(\boldsymbol{Z}')$ is also the definition of the unilateral power gain G_U. Of course G_U maybe expressed in terms of S-parameters [114, 106]:

$$U = \frac{|S_{12} - S_{21}|^2}{det(\boldsymbol{I} - \boldsymbol{S}\boldsymbol{S}^*)} = \frac{\frac{1}{2}\left|\frac{S_{12}}{S_{21}} - 1\right|^2}{K\left|\frac{S_{12}}{S_{21}}\right| - Re\left(\frac{S_{12}}{S_{21}}\right)} \tag{4.21}$$

The G_U is one of the most fundamental figures of merit which is used in the characterization of a three terminal device.

4.5.2 Maximum frequency of oscillation

The frequency f at which $G_U(f)$ becomes unity is defined as maximum frequency of oscillation f_{max} [27]. Sometimes f_{max} is also defined as the frequency at which the MAG becomes unity [117]. In practice the difference is of minor relevance and diminishes if the transistor is unilateral. In this thesis the definition (4.22) is used.

$$G_U(f)|_{f=f_{max}} = 1 = 0\,\text{dB} \tag{4.22}$$

f_{max} is an important figure of merit because it indicates the highest frequency at which a device can amplify the power of a signal [65].

4.6 Short-circuit current-gain cut-off frequency

As f_{max}, the definition of the short-circuit current-gain cut-off frequency f_T bases on a gain definition. The forward current gain of a two-port device with the output shortened is denoted by the hybrid-network parameter H_{21}. The frequency at which this gain extrapolates to one is the quantity f_T[65].

$$|H_{21}(f)|^2\Big|_{f=f_T} = 1 = 0\,\text{dB} \tag{4.23}$$

$|H_{21}|$ in dB is defined as $20 \cdot log_{10}(|H_{21}|) = 10 \cdot log_{10}(|H_{21}|^2)$ in contrast to the power gains defined in this chapter whose dB definition is $10 \cdot log_{10}$(value of the gain). Consequently the magnitude squared of H_{21}, i.e. $|H_{21}|^2$, has to be extrapolated with a slope of -20 dB per decade as it is done for the various power gain depicted in figure 4.2. It should be noted that $f_T > f_{max}$ or $f_T \leqslant f_{max}$ is possible depending on device particularities [65].

4.7 Summary

In this chapter the most relevant high frequency figures of merits f_T and f_{max} are defined for the use in this work and they are discussed in the context of basic two-port theory. However, these figures have to be related to the HEMT small-signal equivalent circuit, discussed in chapter 3, in order to be able to identify the physical elements of the FET which effect the high-frequency performance as indicated by f_T and f_{max}. Having established these relationships it is possible to discuss design strategies with the objective to improve the high-frequencies properties of the HEMTs, as it is done in section 5.3 of chapter 5.

CHAPTER 5

Present Research Status and Optimization Approaches

This chapter begins with a detailed literature research regarding AlGaN/GaN HEMTs and their RF-performance achieved in the past decade. In this way this chapter provides the following: First of all an overview of the present research status as known from literature is given. In this way this chapter sheds light onto the question what performance results can be expected when AlGaN/GaN HEMTs are optimized for high frequency applications. Secondly, by relating RF-performance results indicated by f_T and f_{max} to critical device dimension like the gate length L_G and the barrier thickness $t_{barrier}$ one can extract certain design rules and technology steps which are necessary during an RF-performance optimization of AlGaN/GaN HEMTs. Additionally optimization approaches based on basic HEMT-models are discussed. In a sum this chapter outlines what improvements are necessary taking the standard HEMT-technology of our institute as starting point.

5.1 Literature research

In order to get an overview of the present research status of AlGaN/GaN HEMTs and their RF-performance a detailed literature research was conducted. The results of this research are listed in table 5.1 which contains the most relevant design parameters extracted from literature. The basis of the table 5.1 was the table given in reference [118] which contains eighteen relevant entries found in literature up to the year 2007. This work extends the table given in reference [118] in both dimensions. In comparison to reference [118] additional information as f_{max} and the f_{max}/f_T ratio are given. Especially this work differs between as-measured and deembedded results as indicated by the deemb-column of table 5.1. In cases where a clear declaration of the S-parameters as extrinsic or deembedded could not be found a dash is placed. Also in cases where pieces of relevant information are not given in the specific publication a dash is set in table 5.1.

The latter analysis in this chapter focuses on RF-results based on extrinsic S-parameters. Although deembedding and parameter extraction are common methods to obtain physical properties like the saturation velocity v_{sat} of the intrinsic device [119, 120, 103] at the end of the day the device has to perform in a circuit environment and so the extrinsic parameters are the relevant ones. In order to keep a large data base all references in table 5.1 which do not explicitly declare their data as deembedded are considered to present extrinsic RF-data. However, it should be noted that such a proceeding might lead to wrong conclusions. For example, the publications [121] and [122] obviously base on the same data set. But only in the version [121] the RF-data are declared as deembedded while the version [122] relates the same RF-results to "on-wafer S-parameter measurements".

Additionally it should be emphasized that literature data often refer to the best specific research results. Reference [123] gives a good idea of how large the difference between best and average results might be: The average f_T is 40 GHz and 60 GHz and the best f_T is 55 GHz and 80 GHz for HEMTs with an L_G of 250 nm and 150 nm, respectively.

No.	f_T	L_G	t_b	L_G/t_b	$f_T \cdot L_G$	passiv.	d_{SD}	f_{max}	f_{max}/f_T	deemb.	ref.
1	181	30	11.3	2,7	5,4	SiN	2,0	186	1,03	yes	[88]
2	145	30	11.3	2,7	4,4	SiN	2,0	161	1,11	no	[88]
3	102	35	27.0	1,3	3,6	SiON	2,0	–	–	yes	[124]
4	110	35	27.0	1,3	3,9	SiON	1,5	–	–	yes	[124]
5	110	50	24.0	2,1	5,5	none	2,0	140	1,27	no	[125]
6	107	60	5.5	10,9	6,4	SIN	–	160	1,50	no	[126]
7	163	60	11.3	5,3	9,8	SiN	2,0	192	1,18	yes	[127]
8	152	60	13.2	4,5	9,1	SiN	2,0	173	1,14	yes	[128]
9	190	60	9.0	6,7	11,4	SiN	2,0	241	1,27	yes	[129]
10	70	60	–	–	4,2	none	1,1	300	4,29	yes	[130]
11	63	60	–	–	3,8	none	1,1	270	4,29	no	[130]
12	43	70	36.0	1,9	3,0	none	1,6	100	2,33	–	[131]
13	160	70	14.0	5,0	11,2	none	2,0	200	1,25	yes	[132]
14	81	70	30.0	2,3	5,7	SiN	1,5	190	2,35	–	[119]
15	86	75	19.5	3,8	6,5	SiN	2,0	122	1,42	no	[133]
16	102	85	20.0	4,3	8,7	SiN	–	–	–	–	[134]
17	81	90	30.0	3,0	7,3	SiN	1,5	187	2,31	no	[135]
18	163	90	–	–	14,7	SiN	–	185	1,13	–	[136]
19	153	100	13.0	7,7	15,3	none	–	230	1,50	–	[137]
20	90	100	13.0	7,7	9,0	SiN	–	–	–	–	[100]
21	85	100	11.5	8,7	8,5	SiN	2,1	210	2,47	–	[138, 139]
22	70	100	15.0	6,7	7,0	SiN	–	41	0,59	–	[140, 141]
23	83	100	19.5	5,1	8,3	SiN	1,0	123	1,48	no	[133]
24	48	100	18.0	5,6	4,8	none	7,0	75	1,56	yes	[142]
25	75	100	20.5	4,9	7,5	SiN	1,0	125	1,67	yes	[143]
26	101	120	30.0	4,0	12,1	none	2,0	155	1,53	yes	[144]
27	102	120	25.0	4,8	12,2	none	2,0	133	1,30	no	[121]
28	121	120	25.0	4,8	14,4	none	2,0	162	1,35	yes	[121, 122]
29	65	120	15.7	7,6	7,8	SiN	–	–	–	no	[120]
30	103	130	14.0	9,3	13,4	none	2,9	170	1,65	–	[145]
31	74	150	25.0	6,0	11,1	SiN	–	–	–	no	[146]
32	79	150	35.0	4,3	11,9	none	2,6	124	1,57	–	[147]
33	70	150	10.7	14,0	10,5	SiN	1,7	135	1,93	–	[148]
34	80	150	24.0	6,3	12,0	none	2,0	120	1,50	no	[123]
35	70	160	12.0	13,3	11,2	SiN	–	100	1,43	–	[9]
36	130	160	12.0	13,3	20,8	none	–	170	1,31	–	[9]
37	52	170	30.0	5,7	8,8	SiON	3,3	–	–	–	[149]
38	92	180	20.0	9,0	16,6	SiN	0,6	102	1,11	–	[150]
39	55	200	20.0	10,0	11,0	none	1,5	–	–	no	[151]
40	35	200	20.0	10,0	7,0	none	5,5	–	–	no	[151]
41	50	200	20.0	10,0	10,0	none	1,7	92	1,84	no	[152]
42	75	230	17.0	13,5	17,3	SiN	–	–	–	–	[153]
43	67	250	20.0	12,5	16,8	none	2,0	126	1,88	no	[154]
44	61	250	20.0	12,5	15,3	SiN	2,0	89	1,46	no	[154]
45	82	250	20.0	12,5	20,5	SiN	0,6	103	1,26	no	[155]
46	52	250	20.0	12,5	13,0	SiN	2,0	85	1,63	no	[155]
47	40	250	20.0	12,5	10,1	SiN	2,1	86	2,14	no	[156]
48	66	250	25.0	10,0	16,5	none	2,0	–	–	yes	[121]
49	55	250	24.0	10,4	13,8	none	2,0	100	1,82	no	[123]
50	23	250	27.5	9,1	5,8	SiON	5,0	70	3,04	–	[157]
51	37	290	29.0	10,0	10,7	none	–	–	–	no	[158]
52	37	300	16.0	18,8	11,1	SiN	4,8	55	1,49	no	[159]
53	43	300	25.0	12,0	12,8	SiN	–	–	–	no	[146]
54	25	500	–	–	12,7	none	–	40	1,59	–	[160]
55	21	500	15.0	33,3	10,5	SiN	–	34	1,62	–	[140, 141]
56	24	700	29.5	23,7	16,8	SIN	–	45	1,88	–	[161]
57	20	700	31.3	22,4	14,0	none	–	56	2,80	–	[162]
58	19	750	25.0	30,0	14,4	SiN	–	–	–	no	[146]
59	15	1000	33.0	30,3	15,0	none	3,0	24	1,60	–	[163]
60	14	1000	25.0	40.0	13,5	SiN	–	35	2,60	–	[164]
61	14	1300	20.0	65,0	18,3	none	–	–	–	no	[165]
62	14	1300	20.0	65,0	17,8	none	–	–	–	no	[166]
63	8	2000	30.0	66,7	15,2	none	6,0	24	3,11	–	[167]
64	13	2000	20.0	100,0	25,6	none	6,0	46	3,59	–	[167]
65	10	2000	10.0	200,0	19,2	none	6,0	38	3,94	–	[167]

Table 5.1: Parameters of AlGaN/GaN HEMTs obtained from literature research sorted by L_G.

5.2 Evaluation of literature research

5.2.1 First general observations

To get a first overview the values for f_T in table 5.1 are plotted as function of the gate length L_G and the barrier thickness $t_{barrier}$ as shown in figure 5.1 and figure 5.2, respectively. The triangular data points correspond to f_T values based on deembedded S-parameters. First of all figure 5.1 shows the well-known fact that high f_T is only achieved for short gate lengths, as expected from basic theory (cf. section 3.4). The highest values for f_T in figure 5.1 correspond to deembedded data. Hence the highest extrinsic f_T achieved for AlGaN/GaN HEMTs is 163 GHz so far. Also ultra short gate length devices with $L_G = 30$ nm do not exceed 145 GHz when the extrinsic data are considered. Down to a gate length of about 100 nm a clear improvement of f_T with a reduction of L_G is observed. For gate lengths less than 100 nm this trend saturates as depicted in figure 5.1. The deviation of the f_T-performance of these GaN HEMTs with very short gate length from an ideal $1/L_G$ behavior is attributed to increased effect of parasitic capacitance and resistances including the effective gate length [10].

A first design rule which can be extracted from figure 5.1 is that the L_G has to be reduced to 160 nm or less in order to surpass the 100 GHz border line. Considering that so far the standard HEMT technology was employed to fabricate gate lengths down to 300 nm [168, 74], the need for optimizing the gate lithography becomes apparent. A source drain spacing of 3 μm or less is another feature which all AlGaN/GaN HEMTs with $f_T >$ 100 GHz have in common according to table 5.1. If reference [145] is not considered, a source-drain spacing of 2 μm or less seems to be necessary to surpass the 100 GHz border line. The devices which exhibit the shortest source-drain spacings in table 5.1 also achieve excellent figures of merits. While the HEMT with $f_{max} = 300$ GHz described in [130] employs a source-drain spacing of 1.1 μm, the HEMT featuring an source-drain spacing of 0.6μm due to a self-aligned technology as described in reference [155] achieves a $f_T \cdot L_G$ product of more than 20 GHz·μm. Because the mask layout of standard HEMT technology employs source-drain spacings of greater or equal 3 μm, an optimization of the ohmic-contact-lithography is expected to be necessary, if a high RF-performance is desired.

Even more instructive than the simple f_T-L_G plot shown in figure 5.1 is the f_T-$t_{barrier}$-dependence in figure 5.2. Neglecting the f_T values based on deembedded data the highest f_T value for all AlGaN/GaN HEMTs with a barrier thicker than 15 nm is 110 GHz independent of the employed L_G. Thus, in order to achieve much higher f_T values than 100 GHz a thin barrier of a thickness less than 15 nm is required. This can be achieved in two different ways:

1. The barrier layer of the as-grown material is already thin.
2. The barrier layer has to be thinned locally by an adequate etching procedure, i.e. a local recess has to be performed.

In fact these two options mirror the two main approaches which pushed the RF-performance of AlGaN/GaN device to record values in last years. The first approach is predominantly applied by Higashiwaki et al. [129, 126, 127]. Palacios et al. were the first who followed the second way of a local recess most successfully in combination with other strategies [100, 162, 137]. However, both approaches come at cost of some technology effort. While the first approach requires an appropriate passivation scheme like Catalytic - Chemical Vapor Deposition (Cat-CVD) [129], the second one requires a low-damage recess-procedure

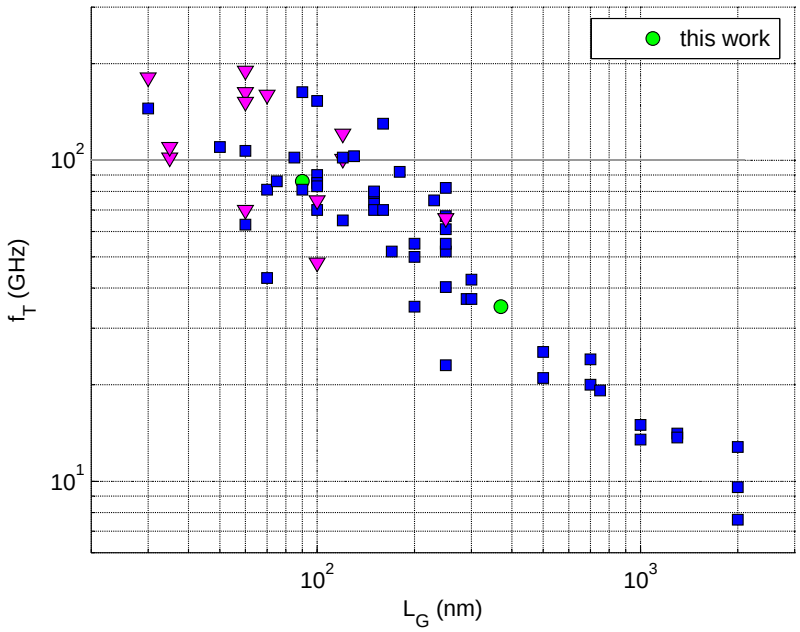

Figure 5.1: Current-gain cut-off frequencies f_T of AlGaN/GaN HEMTs as function of gate-length L_G obtained from literature. Triangular markers correspond to deembedded values.

[169], typically achieved with a Reactive Ion Etching (RIE) tool featuring a BCl_3 or a Cl_2 chlorine chemistry [170, 171]. The first approach of a thin as-grown barrier was not investigated in this work. The recessing approaches developed and investigated in this work are discussed in more detail in chapter 7. In a sum figure 5.2 shows the need for a thin or thinned barrier if AlGaN/GaN HEMTs with $f_T \gg 100\,\mathrm{GHz}$ are desired. Although this work focuses on AlGaN/GaN it should be mentioned at this point that InAlN structures with a barrier thickness below 10 nm are feasible and maybe part of future investigations which require a thin barrier.

5.2.2 Short-channel effects and gate-barrier aspect ratio

Short-channel effects are the sum of effects in which a device with short gate length deviates from its counterparts with a long gate length. One common short channel effect is that the $L_G \cdot f_T$ product will fall when L_G is reduced. The main origin of this effect is a loss of channel control in the case of short gate length. The gate electrode of long channel device is modeled by a parallel plate capacitor whose electrodes are the gate and the sheet electron charge, both separated by the thickness of the barrier layer $t_{barrier}$ (cf. section 3.2 in chapter 3). If the aspect ratio $L_G/t_{barrier}$ is large enough, fringing fields can be neglected. If the gate length is reduced so that the aspect ratio $L_G/t_{barrier}$ becomes small, the simple parallel plate capacitor model is not applicable anymore, because the actual gate capacitance looses its dominance above the fringing field capacitances and the other parasitic capacitance [172].

Accordingly it is instructive to study the dependence of the $L_G \cdot f_T$ product on the $L_G/t_{barrier}$ aspect ratio for various literature values. As shown in figure 5.3 there is a clear trend of a falling $L_G \cdot f_T$-product with a reduced $L_G/t_{barrier}$ aspect ratio. This trend

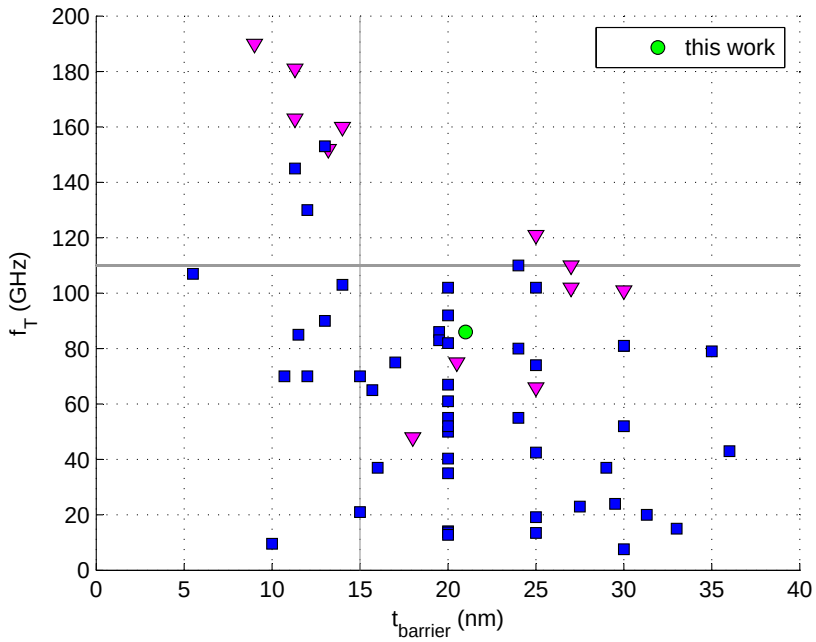

Figure 5.2: Current-gain cut-off frequencies f_T of AlGaN/GaN HEMTs as function of barrier thickness $t_{barrier}$ obtained from literature. Triangular markers correspond to deembedded values.

also holds for the deembedded S-parameters. Two data points in figure 5.3 are situated off the trend as they exhibit an $f_T \cdot L_G$ product greater than $20\,GHz \cdot \mu m$. In a sum there are only three entries in table 5.1 whose $f_T \cdot L_G$ product is greater than $20\,GHz \cdot \mu m$. Number 36 and 64 in table 5.1 refer to recessed device, what supports the need for a thin or thinned barrier layer. Number 45 of table 5.1 refers to one of the first self-aligned AlGaN/GaN HEMTs which exhibit a very short source-drain spacing of only $0.6\,\mu$m. In this sense entry 45 of table 5.1 indicates the importance of the source and drain access region on f_T.

One way to relate L_G and $t_{barrier}$ to the current-gain cut-off frequency f_T is discussed in reference [118]. As outlined in section 5.3 the f_T is in a good approximation equal to the intrinsic transit frequency f_τ. Additionally in section 3.4 f_τ is defined as $\frac{1}{2\pi\tau} = \frac{v_{sat}}{2\pi L_{G,eff}}$ with $L_{G,eff} = L_G + L_{GD}$. Thus, a good approximation for extrinsic f_T of a short channel HEMT is given by (5.1).

$$f_T = \frac{v_{eff}}{2\pi L_{eff}} = \frac{v_{eff}}{2\pi(L_G + L_{GD})} \tag{5.1}$$

where v_{sat} has been replaced by an effective saturation velocity v_{eff} to give a further degree of freedom to adopt the intrinsic device parameter to the measured f_T. Although expression (5.1) is already vague due to two effective parameters, its structure is useful to model and explain the observed non-linearity in figure 5.3. Assuming that L_{GD} is constant for various L_G a linear dependence of $(f_T \cdot t_{barrier})^{-1}$ on $L_G/t_{barrier}$ can be expected given by (5.2) [118].

$$\frac{1}{f_T \cdot t_{barrier}} = \frac{2\pi}{v_{eff}} \cdot \left(\frac{L_G}{t_{barrier}}\right) + \frac{2\pi}{v_{eff}} \cdot \frac{L_{GD}}{t_{barrier}} \tag{5.2}$$

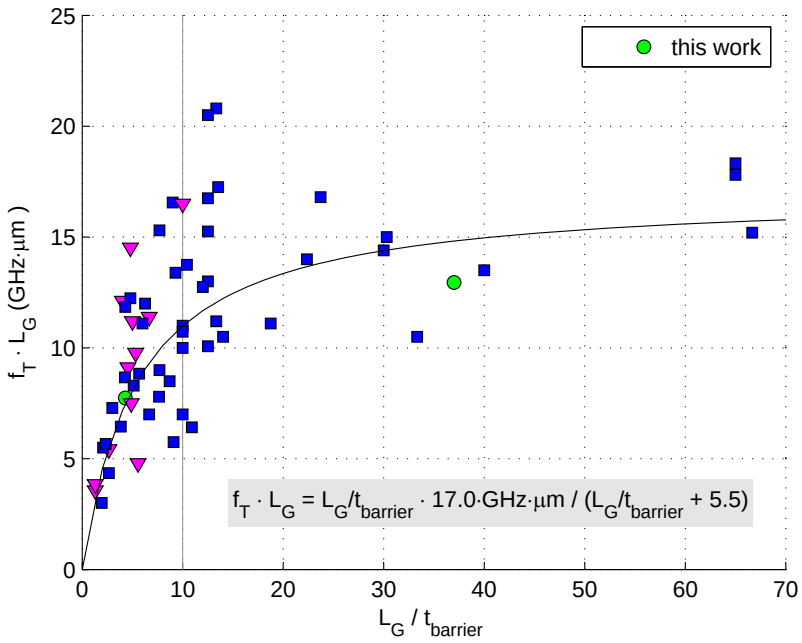

Figure 5.3: $f_T \cdot L_G$-product of AlGaN/GaN HEMTs as function of the $L_G/t_{barrier}$ aspect ratio obtained from literature. Triangular markers correspond to deembedded values.

Fig. 5.4 shows the dependence of $(f_T \cdot t_{barrier})^{-1}$ on $L_G/t_{barrier}$ for various AlGaN/GaN HEMTs. The results of a linear fit are given as inset in figure 5.4. For the linear fit only devices with L_G less than 300 nm and devices whose data base on extrinsic S-parameters are considered, so that the model by (5.1) is applicable. With the results obtained from this linear fit analytical expression for $f_T \cdot L_G$ dependence on $L_G/t_{barrier}$ can be derived and is given as inset in figure 5.3. Additionally a similar expression as given in [118] can be derived for f_T given by (5.3).

$$f_T = \frac{17.0\,\text{GHz} \cdot \mu\text{m}}{L_G + 5.5\,t_{barrier}} \tag{5.3}$$

Although the analysis given in [118] reveals sightly different values for (5.3) , i.e. 19.8 GHz instead of 17.0 GHz and a factor 5.1 instead of 5.5, this equation clearly emphasizes the importance of an adequate vertical device scaling when short gate lengths are employed. Equation (5.3) also shows that a simple $\frac{1}{L_G}$-scaling-rule is not applicable for deep-sub-micrometer AlGaN/GaN HEMTs what is also stated in reference [10]. Attention has to be paid on the effective gate $L_{G,eff}$ which is given by (5.4) according to the analysis in this chapter. The proportionality of $L_{G,eff}$ to $t_{barrier}$ is in accordance with the fundamentals as discussed in section 3.4.

$$L_{G,eff} = L_G + 5.6\,t_{barrier} \tag{5.4}$$

5.2.3 Maximum frequency of oscillation and current-gain cut-off frequency

In order to get an overview of the achievements regarding f_{max} and its dependence on f_T the f_{max}-values of various AlGaN/GaN HEMTs according to table 5.1 are plotted as

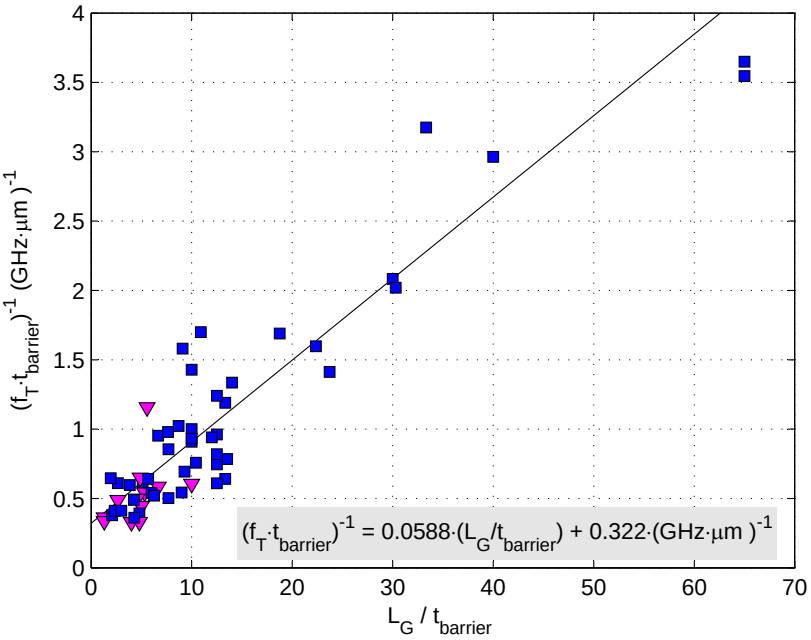

Figure 5.4: $(f_T \cdot t_{barrier})^{-1}$ as function of the $L_G/t_{barrier}$ aspect ratio for AlGaN/GaN HEMTs from literature research. Triangular markers correspond to deembedded values.

function of f_T in figure 5.5. According to references [130, 173, 72] f_{max} is approximately proportional to $\sqrt{f_T}$. Based on this theory a fitting described by (5.5) is also shown in figure 5.5. For the fitting only non-deembedded data points are considered. According to (5.9) the factor 75.4 GHz corresponds to an $R_g \cdot C_{gd}$ time constant of 0.176 ps.

$$f_{max} = 75.4\,\text{GHz} \cdot \sqrt{\frac{f_T/\text{GHz}}{8\pi}} \tag{5.5}$$

As depicted in figure 5.5 almost all data points follow the trend indicated by (5.5), no matter whether they base on deembedded S-parameters or not. Only a few devices deviate clearly from the trend. First of all the two data points at $f_T \approx 70$ GHz and $f_{max} \approx 300$ GHz given in [130] should be discussed. According to Chung et al. [130] the corresponding intrinsic gate-drain capacitance C_{gd} equals 42.6 fF/mm. A value of ≈ 0.120 pF/mm can be assumed for an AlGaAs/GaAs HEMT-technology [174] and it is also proposed in a road map for the harmonious reduction of gate length and parasitic elements in GaN HEMTs according to reference [10].

The value of 0.23 Ωmm for R_g in [130] is normalized to the gate width $W = 0.05$ mm. Consequently R_g has to be considered with $0.23/0.05\,\Omega$ and the gate-drain capacitance C_{gd} has to be considered with $0.0426 \cdot 0.05$ pF. In a sum an $R_g \cdot C_{dg}$ product of $0.23 \cdot 0.0426$ ps $\approx$ 0.010 ps is expected for the devices presented in reference [130]. The value of 0.010 ps is much smaller than the extracted value of 0.176 ps of (5.5) and it is seen as the explanation why a high f_{max}/f_T ratio can be achieved for the devices in [130].

The assumption that the $R_g \cdot C_{dg}$ product determines the f_{max}/f_T ratio is also supported by the second value which clearly deviates from the trend given by (5.5). The data point is situated at $(f_T, f_{max}) = (70,41)$ [140]. In reference [140] an upper bound of 8.5 Ω is assumed for R_g of a $L_G = 100$ nm-device. Because the devices described in [140, 141]

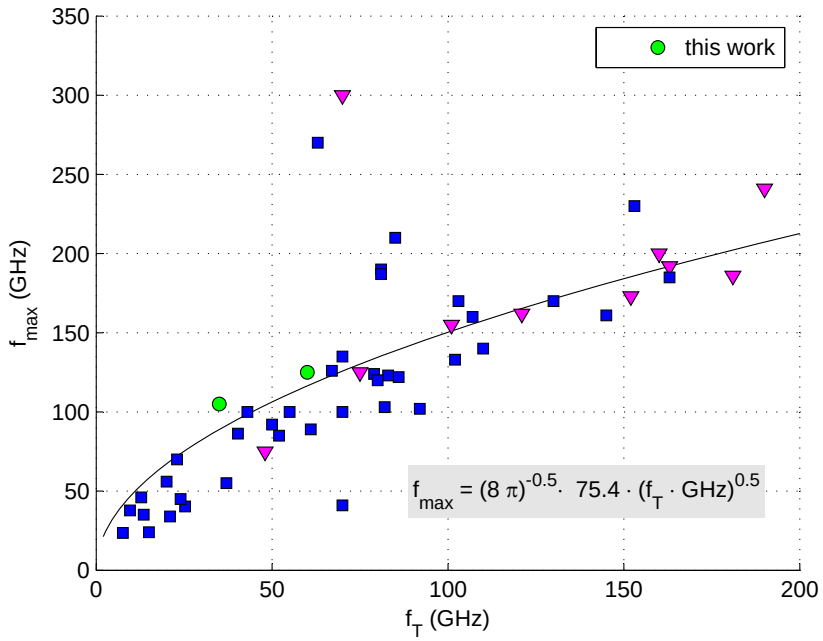

Figure 5.5: f_{max} as function of the f_T various AlGaN/GaN HEMTs from literature research. Triangular markers correspond to deembedded values.

exhibit a field-plate on the drain side of the gate, their C_{dg} can be expected to be much higher than 42.6 fF/mm. Hence the devices of [140] are expected to suffer from a high $R_g \cdot C_{dg}$ product resulting in a f_{max}/f_T-ratio smaller than 1. This observation is also in agreement with the result that the f_{max}/f_T-ratio decreases if the length of the field-plate is extended [175].

The challenge to keep a high f_{max}/f_T ratio while aiming at $f_T > 100$ GHz becomes obvious by inspecting figure 5.6. All devices with $f_T > 100$ GHz exhibit an f_{max}/f_T ratio less than two. The trend line in figure 5.6 was derived from (5.5) and its equation is printed as inset.

5.2.4 Optimization approaches of the semiconductor- and gate-stack

So far the optimization approaches discussed in this chapter focus mainly on geometry scaling. Of course the material stack of the HEMT may be optimized to achieved a better RF-performance. An ideal high-frequency semiconductor material features two major properties [176]:

- High carrier mobility and velocity.
- Tight carrier confinement/localization.

As discussed the HEMT as device structure naturally exhibits these two features to a certain degree. Especially the carrier confinement can be improved by employing a double-heterojunction structure instead of a single heterojunction. Two approaches regarding the material stack of AlGaN/GaN HEMTs led to an improved RF-performance as known from literature. These approaches are:

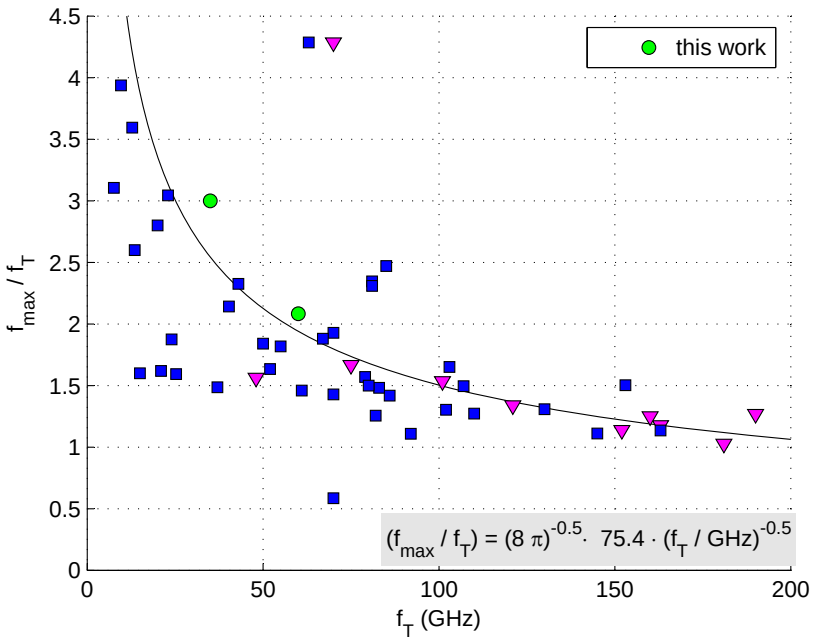

Figure 5.6: f_{max}/f_T as function of the f_T various AlGaN/GaN HEMTs from literature research. Triangular markers correspond to deembedded values.

- AlN spacer layer
- InGaN back barrier

The material stack of this work also features an AlN-spacer layer because it increases the carrier mobility and additionally improves the carrier-confinement [141] as discussed in chapter 2. The InGaN-back barrier was also found to increase the carrier-confinement hence resulting in a higher f_{max} in comparison to reference devices without back-barrier [137].

The gate metal stack in contact with the semiconductor bears room for improving the RF-properties of the AlGaN/GaN HEMT, too.Variations in the gate metal stack in comparison to the standard Ni/Au metalization were investigated. It was found out that for instance Pd/Au or Ir/Au metalization schemes result in a better small-signal and DC-performance than the conventional Ni/Au gate-stack [177]. Also the application of copper as an alternative gate metal was investigated [178] and led to a better RF-performance what is explained by a reduction of defects, potentially caused by formation Ga-Ni compounds at the Schottky-interface [179].

5.3 Optimization approaches based on basic HEMT theory

While section 5.2 gives an overview of the present research status in literature and outlines associated design rules and challenges, this section focuses basic equations for f_T and f_{max}. Based on these equations further design rules may be derived.

5.3.1 Current-gain cut-off frequency

If the small-signal equivalent circuit in figure 3.9 without parasitic Y-shell and the definition of the current-gain cut-off frequency as defined in section 4.6 is considered, a well-known approximation for the extrinsic f_T can be derived [180, 72, 181] given by (5.6).

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{dg})\cdot(1+(R_s+R_d)\cdot g_d)+C_{dg}\cdot g_m\cdot(R_s+R_d)} \tag{5.6}$$

$$\approx \frac{g_m}{2\pi(C_{gs}+C_{dg})} \tag{5.7}$$

From (5.7) it becomes clear that f_T is only a good approximation for the intrinsic transit frequency f_τ if the influence of the source and drain access resistance can be neglected. Generally this assumption is inadequate and (5.6) emphasizes the importance of R_s and R_d to the f_T of millimeter-wave HEMTs [180]. If (5.7) is considered for its own, the only scaling rule, which can be derived, is that L_G has to be reduced as much as possible in order to increase f_T. This is because f_T is $\sim {L_G}^{-2}$ for long-channel devices and $\sim {L_G}^{-1}$ for short-channel devices according to fundamentals outlined in section 3.4 [182]. But as discussed in section 5.2 horizontal scaling of a HEMT requires also an appropriate vertical scaling, i.e. a high aspect ratio design approach [174]. Equation (5.6) stresses the need for a high aspect ratio design, because it considers the drain-transconductance g_d in the denominator. In a sum two design rules for a given material system can be obtained from (5.6):

1. Reduce L_G meanwhile keeping a sufficiently high $L_G/t_{barrier}$ aspect ratio.
2. Reduce R_s and R_d as much as possible.

In fact these two design rules, i.e. a low contact resistance and a device structure that is less susceptible to short channel effects at $L_G < 120\,\text{nm}$, are the main technology advances accomplished by leading institutes in this field which enabled extending the frequency range of GaN MMIC technology beyond 50 GHz [183].

Indeed, GaN HEMTs which show the best RF-performance today (cf. table 5.1) exhibit a contact resistance R_c of $0.15\,\Omega\cdot\text{mm}$ [130] to $0.3\,\Omega\cdot\text{mm}$ [129]. The corresponding sheet resistances $R_\square$ of the semiconductor access regions are $356\,\Omega/\square$ [130] and $200\,\Omega/\square$ [129], respectively. Contact resistances of $0.12\,\Omega\cdot\text{mm}$ for AlGaN/GaN heterostructures are reported in literature [184]. Recently an alloyed ohmic contact resistance of $0.1\,\Omega\cdot\text{mm}$ was achieved for GaN HEMT fabricated on N-faced material [185].

The minimum achievable contact resistance R_c for a given material system is a fundamental limit, because it is the lowest value which can be achieved for R_s and R_d according to section 3.5 [174]. The need to reduce the total source and drain resistance R_s and R_d below $0.2\,\Omega\cdot\text{mm}$ is seen due to their significant role in deep sub-micron AlGaN/GaN HEMTs [10].

What a sufficiently high $L_G/t_{barrier}$ aspect ratio is, depends on the chosen material system. In the GaAs system a ratio of about 5 is considered as sufficient as a rule of thumb. For AlGaN/GaN HEMTs short-channel effect are expected for $L_G/t_{barrier} < 15$ and the aspect ratio should be as high as 6 at least [118]. The fundamental limit of these empirical scaling rules is the minimum barrier thickness $t_{barrier}$ required for 2DEG formation besides potential gate leakage problems of very thin barriers. For high performance short-channel AlGaN/GaN HEMTs the output conductance g_d as an indicator for short-channel

effects should achieve a value of about 10 mS/mm [130, 140] and should be at least below 100 mS/mm for future AlGaN/GaN HEMTs [10].

A design rule for the gate width W cannot be obtained from (5.6) because f_T is independent of W, if reactive elements of the parasitic Y- and Z-shell in figure 3.10 are neglected.

5.3.2 Maximum frequency of oscillation

As stated in references [130, 173, 72] the maximum frequency of oscillation f_{max} depends on f_T and other elements of the small-signal equivalent circuit (cf. figure 3.9) according to (5.8).

$$f_{max} \approx \frac{f_T}{2\sqrt{(R_i + R_s + R_g) \cdot g_d + 2\pi f_T R_g C_{gd}}} \tag{5.8}$$

$$\approx \sqrt{\frac{f_T}{8\pi R_g C_{gd}}} \qquad , (R_i + R_s + R_g) \ll 1/g_d \tag{5.9}$$

As for f_T it is important to achieve a low intrinsic drain transconductance g_d if a high f_{max} is desired. As discussed in the previous section a low g_d can be achieved by a high $L_G/t_{barrier}$ aspect ratio as it ensures channel control free of interference by drain potential. If a low g_d is achieved the approximation (5.9) holds. As discussed above the product $R_g \cdot C_{gd}$ should be reduced. A common method to reduce R_g meanwhile keeping a short L_G is the application of so-called T-gate or mushroom-gates. The foot of the T-gate ensures a short L_G. The head of the T-gate lowers R_g due to its relatively large cross-section. Interestingly R_g and C_{dg} are $\sim W$ [174, 72] and hence f_{max} is approximately proportional to $1/W$ [186], if one gate finger is considered. The AlGaN/GaN HEMT which exhibits the highest f_{max} value up to date has a gate width of only $2 \times 25\,\mu$m [130]. However, a constant improvement of f_{max} with reduced W can not be expected because constant, non-zero parasitic capacitors and inductors in the environment of the device. Especially it has to consider that the charging time associated with the pads τ_{pad}, given by (5.10), depends inversely on the extrinsic g_m, which will reduce linearly with W [187].

$$\tau_{pad} = \frac{C_{pad}}{g_m} \tag{5.10}$$

Another approach to reduce R_g while keeping W constant is a multi-gate-finger layout with N gate fingers because $R_g \sim N^{-1}$. However, a multi-gate-finger approach will add additional parasitic elements due to the required via-hole- or air-bridge technology. In a sum three additional design rules can be obtained from (5.8) in order to increase f_{max}:

1. Increase f_T
2. Reduce Rg
3. Reduce C_{dg}

5.4 Optimization approaches

On basis of the previous discussion in this chapter the following optimization approaches for a improved RF-performance could be identified:

Reduction of gate access resistance R_g: For the reduction of R_g two T-gate processes are developed and investigated regarding their advantages and disadvantages. Details of the T-gate technology are described in chapter 6.

Reduction of gate length L_G: Because of the fundamental impact of L_G on f_T and f_{max} it is instructive to investigate gates lengths smaller than the standard 300 nm of our institute, what implies an optimization of the gate-lithography. Especially gate lengths of less than 160 nm are of interest because the f_T values of devices with such short gate lengths bear the potential to surpass the 100 GHz border line.

Reduction of source and drain access resistance R_s and R_d: A reduction of R_s and R_d is achieved by a spatial shorting of the source-drain access region. The source-drain access region was reduced from a minimum of 3 μm of the standard HEMT technology to about 1 μm by the application of electron-beam (e-beam) lithography instead of optical lithography. An optimization of the ohmic contacts of the standard HEMT technology would have been important due to two major aspects: The contact resistance of the standard HEMT technology is $\approx 0.6\,\Omega$·mm which leaves room for improvement in comparison to state of the art values of $0.2\,\Omega$·mm [188] for contact resistances. Additionally the ohmic contacts of the standard HEMT technology have a modest line-edge definition and morphology what make them inadequate as e-beam markers and impose a limit for the reduction of the source and drain access region. However, a systematic improvement of the contact resistance regarding the afore mentioned criteria is a challenging task, because the optimum of R_c is expected to depend strongly on the specific epitaxial material [189] and a simultaneous optimization of the electric properties, the morphology and the line edge definition cause additional effort [190].

Maintaining an adequate $L_G/t_{barrier}$ aspect ratio: In order to maintain a sufficiently high gate-barrier aspect ratio and hence maintain a low g_d, two recess approaches are investigated and developed in this work. The two approaches are compared to each other and discussed in more detail in chapter 7.

5.5 Estimation of RF-performance development

In this chapter design strategies for the improvement of RF-performance are outlined and these strategies base on an analysis of an detail literature research and analytical expression for f_T and f_{max}. In this section the impact of the proposed optimization approaches on the RF-performance are investigated quantitatively. As a starting point for this quantitative analysis RF-data are chosen, which describe one of the best of a AlGaN/GaN HEMT regarding its RF-figures of merit as known from literature [130]. According to reference [130] the values of the small signal equivalent circuit, describing the behavior of this AlGaN/GaN HEMT at the bias point $V_{GS} = -2.2$V and $V_{DS} = 16$ V, are as follows: $W = 0.050$ mm, $g_m = 369.8$ mS/mm, $R_s = 0.42\,\Omega$·mm, $R_d = 0.57\,\Omega$·mm, $R_g = 0.23\,\Omega$·mm, $R_i = 0.045\,\Omega$·mm, $1/g_d = 95.7\Omega$·mm, $C_{gs} = 740.8$ fF/mm, $C_{gd} = 42.6$ fF/mm [130].

With these parameters the S-parameters are calculated on the basis of the small-signal Y-parameters according to the fundamentals presented in chapter 3 and chapter 4. Elements of the small-signal equivalent circuit, depicted in figure 3.9, which are not given in reference [130] are assumed to be zero in the analysis presented in this section. Also C_{ds} is assumed to be zero. According to other studies C_{ds} might achieve negative values [39] or maybe accounted for with a value of $C_{gd} = 270\,\mathrm{fF/mm}$ [1].

Figure 5.7 shows the RF-gains which were calculated on the basis of the values for the small-signal equivalent circuit elements given in reference [130]. The gains plotted in figure 5.7 are in very good agreement with reference [130], because f_T and f_{max} are predicted to be 73 GHz and 288 GHz as it is in the original work. The measured f_T and f_{max} are 70 GHz and 300 GHz in reference [130]. Hence the assumption of zero C_{gd} is justified for this model. Starting from the RF-performance shown in figure 5.7 each considered element of the small-signal equivalent circuit is increased or decreased two times in order to study their influence on the RF-performance.

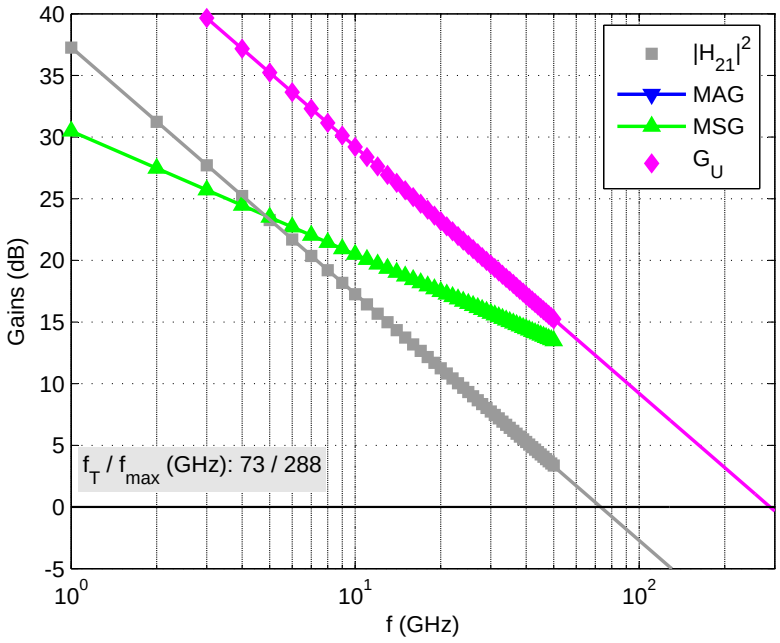

Figure 5.7: RF-gains calculated on the basis of the values for the small-signal equivalent circuit elements given in reference [130].

During the variation of a particular element the remaining elements are held constant and the impact on f_T and f_{max} is observed. The plot of the RF-gains for each variation is given in appendix A.5. Table 5.2 lists the results for each of the eight variations of elements. In contrast to reference [130] it is assumed that R_g is proportional to W [101, 93, 72, 97]. By assuming R_g proportional to W the small-signal equivalent circuit becomes dependent on W what allows to study the impact of the gate width W on the RF-performance additionally. Consequently the initial value of R_g has to be $0.023\,\Omega\cdot\mathrm{mm}/(0.05\,\mathrm{mm})^2 = 92\,\Omega/\mathrm{mm}$ in the altered model. The results for varying gate width W are also listed in table 5.2.

A variation of R_g does not influence f_T but it has a strong impact on f_{max} as it is expected from the discussion in section 5.2. Both access resistances R_s and R_d effect f_T modestly but show a clear impact on f_{max}. Considering that an improvement of the ohmic contact

R_g (Ω/mm)	f_T / f_{max} (GHz)	R_s ($\Omega \cdot mm$)	f_T / f_{max} (GHz)	R_d ($\Omega \cdot mm$)	f_T / f_{max} (GHz)
92	73 / 288	0.42	73 / 288	0.56	73 / 288
368	73 / 191	0.80	72 / 256	1.20	71 / 279
1472	73 / 106	1.20	71 / 232	1.80	70 / 271
g_d (mS/mm)	f_T / f_{max} (GHz)	C_{gd} (pF/mm)	f_T / f_{max} (GHz)	C_{gs} (pF/mm)	f_T / f_{max} (GHz)
10.5	73 / 288	0.043	73 / 288	0.741	73 / 288
50.0	70 / 175	0.200	58 / 154	1.100	50 / 208
100.0	61 / 107	0.400	46 / 94	1.400	40 / 169
g_m (mS/mm)	f_T / f_{max} (GHz)	R_i ($\Omega \cdot mm$)	f_T / f_{max} (GHz)	W (mm)	f_T / f_{max} (GHz)
369.8	73 / 288	0.046	73 / 288	0.05	73 / 288
300.0	59 / 243	0.800	73 / 261	0.10	73 / 191
150.0	30 / 132	1.200	73 / 239	0.20	73 / 106

Table 5.2: Influence of various parameter of the small-signal equivalent circuit on the RF-performance.

technology and/or a reduction of the sheet resistance always effects both access resistances simultaneously the relevance of these approaches for the RF-performance becomes obvious. The drain transconductance g_d is related to the aspect ration design, i.e. the design of the $L_G/t_{barrier}$ ratio, because g_d is expected to increase if the $L_G/t_{barrier}$ ratio is lowered due to a loss of channel control. While an increase in g_d has a modest impact on f_T, its influence on f_{max} is very pronounced. The strong influence of g_d on f_{max} emphasizes the need for a recessing procedure, if material with a thin as-grown barrier is not available.

Table 5.2 also shows the influence of the feedback capacitance C_{gd} on f_T and f_{max}. An increase of C_{gd} causes a reduction in f_T and f_{max} while the f_{max}/f_T ratio also decreases from about four to about a factor of two in the particular scenario. If C_{gs} is increased, f_T is reduced but in contrast to an increase in C_{gd} the f_{max}/f_T ratio is maintained at a value of about four. A reduction of g_m has a similar effect, what is plausible because both elements are related to the intrinsic transit frequency f_τ as outlined in section 3.4. The channel resistance R_i does not effect f_T as it is the case for R_g. However, an increase in R_i causes f_{max} to fall. Finally the f_T and f_{max} values for an increased gate width W are listed in table 5.2. Because with an increase in W both R_g and C_{gd} increase the values of f_{max} clearly decrease as a consequence. As expected from (5.6) a variation of W does not influence f_T.

Scaling of the gate width W is a common way to modify the DC- and RF-properties of a FET. The theoretical impact of W on the DC-characteristic is clear from chapter 3. The drain saturation current $I_{D,sat}$ and the mutual transconductance under saturation $g_{m,sat}$ is proportional to the gate width W, for short channel and for long channel devices. Because of this proportionality the drain current and the transconductance of a FET are typically given as quantities per unit gate width and hence typically units are A/m and S/m, respectively. If parasitics like pad capacitances and inductances are neglected no impact of W on f_T is expected. If the number of gate fingers is constant the maximum frequency of oscillation f_{max} is approximately proportional to $1/W$. But reducing W excessively in order to achieve record f_{max} is meaningless for the following reasons:

Firstly, the transistor itself will be dominated by extrinsic parasitics if its dimensions become small in comparison to contact pads. This is especially true for today's highly integrated digital CMOS circuits where the interconnect capacitances dominate the FET input capacitances by far and they are a major performance limiting factor making low-k dielectrics like Hydrogen Silses-Quioxane (HSQ) necessary in the back-end CMOS process (cf. section 6.2).

Secondly, the maximum linear RF-output power $P_{out,RF}$ for a FET operating as class A amplifier is given by (5.11) [39, 74], with BV_{on} denoting the breakdown voltage of the on-state device.

$$P_{out,RF} = \frac{I_{D,sat} \cdot (BV_{on} - V_{DS,sat})}{8} \tag{5.11}$$

Hence $P_{out,RF}$ is proportional to W. Because AlGaN/GaN HEMTs are generally considered for high-frequency and high-power applications the gate width W has to be dimensioned carefully in light of the $P_{out,RF}$-f_{max} trade-off situation. Additionally it has to be considered that W cannot be increased arbitrarily in order to increase $P_{out,RF}$ because the device dimensions have to small in comparison to operating frequency, i.e. the device dimensions have to be clearly less than $\lambda/4$, where λ denotes the wavelength of the guided wave [110]. Consequently at X-band (8.2 GHz - 12.4 GHz) [1] the width of a single gate finger is typical 150 μm, at Ka-band (26.5 GHz - 40.0 GHz) 75 μm and W-band (75 GHz - 110.0 GHz) about 40 μm [191].

5.6 Summary

This chapter provides a broad overview over the present research status of AlGaN/GaN HEMTs and their RF-capabilities. By a detailed evaluation of a literature data base certain trends and design strategies are revealed which lead to an increase of the devices' RF-performance. These design strategies are augmented and supported by an inspection of analytical expressions for f_T and f_{max}. On the basis of fundamental device and RF-theory the influence of the main small-signal equivalent circuit elements on the RF-performance is studied in detail. In this way the observations made by the evaluation of the literature data base are augmented by numerical estimates of the RF-performance.

CHAPTER 6

T-gate Processes

This chapter describes the investigated T-gate technologies of this work. At the beginning of this chapter an overview of various T-gate processes found in literature is given and their fundamental ideas and their advantages and disadvantages are discussed briefly.

6.1 Approaches of T-gate fabrication

There are several different approaches to fabricate a gate whose cross section has the shape of a "T", i.e. a so-called T-gate. Typical dimensions of a T-gate are as follows: Common gate foot lengths vary from about 200 nm [192] down to 25 nm [193]. The lateral gate head dimensions might vary from 300 nm to 900 nm [194] while the height of the gate head is determined by the thickness of the evaporated gate metal, e.g. about 400 nm. To give an overview various approaches for the fabrication of a T-gate are listed in table 6.1. The listed T-gate process are sketched in cut-down versions in figure 6.1. Whether one of the listed processes can be incorporated into a certain HEMT-technology or not, depends on the specific material system and the availability of required resources and resists. Moreover the aspect of reproducibility of a certain T-gate process is of major importance when the application in a circuit environment is considered. A further important aspect is the scalability of a T-gate-process, that is the minimum gate length L_G which can be achieved. Additionally it might be desirable to modify the dimensions of the gate head independently from the gate-foot of the T-gate. With this degree of freedom gates with a special field plate extension may be designed [195]. Field-plates are used to alter the electric field at the drain side of the gate in order to increase the breakdown voltage of the device and hence allow for higher operating voltages. The aspect of an increase breakdown voltage is especially interesting in the case of AlGaN/GaN HEMTs as they are generally considered as high-power and high-frequency devices [196, 197, 175].

The first major distinction between the various T-gate processes of table 6.1 to be made is the one regarding the number of required process steps. The main advantage of a one-step T-gate process is the minimum processing effort. However, in a one-step T-gate process it is generally challenging to define a thin foot pattern due to the combined definition of gate head and gate foot.

One-step processes may be divided into processes employing e-beam lithography and processes employing optical UV-lithography. One-step e-beam processes achieve the T-shape by a multi-layer resist stack with resists of different e-beam dose sensitivity. The bottom layer of the stack defining the gate foot exhibits a resist with a lower sensitivity than the top layer, which defines the gate head. If the multilayer resist stack is built of resists with chemically similar solvents, like for instance PMMA and MMA, the problem of intermixing may occur during resist spinning. To avoid this mixing of layers the incorporation of organic or non-organic interlayer may be applied [201].

No.	layer and resists	steps	lithography	description and basic idea	ref.
1	tri-layer Poly-Methyl-MethAcrylat (PMMA)/ Methyl-MethAcrylat (MMA)/ PMMA	1	e-beam	different sensitivity of PMMA and MMA	[198]
2	bi-layer ZEP/ UV113	1	e-beam	chemical different and difference sensitivity	[199]
3	HSQ and tri-layer ZEP/ Poly-di-Methyl-Glutar-Imide (PMGI) /ZEP	2	e-beam	thin HSQ fin, defining foot size, selectively removed	[200]
4	tri-layer PMMA/ Lift-Off Resist (LOR)/ UV-III	1	e-beam	Aluminum interlayer is replaced by LOR-A	[201]
5	mono-layer PMMA	1	e-beam, ion-beam	different penetration depth of ions vs. electrons	[202]
6	mono-layer AZ1350	1	optical Ultra Violet (UV)	angle evaporation of sacrificial metal layer and subsequent selective wet-etch	[192]
7	Si_3N_4/PMMA and bi-layer MMA/ PMMA	2	e-beam	Si_3N_4 passivation as transfer layer for gate foot definition	[203]
8	SiO_2 and tri-layer ZEP/ PMGI/ ZEP	2	e-beam	SiO_2 is used as transfer layer for gate foot lengths down to 25 nm	[193]
9	PMGI/ AZ5206	2	e-beam, optical UV	good lift-off with image reversal resist AZ5206	[204]
10	Si_3N_4/ZEP and tri-layer PMMA/ LOR/ UV-III	2	e-beam	mechanical stable sub-25nm T-gate with elevated bulk of the gate head	[194]
11	mono-layer PMMA	1	nano-imprint	steps with T-gate structure are pressed into the PMMA coating of target wafer	[205]
12	bi-layer PMMA/ MAA	1	e-beam	PMMA bottom layer is thermally re-flowed to reduce gate foot length down to 30 nm	[206]
13	bi-layer PMMA/ AZ-PF-514	2	e-beam	Chemical difference between PMMA and AZPF514 allows for selective development	[207]
14	mono-layer photo resist	1	optical UV	selective wet-chemical under-etch of Au gate head	[208]
15	bi-layer PMMA/ PFI	2	e-beam	gate foot length reduction due to PMMA-PFI intermixing layer	[209]
16	HSQ and tri-layer PMMA/ MMA/ PMMA	2	e-beam	HSQ for gate foot definition	[210]
17	Si_3N_4/Ge/ZEP and mono-layer MMA	2	e-beam	reduced parasitic capacitance due to Ge sacrificial layer	[136, 148]
18	mono-layer photo resist	1	optical UV	selective dry-chemical under-etch of Au gate head	[211]
19	mono-layer photo resist	2	optical UV	thinned photoresist reversed by Al-metal mask	[212]

Table 6.1: Various T-gate processes from literature. The column *steps* denotes the number of lithographies which has to be conducted.

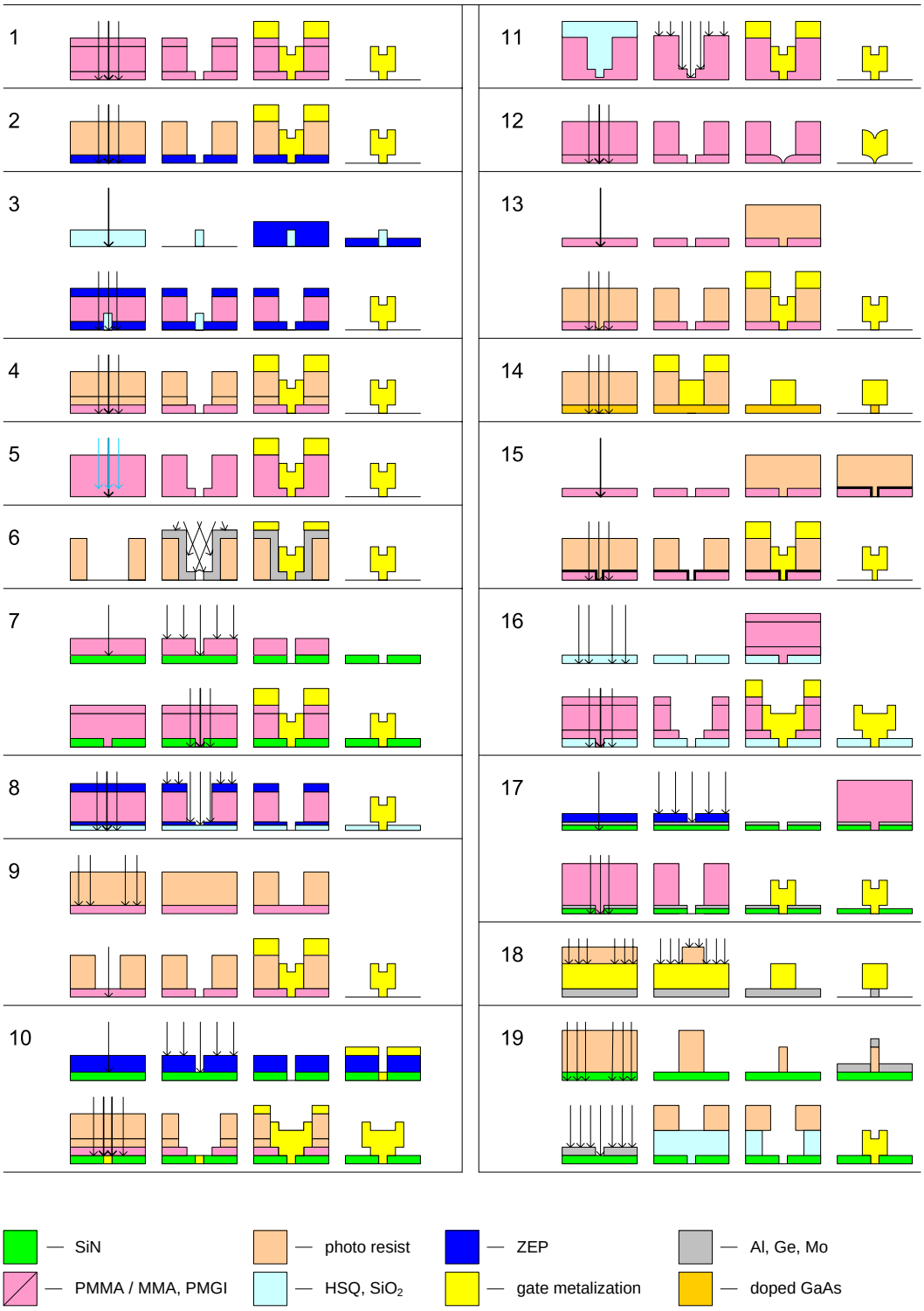

Figure 6.1: Schematic illustration of various T-gate processes.

One-step optical processes typically require only a mono-layer of photo resist. In these processes the gate head is defined by optical lithography. In the one-step optical processes

the T-shape is achieved by a selective wet- or dry-etch of metal or semiconductor material under the gate head, whose remainder builds the gate foot [211, 208]. Other one-step T-gate processes which require only a mono layer of resist are the gate definition by Nano-imprint [205] and a combined e-beam/ion-beam process, which achieves the T-structure due to different penetration depth of electrons and ions, respectively [202].

The class of two-step T-gate processes contains all image reversal processes. In the case of image reversal processes a positive pattern of the gate foot is defined what is typically achieved with a negative resist like HSQ [200]. The positive pattern is finally replaced by the actual gate metalization [200] or it is used to structure a negative metal mask [212]. Of course, all T-gate processes, which combine optical UV and e-beam lithography, belong to the class of two-step e-beam processes while their advantages in comparison to the other approaches seem to be limited to a good lift-off achieved by a negative photo resist [204].

Other two-step T-gate processes are often step-by-step versions of similar one-step processes, e.g. [194, 136, 148]. The separate definition of gate foot and gate head increase the degree of freedom in the device fabrication process which allows for a careful reduction of associated parasitics [194, 136, 148] or field-plate engineering [195]. The major disadvantage of two-step T-gate processes is that a very high overlay accuracy of the gate head lithography with respect to the gate foot lithography has to be ensured.

In this work two different approaches for T-gate processes were developed and investigated. In the first approach an HSQ-based T-gate process, which is similar to the process described in reference [210], was developed. For the AlGaN/GaN material system this approach is new. Details of this HSQ-based process are outlined in section 6.2. The second approach of this work is similar to the one described in [136] while a metal mask was used for gate foot definition instead of the costly ZEP resist and the developed process of this work does not feature a spacer layer. A detailed documentation of the second T-gate process developed in this work is given in section 6.3. If MMA is available, the common tri-layer PMMA/ MMA/ PMMA is also an alternative [130].

6.2 HSQ-based T-gate process for AlGaN/GaN HEMTs

In this section the HSQ-based T-gate process for AlGaN HEMTs is outlined. In the beginning this approach is briefly motivated and particularities of the HSQ resist are summed up. Finally the main steps of the process are described.

6.2.1 Motivation for an HSQ-based T-gate process

One challenge in the fabrication of T-gates with a sub-100-nm is the mechanical stability [104, 210]. Therefore in many T-gate process the gate foot is fixed in a dielectric layer [193]. The major draw back of placing the gate foot into a dielectric is the increase of parasitic capacitances. This is especially true for Si_3N_4 as dielectric layer because of its relatively high dielectric constant ϵ_{r,Si_3N_4} of about 7.5 [195]. HSQ is well-known as low-k dielectric. Due to its porous structure HSQ features a dielectric constant $\epsilon_{r,HSQ}$ of as low as 2.2 [213]. In this way incorporation of HSQ into a T-gate process gives the mechanical stability on the one hand and on the other hand it allows to keep the parasitic capacitance low without employing elaborated multi-layer resist techniques [194] or an additional sacrificial layer [148]. Another challenge involved with using conventional dielectric layers is the pattern

transfer from a positive resist like PMMA or ZEP into the dielectric layer. This pattern transfer is typically achieved by an anisotropic dry-etch in a RIE tool. However, etch processes might cause damage to the semiconductor and degraded device performance. In contrary the application of HSQ allows defining the gate foot by e-beam exposure and development without the need to apply potentially destructive dry-etch processes.

6.2.2 HSQ particularities

Originally HSQ was used as spin-on dielectric or so-called flowable oxide in the semiconductor technology [214]. HSQ-molecules are typically solved in Methyl Iso-Butyl Ketone (MIBK). Tempering steps at elevated temperature of at least greater than 280°C [215] starts to turn the HSQ-molecules into amorphous silicon oxide. A curing temperature of $350 - 400$°C is sufficient to make HSQ resistant against the developer, typically a Tetra-Methyl Ammonium Hydroxide (TMAH) based solution [214]. The required reaction energy can also be applied by e-beam exposure what allows to use HSQ as e-beam negative resist since 1998 in addition to its conventional use as flowable oxide. Feature sizes achieved with e-beam lithography are as small as 6 nm [216] enabled by the small HSQ-molecular-size [210]. Due to its sensitivity to H_2O the exposure time to ambient humidity prior spinning should be as short as possible [217]. A typical e-beam area dose is about $250 - 300\,\mu C/cm^2$ [215, 214]. For single line structures the required dose can reach up to $9.000\,\mu C/cm^2$ [215, 217].

6.2.3 T-gate prototypes on silicon

T-gate prototypes on silicon were processed prior to the development of an HSQ-based T-gate process for the AlGaN/GaN material system similar to process 16 depicted in figure 6.1. It started with ohmic metalization without annealing to define e-beam marker. Subsequently the gate foot was defined with HSQ. The gate head was structured in a final e-beam lithography with PMMA as resist. The first problem solved was the way how to spin HSQ. Prior work at our institute [215] estimated the minimum sample size applicable for HSQ-spinning of about $2 \times 2\,cm^2$. The reason of this minimum sample size is that HSQ is very sensitive to edges and the rim of a sample during spinning. Typically HSQ forms large sidewall extending far toward the center of a sample. For a $12 \times 12\,mm^2$ sample geometry the ratio between sidewall area and area where HSQ is homogeneously spun is about equal. Thus conventional spinning procedures as used for wafers are not applicable for quadratic samples of minor size.

However, a solution how to cover samples of a size $12 \times 12\,mm^2$ very homogeneously with HSQ was found in this work. The sidewall formation was not found to improve much with a different spinning speed, varied from 2000 rpm to 6000 rpm. But by using a wafer-chuck covered with a lid, also referred to as Gyrset, it is possible to spin the resist in a solvent ambient. The solvent ambient results in a much thinner HSQ film, e.g. ~ 50 nm instead of ~ 200 nm at 4000 rpm, but it also results in a clear reduction of the side wall formation. With this result HSQ could be used for the AlGaN/GaN samples of $12 \times 12\,mm^2$ in this work.

Figure 6.2 shows a ~ 100 nm wide gap in a 50 nm HSQ-oxide film on Si. Gap widths of down to 60 nm where achieved in this work with a 500 pA beam, 10 nm beam-step-size and a dose of $420\,\mu C/cm^2$. In principle gap width of ~ 30 nm should be possible [210]. In order

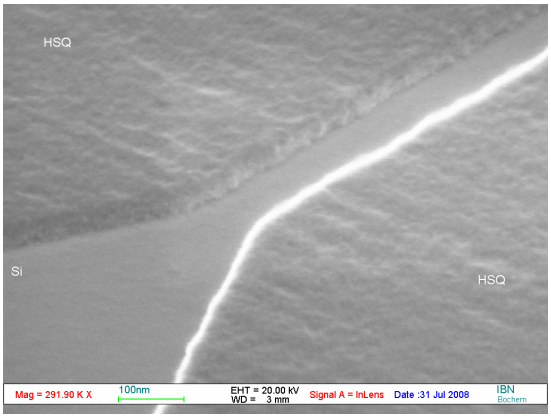

Figure 6.2: HSQ pattern on Si wafer.

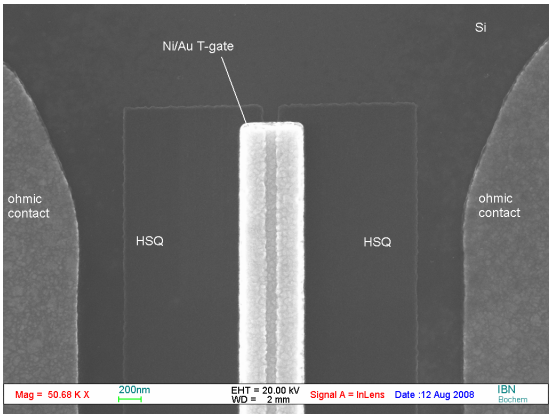

Figure 6.3: Top view of a T-gate prototype on Si wafer.

to complete the preliminary studies a T-gate prototype was built as depicted in figure 6.3. The good overlay accuracy between the HSQ gap, which defines the gate foot, and the gate head could be achieved by an automatic marker search instead of a manual marker search during e-beam writing. However, a basic requirement for an automatic marker search are e-beam markers with a good line edge definition and smooth morphology which are not given in the standard HEMT technology [74]. Consequently, the development of a high quality e-beam marker was necessary in this work in order to enable two-step T-gate processes.

6.2.4 Introduction of a marker layer

In general, high quality e-beam markers and the related lithography should exhibit the following features:

1. Straight line-edge definition and smooth morphology of the markers.
2. High marker contrast (positive or negative) in comparison to the background material.
3. Good mechanical and chemical stability of the markers.

The first item is necessary to ensure the seamless recognition of the e-beam marker and its precise localization. In the same sense a high contrast is required, especially if markers are covered by e.g. passivation schemes during the process flow. A complete set of markers is necessary to allow the e-beam writer to proceed according to its standard algorithms. Although a single marker loss is compensated easily by the e-beam standard routines, the absence of several markers reduces the achievable accuracy and eventually causes the writing process to stop. Consequently the e-beam markers must also be mechanical and chemical stable, so that there is no loss of them during processing.

It may be thought of three approaches to obtain high quality e-beam markers. The first approach is to introduce the e-beam marker with the ohmic contact lithography as it is done in the standard HEMT technology. This way is appropriate, if the ohmic contacts exhibit a good line edge definition and morphology besides good electrical properties. However, there might be a trade-off between the morphology and the electrical characteristics of an ohmic contact scheme [218]. Generally, if the e-beam marker should be part of the ohmic

layer, the ohmic metalization scheme has to contain elements of high atomic number like e.g. Au or Pt. Elements of high atomic number are required because the atomic number of Al and Ti, which are typically included in ohmic contacts [219, 189, 184, 130], are too low to yield efficient backscattered electron emission for the alignment marks resulting in a poor contrast using e-beam lithography [220].

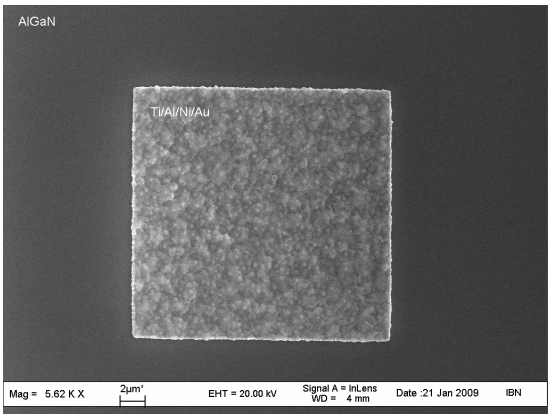

Figure 6.4: E-beam marker of ohmic contact layer after RTP annealing.

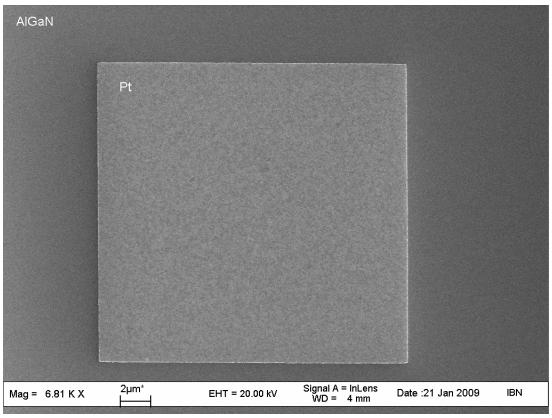

Figure 6.5: Introduced Pt-marker after RTP annealing.

The second approach toward high quality e-beam markers is the introduction of a separate marker layer which was pursued in this work. By the introduction of a separate marker layer the marker can be optimized without consideration regarding the electric properties as it would be the case if the markers were part of the ohmic layer. Figure 6.4 shows an e-beam marker made of ohmic metalization after Rapid Thermal Process (RTP) anneal. In comparison to ohmic marker in figure 6.4 the annealed Pt-marker shown in figure 6.5 has a much smoother line etch definition and morphology. The Pt marker layer features all requirements of high-quality e-beam markers as discussed above. The Pt marker layer comes at the cost of an additional lithography step and builds the basis for both two-step T-gate processes investigated in this work, because it ensures the overlay accuracy between gate foot layer and gate head layer.

The third approach toward high quality e-beam markers would be etched e-beam markers. In this case a topographical contrast is achieved instead of the common material contrast caused by elements with different atomic numbers. In the case of silicon technology step heights of $> 600\,\mathrm{nm}$ provide a sufficiently high contrast [221]. Generally this approach requires a highly anisotropic etch into the specific material, typically achieved with a RIE tool. However, in the beginning of this work a RIE tool with appropriate chlorine chemistry was not available. Hence a marker layer with etched e-beam marker was not investigated, although it may be a new and interesting alternative to the introduced Pt marker layer introduced in this work.

6.2.5 HSQ-based T-gate process

A sketch of process flow for the HSQ-based T-gate process is drawn in figure 6.6. The process starts with the marker layer (A in figure 6.6), the ohmic contact definition, ohmic metal deposition and subsequent RTP anneal according to the standard HEMT technology (cf. appendix A.3) corresponding to B.1 and B.2 in figure 6.6. Because HSQ features the capability to make bumpy topographies of a structured wafer planar [215], it is necessary

to conduct the gate foot definition with HSQ (C.1 and C.2 in figure 6.6) prior to mesa insulation (D.1 and D.2 in figure 6.6). The last process step is the definition of the gate head and the contact pads (E.1 and E.2 in figure 6.6). These definitions may be split into two separate lithographies, if e.g. different metalization schemes for the gates and the pads are desired.

Figure 6.7 shows a Scanning Electron Microscope (SEM) image corresponding to process step D.2 in figure 6.6. In comparison to the Si-prototype the HSQ stripes had to be designed smaller for the AlGaN/GaN material to ensure a sufficiently small gap. The requirement of smaller HSQ stripes is attributed to a higher backscattering of electrons during e-beam writing in the case of AlGaN/GaN. Figure 6.8 shows the final gate structure running across the etch of the AlGaN/GaN mesa.

Although an HSQ based T-gate process has been successfully established for the InGaAs/-InAlAs/InP material system by Jin et al. [210] and this work adopts the process to the AlGaN/GaN system the HSQ-based T-gate process was not optimized any further because of the following general difficulties observed during the development of the process:

Defining the HSQ thickness: The definition of the HSQ thickness is determined during the resist spinning. As already outlined spinning of HSQ homogeneously on small samples is already hard to do in a high yield and reproducible way. Multilayer coating with HSQ can only be achieved if intermediate temper steps are applied [215] what makes HSQ useless as an e-beam resist. Additionally it has to be considered that the thickness of the HSQ resist does not only define the height of the gate foot but also determines the minimum gap width which can be achieved. Generally reduced resist thickness allows for smaller HSQ-gaps [210].

Homogeneous HSQ coating: Besides a pronounced sidewall formation HSQ is also very sensitive to any other step in the topography on the wafer because it tends to fill up small grooves and makes the sample planar. While the influence of the mesa etch could be circumvented by defining the HSQ gate foot pattern prior to mesa isolation the influence of the ohmic contact topography had to be accounted for. In the vicinity of ohmic contact metalization, especially in the source-drain access region, the HSQ layer was thicker than in several μm distance from a step.

HSQ development on AlGaN: While during the development of Si prototypes no adhesion problems of the exposed HSQ patterns were observed during development, adhesion problems of exposed HSQ patterns were pronounced on the AlGaN surface. The explanation is that basic developer like AZ400K or TMAH are known to remove native oxides from the AlGaN surface [69]. In this way the developer TMAH does not only remove the unexposed HSQ but also lifts the exposed HSQ patterns from the AlGaN surface.

Besides the above mentioned disadvantages it should be considered that HSQ patterns, which define the gate foot, also act as surface passivation in this region. A HSQ-based surface passivation of AlGaN/GaN HEMTs has not been investigated yet, may be part of future work.

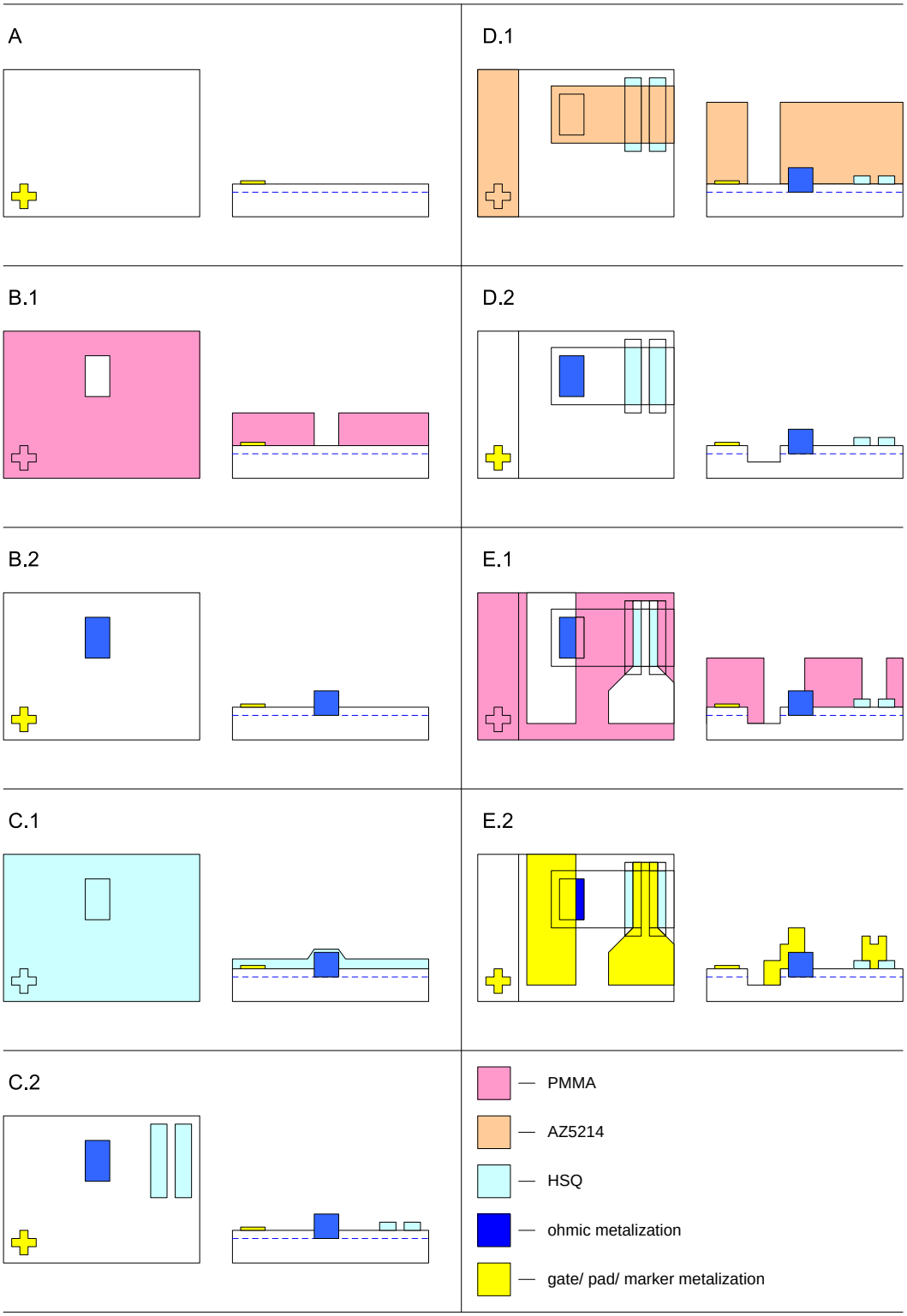

Figure 6.6: Schematic illustration of the HSQ-based T-gate process. Only one ohmic contact of the gate-symmetric structure is depicted to avoid the illustration of redundant information.

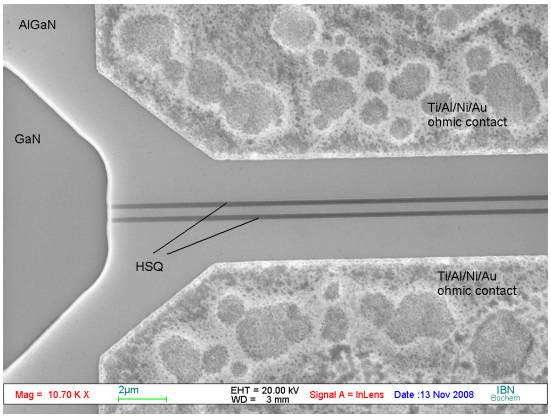

Figure 6.7: HSQ-oxide stripes running parallel through the source-drain region.

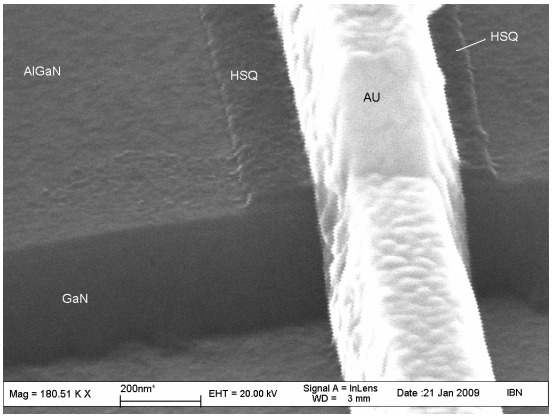

Figure 6.8: Final gate structure in between HSQ stripes running across mesa etch.

6.3 Metal-mask T-gate process for silicon nitride passivated AlGaN/GaN HEMTs

In this section the metal-mask T-gate process for silicon nitride passivated AlGaN/GaN HEMTs is outlined. In the beginning of this section the process is briefly motivated. The most critical step of the process is the definition of the gate foot which is described in detail in this section. Finally, the flow of the metal-mask T-gate process is sketched while a detailed description is given in the appendix A.4.

6.3.1 Motivation for the metal-mask T-gate process

The basic idea of this process is to define the gate foot by etching a groove into the surface passivation of the AlGaN/GaN HEMT and fill this groove in a subsequent process step with the Schottky-metalization. This approach is also used by leading groups in the field of GaN technology [148, 141, 150]. For deep-sub-micrometer HEMTs the resist ZEP may be used for the gate foot definition via e-beam lithography [148].

In this work a combined PMMA/Cr mask is used for the gate foot definition. Grooves of width down to 40 nm have been processed with this mask scheme in this work, showing that this scheme is also appropriate for deep-sub-micrometer gate foot definition. SiN was chosen as surface passivation because it is the most common dielectric of choice for this purpose [222, 223]. If applied in an appropriate way, a SiN surface passivation effectively suppresses dispersion and surface trapping effects [47] and hence potentially leading to increased output power and breakdown voltage [224, 160], reduced surface leakage current [225] as well as improved long-term reliability [226]. On the other hand a SiN passivation generally increases parasitic capacitances [148] in comparison to unpassivated devices and hence a surface passivation is expected to reduce the RF-performance [224, 160], although an improvement of RF-performance due to SiN passivation can also be found in literature [222].

6.3.2 Impact of fluorine RIE on the electrical properties of AlGaN/GaN heterojunction

The most critical step in the metal-mask T-gate process is the opening of the SiN passivation layer in order to define the gate foot. To transfer the gate foot pattern of the PMMA/Cr mask into the SiN passivation a RIE tool is used. Typical gases used to etch SiN are the fluorine-based gases CHF_3, CF_4 and SF_6. Unfortunately these fluorine gases are known to have a strong influence on the nitride semiconductor and its surface condition. For example, an SF_6/O_2 treatment prior to SiN passivation was found to lower the sheet resistance and decrease in RF-dispersion in comparison to samples processed without pretreatment [223]. Furthermore, the leakage current of Schottky-gates on GaN and AlGaN/GaN heterostructures can be significantly reduced by exposing the gate region to CF_4 plasma prior to Schottky-gate metalization [227]. Most importantly a fluorine plasma treatment can lead to the fabrication of an Enhancement-mode (E-mode) HEMTs [228].

In order to find fluorine plasma conditions which are capable of removing the SiN passivation without having a detrimental impact on the AlGaN/GaN material system, etch experiments on van-der-Pauw structures [229] were conducted in this work. The advantage of using Hall-fields is that the impact of etch conditions on sheet carrier concentration n_s and Hall-mobility μ_{Hall} can be investigated meanwhile allowing for a simplified process flow without gate lithography. Hall etch experiments started with a reference measurement on the specific sample after device processing. Subsequently the Hall-field was exposed to a certain plasma condition and Hall-data were determined again. After this first plasma exposure the step was repeated for at least two more times. Processing of the Hall-field was carried out accordantly to the standard HEMT process (cf. appendix A.3) without the gate lithography.

A CHF_3 plasma and a combined CF_4/O_2 plasma were the first ones investigated in this work. The RIE chamber conditions for the CHF_3 plasma were 30 μbar chamber pressure and 30 sccm gas flow resulting in a self-bias voltage of -330 V and -195 V for 100 W and 50 W RIE power, respectively. The chamber conditions for the CF_4/O_2 plasma were 30 μbar chamber pressure with a gas flow of (20/2) sccm. These chamber conditions lead to a self-bias voltage of about -330 V and -210 V for 100 W and 50 W RIE power, respectively. Figure 6.9 and figure 6.10 show the impact on n_s and μ_{Hall} for both plasmas as a function of summed up etch time.

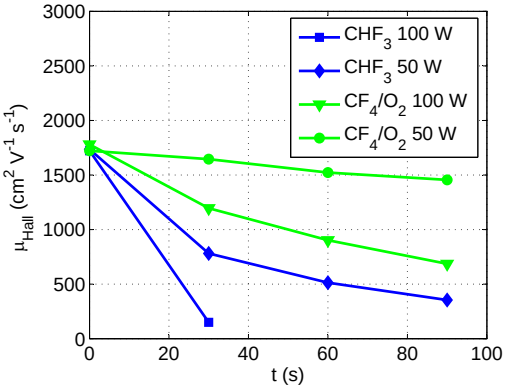

Figure 6.9: Hall-mobility μ_{Hall} as function of accumulated etch time and RIE power.

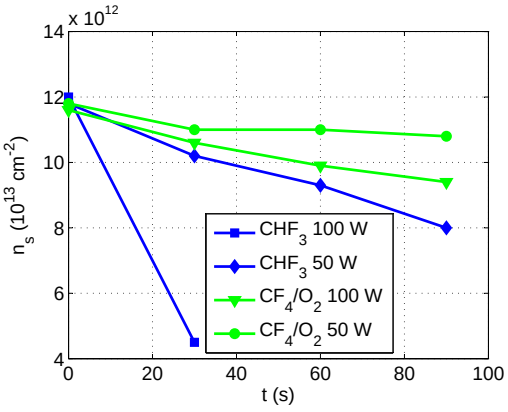

Figure 6.10: Sheet carrier concentration n_s as function of accumulated etch time and RIE power.

Three conclusions can be drawn from the results presented in figure 6.9 and figure 6.10: First of all both applied plasma conditions are clearly detrimental to the mobility and sheet concentration of the AlGaN/GaN heterojunction and the caused damage increased with exposure time. Secondly, the CHF_3 chemistry has a much more negative impact on the mobility than the CF_4/O_2 chemistry. Whether this difference originates from the chemical difference of the fluorine chemistries itself or is caused by the additional O_2 gas flow in the case of the CF_4/O_2 plasma is not clarified at the time of writing. Thirdly, the etch damage, indicated by a lower mobility, increases with applied RIE power which is accompanied with an increased self-biased in these experiments. Especially the plasma self-bias is expected to have a strong influence on the electrical properties of the GaN according to prior results [230].

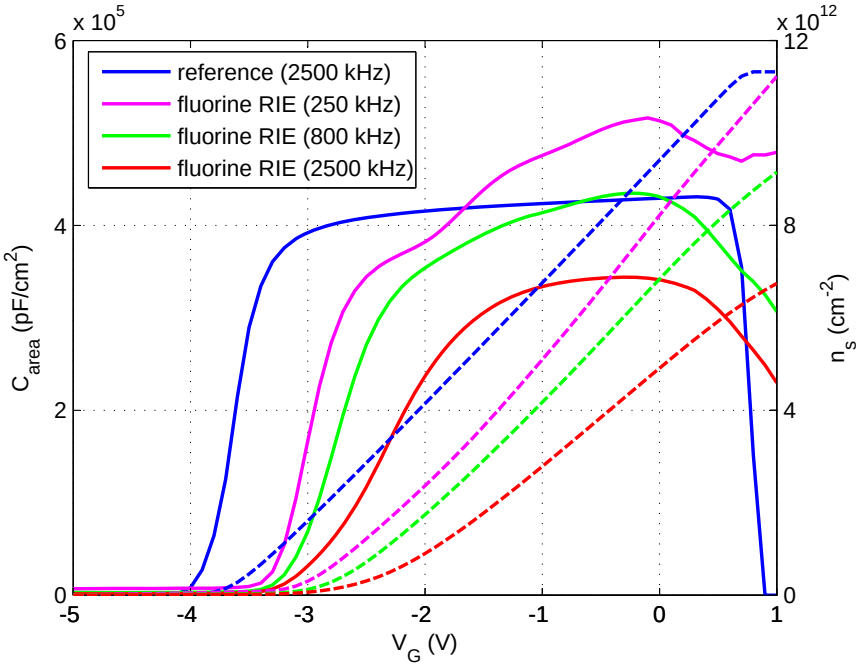

Figure 6.11: Capacitance per unit area C_{area} as determined from C-V-measurements (solid lines) together with the extracted sheet carrier concentration n_s (dashed lines). In contrast to the reference diode the fluorine plasma treated Schottky-diode exhibits a clear V_{th} shift and strong frequency dependence.

The observed reduction of n_s with increasing plasma exposure time cannot be explained by a thinned barrier layer as the etch rate is estimated to be $\leq 1\,\mathrm{nm/min}$ as known from other experiments. The introduction of acceptors which deplete the mobile electrons [227], is seen as a cause for the reduced n_s depicted in figure 6.10.

Figure 6.11 shows the influence of a fluorine plasma on the Capacitance-Voltage (CV)-characteristic of AlGaN/GaN Schottky-diode. The plasma damage, whose impact on the CV-characteristic is presented in figure 6.11, is attributed to an over etching with a CHF_3 plasma during T-gate fabrication. The CHF_3 plasma conditions were 100 W forward power with a self-bias of about $-340\,\mathrm{V}$. The duration of over etching can not be given exactly due to particularities of the metal-mask T-gate processing, but it is estimated to be less than 1 min. A low damage CF_4/O_2 plasma followed the high-bias CHF_3 RIE step, but is not expected to contribute significantly to the observed behavior. Measurements on Hall-fields, whose area is comparable to the area of the Schottky-diodes and hence are expected to

have been exposed the same plasma conditions as the diodes, exhibited a sheet resistance $R_{\square}$ of about 4700 Ω/□ and a sheet carrier concentration n_s of $7.5 \cdot 10^{12}\,\mathrm{cm}^{-2}$.

Besides the clear threshold voltage shift, which eventually leads to the fabrication of an E-mode HEMT [228], figure 6.11 shows a strong frequency dependence of the CV-characteristic of the CHF_3 treated diode in comparison to the reference diode. While for a frequency of 250 kHz the $n_s(V_G)$ dependence is even slightly steeper as for the reference diode, the $n_s(V_G)$ dependence flattens with increased frequency, indicating a worsen in the modulation efficiency. The CV-characteristic of the reference diode given in figure 6.11 was determined at 2500 kHz but its shape varies only very slightly in the range from 250 kHz to 2500 kHz and hence its frequency dependence is negligible. A broader experimental data base is desirable for a better understanding and interpretation of the observed influence of fluorine chemistry on the properties of the nitride material. E.g. studies regarding temperature dependence of fluorine etch processes might be part of future work.

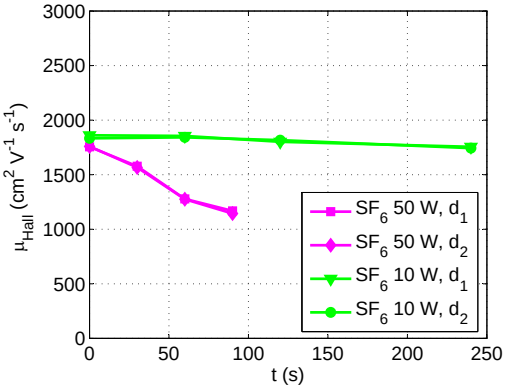

Figure 6.12: Hall-mobility μ_{Hall} as function of accumulated etch time and RIE power.

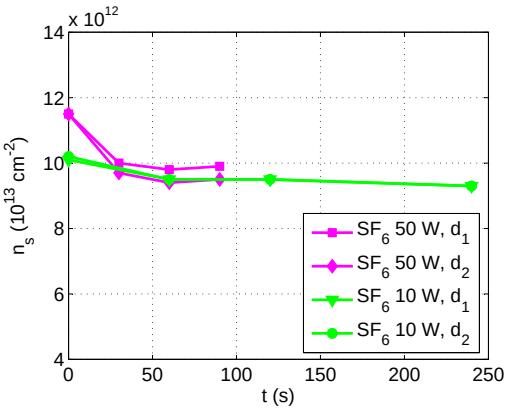

Figure 6.13: Sheet carrier concentration n_s as function of accumulated etch time and RIE power.

An SF_6 plasma as the last fluorine chemistry available for this work was also investigated. The chamber pressure was set to 20 μbar and the gas flow was set to 20 sccm. The resulting self-bias voltages were −170 V and −48 V for 50 W and 10 W RIE power, respectively. Figure 6.12 and figure 6.13 show n_s and μ_{Hall} as function of accumulated etching time and RIE power. For figure 6.12 and figure 6.13 two Hall-data sets, obtained from different Hall-fields and labeled as d_1 and d_2, are given to put the results on a broader basis. While for the SF_6 plasma the sheet carrier concentration is nearly unaffected as shown in figure 6.13 there is also a strong impact on the mobility in the case of the 50 W RIE power. In contrast to the 50 W etch condition the 10 W SF_6 plasma decreases the mobility only slightly and hence might be considered as appropriate plasma condition for opening the SiN passivation. Generally, a low RIE power plasmas with a correspondent low self-bias voltage seem to be appropriate to open the SiN passivation without causing pronounced damage to the AlGaN/GaN material and allowing for a good device performance.

Because low RIE power etching conditions were identified as beneficial, the CF_4/O_2 chemistry was investigated at low RIE powers of 30 W and 15 W, respectively. The self-bias voltage for 30 W RIE power was −170 V. The self-bias voltage for the 15 W plasma was −100 V at an increased chamber pressure of 50 μbar. As depicted in figure 6.14 the 15 W-CF_4/O_2 plasma barely affects the mobility, even for a total etch time of ten minutes. As the associated etch time for SiN is greater than 10 nm/min an appropriate etching condi-

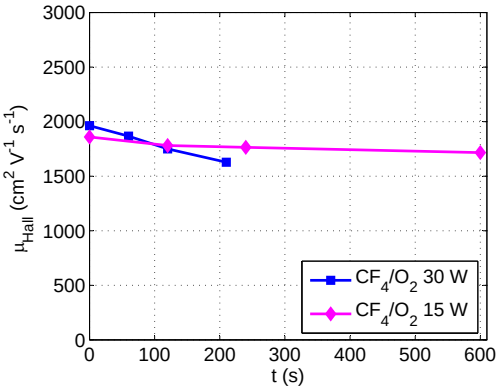

Figure 6.14: Hall-mobility μ_{Hall} as function of accumulated etch time and RIE power.

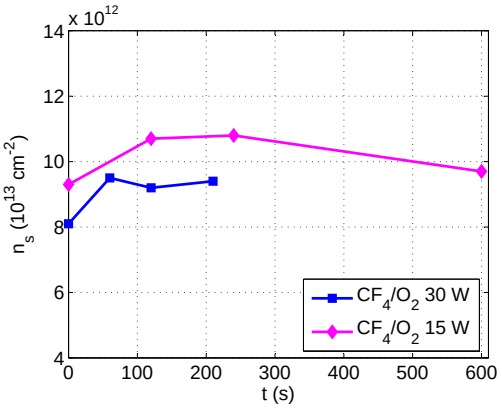

Figure 6.15: Sheet carrier concentration n_s as function of accumulated etch time and RIE power.

tion for the metal mask T-gate process was found. The variation in n_s as shown in figure 6.15 can not be explained at the time of writing but may be attributed to material or/and process variations.

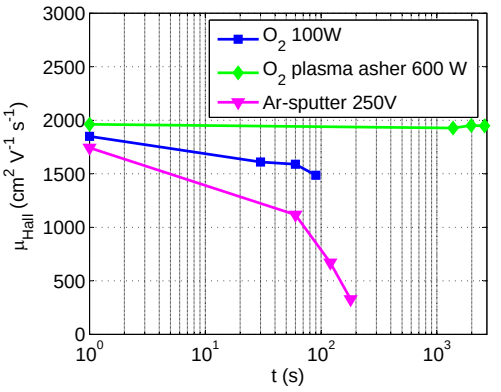

Figure 6.16: Hall-mobility μ_{Hall} as function of accumulated etch time for different plasma conditions. Initial values were plotted at $t = 1\,\mathrm{s}$ due to logarithmic scaling of the x-axis.

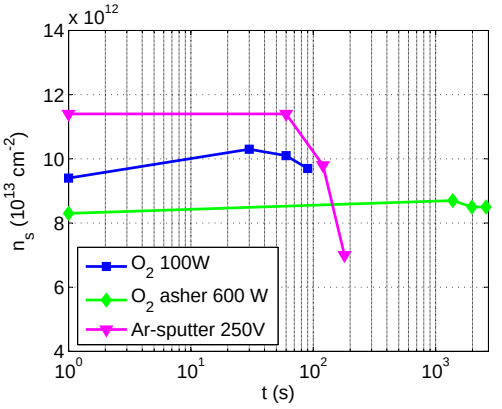

Figure 6.17: Sheet carrier concentration n_s as function of accumulated etch time for different plasma conditions. Initial values were plotted at $t = 1\,\mathrm{s}$ due to logarithmic scaling of the x-axis.

To complete the investigations on various plasmas and their impact on the electrical properties of the AlGaN/GaN heterojunction, three additional etch experiments were conducted. Firstly the impact of O_2 plasma ashing on n_s and μ_{Hall} were investigated because plasma ashing is a common cleaning step in the standard HEMT technology (cf. appendix A.3). In the plasma ashing process oxygen radicals hit the sample surface without being accelerated in the self-bias field as it is present in a RIE tool. Thus the etching in a plasma ashing tool has only a chemical component but no mechanical component. The RF-power of the plasma asher was set to 600 W with an O_2 gas flow of 200 sccm and a process chamber pressure of 1 mbar.

To study the influence of an additional mechanical etch component an O_2 RIE plasma was chosen as second etch condition. The RIE power for the oxygen plasma was set to 100 W

with a corresponding self-bias of about −340 V. The chamber pressure was 20 μbar and the O_2 gas flow was 30 sccm. In order to investigate an etch condition which features only a mechanical etch component, a Hall-field was etched in a Ion Beam Etching (IBE) tool by argon sputtering. The acceleration voltage of the Ar-ions was 250 V, the ion current was 44 mA. During IBE the chuck was tilted by an angle of 30 ° with respect to the incident ion stream and rotating. In figure 6.16 and figure 6.17 the influence on n_s and μ_{Hall} for all three plasma conditions are depicted. Each data set for a certain plasma condition was obtained on different samples and at different stages of this work. Nevertheless, the origin of the different initial conditions is not expected and can not be explained at the time of writing. But still it is instructive to compare the development of n_s and μ_{Hall} as function of time for each plasma condition.

More than 40 min of O_2 plasma ashing do not affect carrier mobility. In contrary, a high μ_{Hall} around 1900 cm^2/Vs is maintained at the cost of a relatively low n_s of about $8 \cdot 10^{12} cm^{-2}$ so that in a sum the sheet resistance is not increased by plasma ashing. But if the oxygen ions hit the AlGaN surface with additional kinetic energy as it is the case for RIE, there is a decrease in μ_{Hall} and n_s after 90 s of etching time. The observed degradation of mobility and sheet carrier concentration with increased RIE power and increased exposure time is well in accordance with prior results [231]. Argon sputtering has the most detrimental effect on μ_{Hall} and n_s. In contrast to the other plasma conditions of this study argon-sputtering clearly thins the AlGaN barrier at an etch rate of about 7.5 nm/min for the chosen conditions. Consequently the reduction of n_s is explained by a reduction of barrier thickness. The reduction of μ_{Hall} might be explained by increased surface scattering due to the reduced channel-surface distance or introduced etch damage.

In a sum the investigations show that only low-power RIE processes with a self-bias below 100 V are applicable if damage or modifications of the AlGaN/GaN material should be avoided. Besides the chosen chamber conditions the choice of the fluorine chemistry itself has a strong impact on the amount of etch damage caused. CHF_3 chemistry is found to be much more detrimental than a combined CF_4/O_2 plasma. Also SF_6 might be applicable to remove the SiN passivation without causing serious damage, if low RIE power conditions with a self-bias below 50 V are chosen.

6.3.3 Metal-mask T-gate process

In the current version of the process Cr is used as metal mask. An alternative metal is Ti which was used in the first version of this process. The advantage of Cr as mask is that it can be removed wet-chemically with a high selectivity to the silicon nitride passivation and to other metals sensitive to fluorides like Ni of the Schottky-contact or Ti/Al in the ohmic contact.

The metal-mask T-gate process starts in the same way as the HSQ-based process. Firstly, the markers are defined. Secondly, the ohmic contacts are fabricated (cf. A, B.1 and B.2 of figure 6.6). Afterward mesa insulation is performed according as depicted in steps C.1 and C.2 of figure 6.22. Subsequently a SiN dielectric layer is deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD). On top of the SiN passivation a 15 nm Cr layer is deposited via electron-beam evaporation. A single layer PMMA is spun onto the SiN/Cr stack and structured by e-beam lithography (cf. step D.1 of figure 6.22). The pattern transfer from PMMA to the Cr-mask is achieved by argon sputtering shown in step D.2 of figure 6.22.

The pattern transfer from Cr-mask into the SiN etch is performed by fluorine-based RIE. In the current version of the metal-mask T-gate process gate foot definition and opening of ohmic contact windows is performed simultaneously. Due to the different pattern size of ohmic contact windows and gate foot windows the ohmic contacts are over etched in this process step. However, a detrimental impact on the contact was not observed, especially as the ohmic metalization scheme of the standard HEMT process (cf. appendix A.3) is thick in comparison to the ones used by some other groups [141, 133]. The fluorine-based RIE step consists of a 100 W, highly anisotropic CHF_3 etch followed by a low power, low self-bias CHF_4/O_2 soft landing which removes the residual SiN in the gate foot grooves. Due to the presence of oxygen in the soft landing plasma the PMMA is removed in this step. Consequently only the Cr-mask remains as depicted in step D.4 of figure 6.22.

For the next e-beam lithography PMMA is spun and the head of the T-gate as well as the contact pads are defined. As for the HSQ-based process, this lithography might be split into two separate lithographies, if for instance different metalization schemes for the pads and the gates are desired. After the lift-off of the pad and gate metalization, as indicated in E.2 of figure 6.22, The Cr-mask has to be removed, after the lift-off of the pad and gate metalization, as indicated in E.2 of figure 6.22. This is achieved by a short Cr-wet-etch (cf. E.3 in figure 6.22).

It is important to note that the Pt-marker layer, as developed for the HSQ-based T-gate process, is also applicable for the metal-mask process. A Pt metalization thickness of 40 nm is already sufficient to ensure a successful marker search during e-beam lithography although the Pt markers are covered by the SiN passivation and the Cr/PMMA mask.

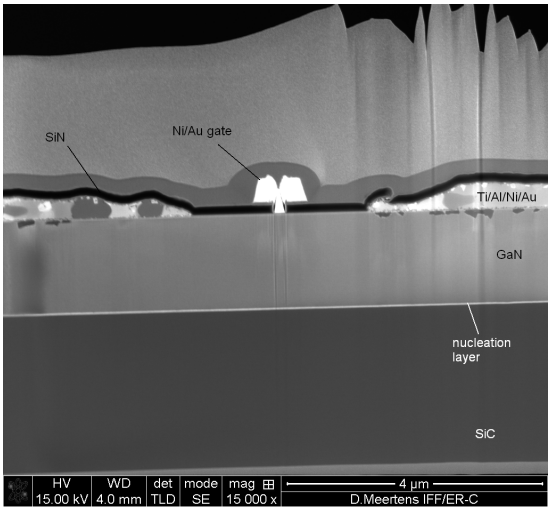

Figure 6.18: SEM image of the cross-section of a HEMT after Cr-mask T-gate process of this work.

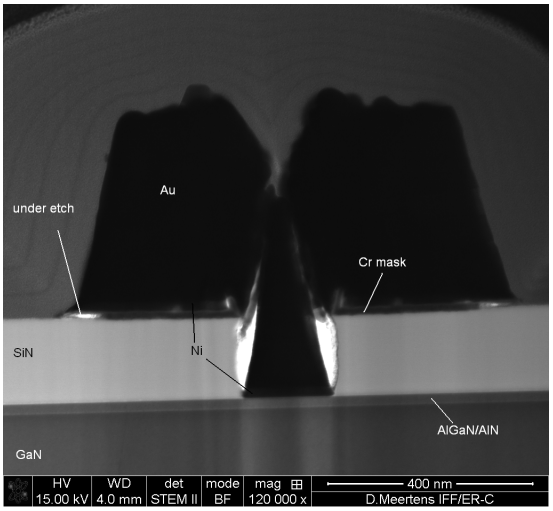

Figure 6.19: STEM image of the cross-section of a HEMT after Cr-mask T-gate process of this work.

Figure 6.18 shows a SEM picture of the cross-section of a AlGaN/GaN HEMT processed according to the metal-mask T-gate process developed in this work. The cross-sectional cut was done with a Focused Ion Beam (FIB) tool. The thin black ribbon in figure 6.18 corresponds to the SiN passivation. The T-gate is centered between the polycrystalline ohmic contacts. An excellent overlay accuracy between gate head and gate foot could be achieved. The SiC substrate, colored dark-gray, is also partly visible at the bottom of figure 6.18. The SiC substrate is separated from the 2 μm-thick GaN buffer layer by a thin nucleation layer, colored light-gray.

A more detailed view of the T-gate is given by a Scanning Transmission Electron Microscopy (STEM) image shown in figure 6.19. In contrast to the SEM picture in figure 6.18 the black-white scale appears reversed, i.e. elements with a high atomic number appear darker than those with a low atomic number. Consequently, the gate itself appears almost black while gaps appear white in the STEM mode. White gaps in figure 6.19 next to the gate foot indicate material free space.

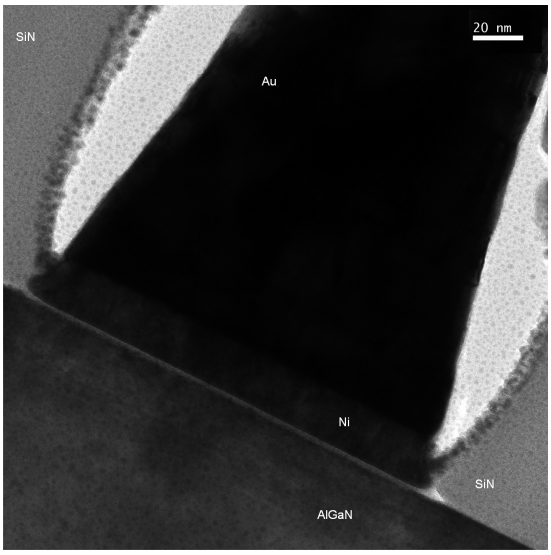

Figure 6.20: TEM image of the gate region of a HEMT after Cr-mask T-gate process of this work.

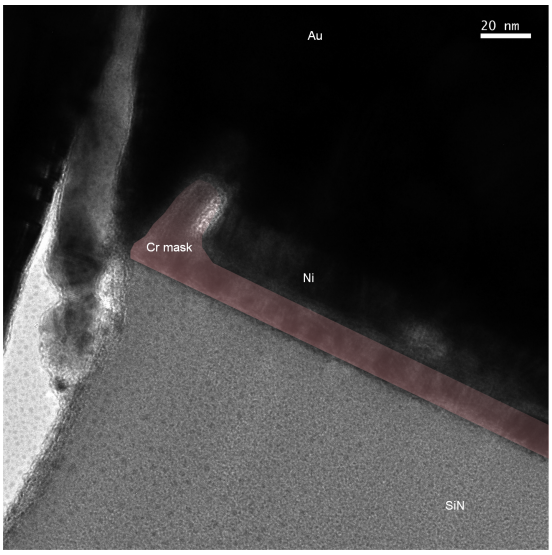

Figure 6.21: TEM image of the contact region of gate foot and gate head with residual Cr-mask.

The curvature of these gaps in the SiN passivation is due to the anisotropic nature of the soft-landing CHF_4/O_2 etch. The other two white gaps can be found underneath the edges of the gate head. These gaps originate from the final Cr-mask removal, i.e. a wet-chemical under-etching. The 20 nm thick AlGaN barrier layer on-top of the GaN buffer layer is also clearly depicted at the bottom of figure 6.19.

Figure 6.20 shows a Transmission Electron Microscopy (TEM) image of the gate foot on-top of the AlGaN barrier layer. The crystalline structure of the AlGaN is now visible in figure 6.20 and there is a thin layer, colored light gray as the SiN passivation, at the Ni-AlGaN interface. For this sample a wet-chemical cleaning procedure prior to gate metalization was omitted and hence the Ni-AlGaN interface is in its state after soft-landing with the CHF_4/O_2 RIE and an oxygen descum step.

Finally, figure 6.21 shows the contact region of the gate foot and the gate head together with the residual Cr-mask. The residual Cr-mask is emphasized by a shallow red coloring. The spike of the Cr-mask near the gate foot opening is caused by redeposition effects during pattern transfer from PMMA to the Cr-mask by argon sputtering.

6.4 Gamma- vs. T-gate

A reduction of R_g can be achieved by the application of T-gates whose technology and development are discussed in this chapter 6. However, the gate-drain feedback capacitance C_{gd} as depicted in figure 3.9 and in figure 3.10 is as important to f_{max} as R_g itself according

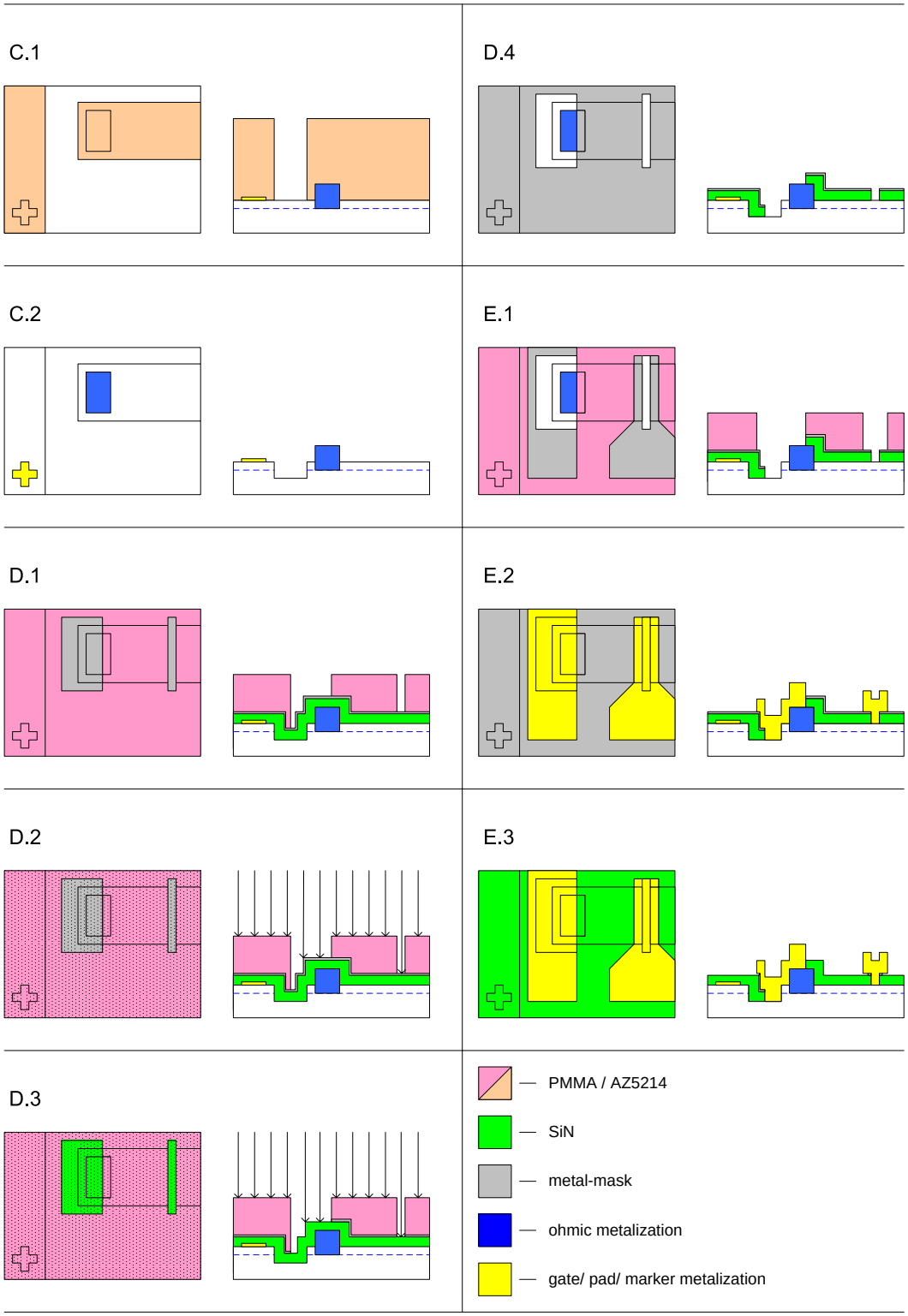

Figure 6.22: Schematic illustration of the metal-mask T-gate process. Only one ohmic contact of the gate-symmetric structure is depicted to avoid the illustration of redundant information.

to (5.9). Therefore it is instructive to study HEMTs which have nominally the same R_g but different C_{gd} values. One way to study the impact of the gate-drain capacitance C_{gd} on the RF-performance is comparing the performance of HEMTs with T-gates to HEMTs employing Γ-gates. Γ-gates are T-gates whose gate head is asymmetrically positioned on the gate foot. Figure 6.23 shows a SEM picture of a T-gate which was fabricated according to the Cr-mask T-gate process of this work. Figure 6.24 shows a SEM picture of a corresponding Γ-gate.

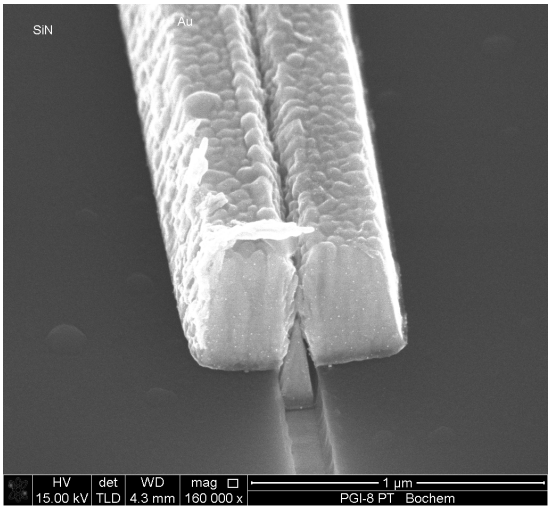

Figure 6.23: SEM image of a T-gate of the Cr-mask process of this work.

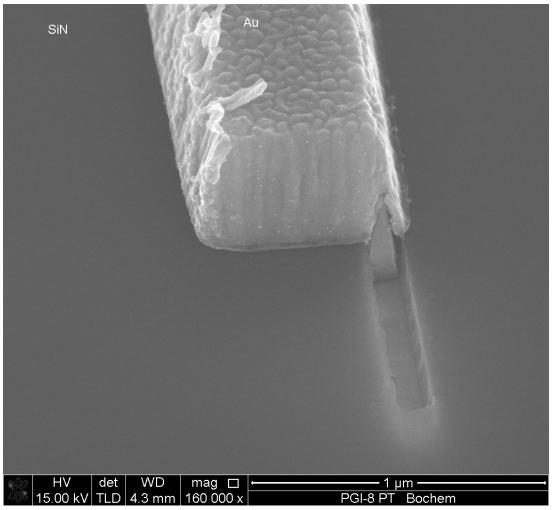

Figure 6.24: SEM image of a Γ-gate of the Cr-mask process of this work.

It is clear from electrostatic considerations that shifting the gate head toward the source side of the HEMT causes a decrease in the parasitic C_{gd} and an increase in parasitic C_{gs}. Because the gate head definition and the gate metalization thickness is the same for T-gates and Γ-gates, both gates are expected to have the same R_g value. This interesting experiment was done for AlGaN/GaN HEMTs by Palacios et al. for the first time according to the literature [100].

Because of the relevance of this experiment to this work it was repeated by own means. In contrast to the experiment made by Palacios et al. instead of T-gates mirrored Γ-gates, i.e. gate with the gate head shifted to the drain, were fabricated in order to increase the effect a varying C_{gd} and C_{gs}, respectively. In the following Γ-gates denote gates whose gate head is shifted to toward the source, i.e. reduced C_{gd}. Mirrored Γ-gates denote gates whose gate head is shifted toward drain, i.e. increased C_{gd}, and are referred to as m-Γ-gates in following. The Γ-gates and the m-Γ-gates were fabricated according to the metal-mask T-gate process as described in detail in section 6.3 of chapter 6 of this work. The epitaxial material used was grown by the company CREE on SiC. It consists of a 2 μm GaN buffer, a 1.25 nm AlN spacer and a $Al_{0.29}Ga_{0.71}N$ unintentionally doped barrier layer of 20 nm thickness.

The thickness of the SiN passivation is about 150 nm. The gate head is about 600 nm in width with a gate metalization thickness of about 400 nm. A high-yield of Γ-gate HEMTs with a precise off-set of the gate head with respect to the gate foot could be achieved due to the marker layer which was introduced in this work. A SEM picture of a Γ-gate characterized is given in appendix A.8.

Figure 6.25 and figure 6.27 compares the input and output characteristics of a HEMT

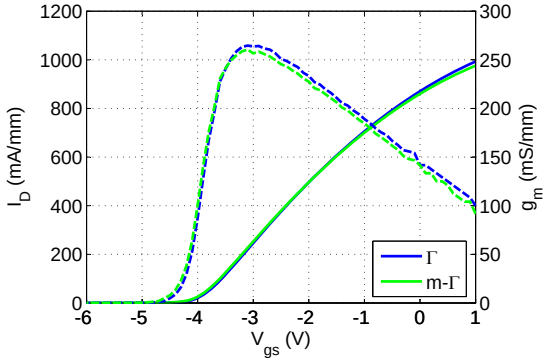

Figure 6.25: Input characteristic of m-Γ-gate and Γ-gate HEMT. $V_{DS} = 5\,\mathrm{V}$.

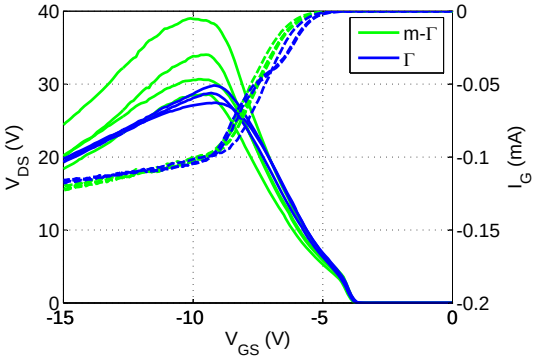

Figure 6.26: Comparison of V_{DS} and I_G of m-Γ-gate and Γ-gate HEMTs for constant I_D of 0.1 mA.

with a m-Γ-gate to those of a HEMT with a Γ-gate structure. Because both characterized devices feature the same dimensions except the position of the gate head, i.e. $W = 2 \times 60\,\mu\mathrm{m}$, $d_{SD} = 5\,\mu\mathrm{m}$, L_G is about 100 nm, their DC-behavior is almost identical. Also the gate-current behavior is very similar as depicted in figure 6.27. First differences in DC-behavior becomes apparent if the breakdown voltage BV_{DG} according to reference [232] is investigated. Figure 6.26 shows the measured breakdown characteristics for Γ-gate and m-Γ-gate devices.

The average breakdown voltage BV_{GD} of Γ-gate HEMTs was about 35 V. Counterparts with a T-gate exhibited an average BV_{GD} of about 43 V. Of course, the observed trend regarding the breakdown behavior should be put on a broader data basis in future work. But generally a better breakdown capabilities of the m-Γ-gate HEMTs in comparison Γ-gate HEMTs is expected due to a field-plate effect caused by the gate head overlap toward the drain side of the gate. In a sum devices with a m-Γ-gate and devices with a Γ-gate exhibit very similar DC-behavior. Only with respect to the breakdown properties the m-Γ-gate devices tend to achieve higher BV_{GD} values.

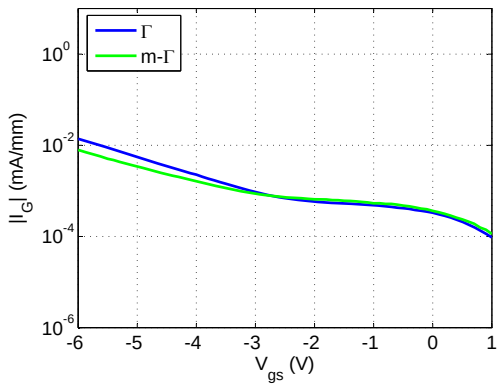

Figure 6.27: Gate current of m-Γ-gate and Γ-gate HEMT at $V_{DS} = 5\,\mathrm{V}$.

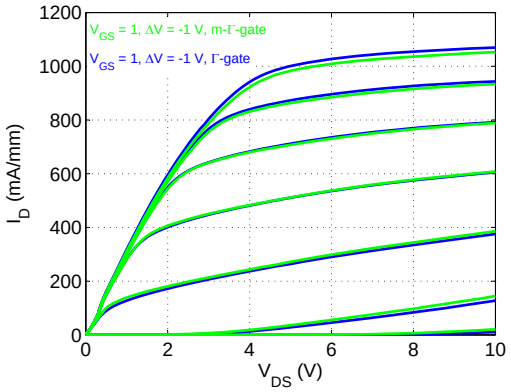

Figure 6.28: Output characteristic of m-Γ-gate and Γ-gate HEMT.

Figure 6.31 illustrates a typical difference between the RF-data of m-Γ-gate and Γ-gate

HEMTs. A clear improvement of f_T and f_{max} is achieved if Γ-gates are utilized instead of standard m-Γ-gates. While the m-Γ-gate HEMT only exhibits a maximum f_T of about 50 GHz the Γ-gate HEMT achieves about 60 GHz. Also the maximum f_{max} improves from about 80 GHz to about 125 GHz, if a Γ-gate is employed instead of a m-Γ-gate.

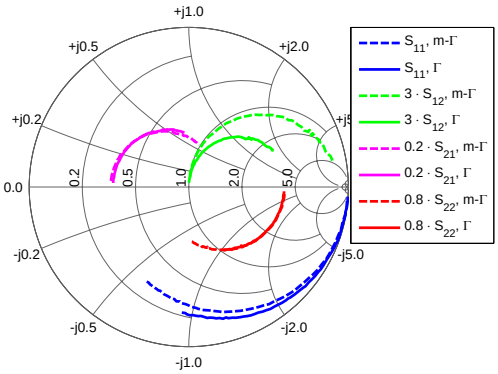

Figure 6.29: Comparison of measured S-parameters for a m-Γ-gate and Γ-gate device. $V_{GS} = -4.4\,\mathrm{V}$. $V_{DS} = 14\,\mathrm{V}$. $f = 1..30\,\mathrm{GHz}$.

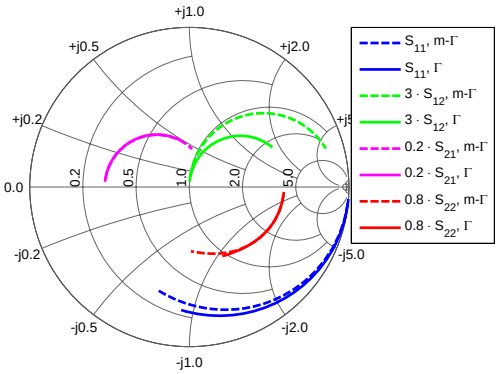

Figure 6.30: Comparison of modeled S-parameters. $f = 1..30\,\mathrm{GHz}$.

The difference in the S-parameters which is caused the shift of the gate head toward the source is depicted in figure 6.29. The strongest influence caused by the gate head shift is observed for the S_{12} parameter which is generally associated to the feedback mechanism (cf. section 4.3). In order to understand the observed change of the S-parameters better simple small-signal models are considered on the basis of the observed DC-data and typical values for small-signal parameters of an AlGaN/GaN HEMT. Modeling on the basis of small-signal parameter extraction may be part of future work. For the device with a Γ-gate structure the following parameters are considered: $W = 0.120\,\mathrm{mm}$, $R_s = R_d = 1.4\,\Omega{\cdot}\mathrm{mm}$, $R_g = 15\,\Omega/\mathrm{mm}$, $g_m = 440\,\mathrm{mS/mm}$, $g_d = 43\,\mathrm{mS/mm}$, $R_i = 0.09\,\Omega{\cdot}\mathrm{mm}$, $C_{gs} = 770\,\mathrm{fF/mm}$, $C_{gd} = 110\,\mathrm{fF/mm}$, $C_{pgs} = 10\,\mathrm{fF}$, $C_{pds} = 30\,\mathrm{fF}$,$C_{pgd} = 5\,\mathrm{fF}$. For the small signal model of the m-Γ-gate device all parameters except C_{gs} and C_{gd} are held constant. In the case of the m-Γ-gate device C_{gs} is reduced by 190 fF/mm to 580 fF/mm while C_{gd} is increased by the same amount to a value of 300 fF/mm. The value of 190 fF/mm is about the value which the gate head overlap of about 500 nm is expected to cause. Figure 6.30 shows the comparison of the modeled S-parameters for a m-Γ-gate and a Γ-gate device. Figure 6.30 shows that the difference in the measured S-parameters can be explained by a trade between C_{gs} and C_{gd} while the magnitude of the traded value is about the electrostatic capacitance caused by the gate head overlap on each side of a m-Γ-gate structure. On the basis of the modeled S-parameters an f_T/f_{max} of 52/121 GHz is predicted for the Γ-gate device while 45/80 GHz is expected for a T-gate device (cf. appendix A.6). These predicted RF figures of merit are in good agreement with the observed performance depicted in figure 6.31.

In a sum the RF-performance improvements caused by Γ-gates are in accordance with prior results as known from literature [100] and they allow to draw two important conclusions: Firstly, the gate-drain capacitance has a strong impact on the HEMT RF-performance and its influence is comparable to the one of R_g itself. Secondly, because in this experiment the parasitic C_{gd} is treated for the parasitic C_{gs} by shifting the gate head it is shown that the parasitic gate-drain capacitance may play the dominant role of both. In this sense a simple

approximation for f_T like $f_T \approx g_m/C_{gs}$ does not mirror all interdependencies, which are relevant to the RF-performance optimization of FETs, and hence maybe regarded as an over-simplification in same cases.

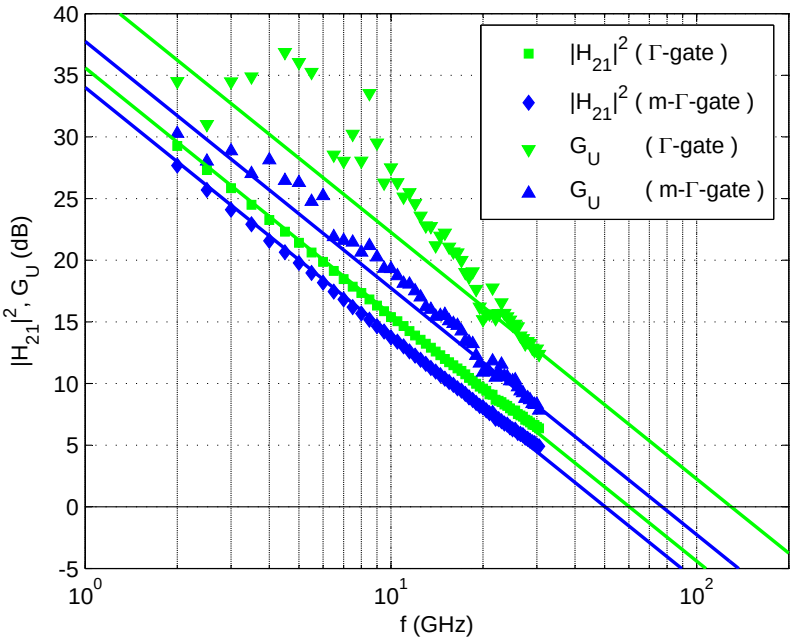

Figure 6.31: Current-gain $|H_{21}|^2$ and Unilateral Power Gain G_U for a Γ-gate HEMT and a T-gate HEMT. $L_G \approx 100\,\text{nm}$, $W = 2 \times 60\,\mu\text{m}$, $d_{SD} = 5\,\mu\text{m}$.

Figure 6.32 shows that the observed superior RF-performance of Γ-gate HEMTs in comparison to m-Γ-gate HEMTs is generally the case. The square markers in figure 6.32 refer to $W = 2 \times 60\,\mu\text{m}$ HEMTs with a source-drain spacing of $5\,\mu\text{m}$. Additionally f_T and f_{max} values of T-gate HEMTs and Γ-gate HEMTs with a gate widths of $2 \times 110\mu\text{m}$ have been added to figure 6.32 in order to provide a broader data base. Although the HEMTs of $220\,\mu\text{m}$ width are not directly comparable to the HEMTs of $120\,\mu\text{m}$ width, because they exhibit a shorter d_{SD} of $3\,\mu\text{m}$, their RF-performance is also clearly improved by the application of Γ-gates instead of m-Γ-gate.

Additionally it can be observed in figure 6.32 that the HEMTs with a shorter gate width W exhibit a slightly better f_{max}-performance independently of the type of the gate. In this sense a reduction of W below $2 \times 60\,\mu\text{m}$ might also be useful for T-gate HEMTs or Γ-gate HEMTs, respectively, if high f_{max} values are desired.

6.5 Summary

This chapter starts with a survey of various T-gate processes and briefly discusses their basic ideas, advantages and disadvantages. Two approaches of a T-gate process, the HSQ-based T-gate process an the metal-mask T-gate process for passivated AlGaN HEMTs, were developed and investigated in this work and are described in this chapter. Their process flows including relevant intermediate results like spinning procedures and etch conditions are also outlined. The introduction of Pt-marker layer is described as a key improvement of this work because it allows for reproducible, high-yield two-step T-gate

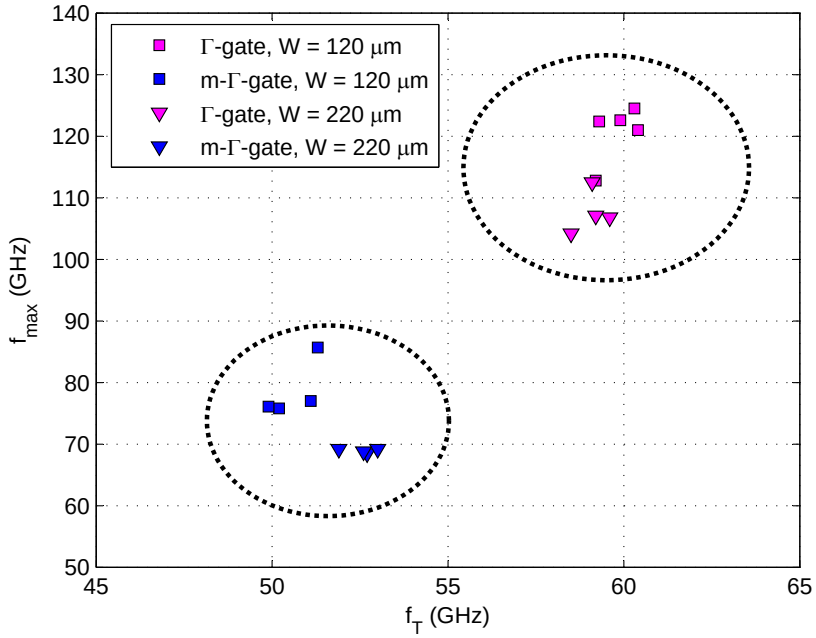

Figure 6.32: Comparison of RF-performance of m-Γ-gate HEMTs and Γ-gate HEMTs for two different gate widths W.

processes. On the basis of the developed Cr-mask process HEMTs with different gate cross-sectional structure, i.e. m-Γ-gate structure and Γ-gate structure, are characterized. Γ-gate devices achieve a better RF-performance than their counterparts with a mirrored Γ-gate because of a reduced C_{gd} feedback capacitance. Because of the relevance of a low C_{gd} for a good RF-performance a combined SiN/HSQ passivation scheme is proposed for future work. While SiN ensures a proper surface passivation, the HSQ-layer carries the gate head meanwhile keeping parasitic capacitance of a T-gate structure low.

CHAPTER 7

Recessing Technology

In this chapter the two recess procedures investigated in this work are outlined. After a brief discussion of general aspects regarding a recess technology for AlGaN/GaN HEMTs each recess approach of this work is described in detail and their advantages and disadvantages are discussed.

7.1 General considerations regarding recessing of AlGaN/GaN HEMTs

In a recess procedure the distance between gate metalization and channel is reduced by a thinning of the barrier layer. Generally, the specific thinning procedure should be reproducible and controllable what commonly requires etching at low rates, because only a few nanometers of the AlGaN barrier have to be removed for typical applications [100]. Furthermore the remainder of the thinned barrier layer should maintain its crystal quality to ensure high device performance. Consequently, a slow and non-detrimental etch procedure for AlGaN had to be developed in this work in order to study recessed devices.

Commonly chlorine based dry-etch techniques are applied for the reduction of the AlGaN-barrier thickness [1, 167, 147, 170]. A low power Cl_2 based RIE process was found to be applicable for the fabrication of recessed AlGaN HEMTs with excellent microwave performance [171]. Pure BCl_3 chemistry may also be used for dry-etching GaN [233]. Furthermore BCl_3 pretreatment was found to efficiently remove native surface oxide, which causes pronounced etch-delays during Cl_2 based RIE processes, if it is not initially removed [234, 235]. Consequently combined BCl_3/Cl_2 RIE processes are employed by leading groups in the field of GaN technology [130, 236]. A Cl_2/Ar gas mixture in an Inductively Coupled Plasma (ICP) RIE tool was also successfully used for recessing AlGaN/GaN HEMTs [147] while incorporation of argon to the Cl_2 potentially leads to smoother etch surfaces [237].

Fluorine based dry-etch procedures for AlGaN have also been investigated [238] and may feature slow etch rates and low selectivity while maintaining a smooth surface [239]. But as discussed in chapter 6, RIE with fluorine gases has a strong impact on the electrical characteristics of the AlGaN/GaN material system and therefore they commonly are not considered for recessing steps.

Standard wet-etch recipes are not applicable to nitrides without being augmented e.g. by UV-illumination or elevated temperatures [240, 241]. Nevertheless, digital wet-etch techniques might be applicable as recess procedure for AlGaN/GaN HEMTs [159], but they are not investigated in this work. Instead two dry etch techniques are investigated and described in the following sections.

7.2 Recessing AlGaN/GaN HEMTs by argon sputtering

In the beginning of this section the recess procedure by argon sputtering is motivated. Afterward the procedure itself is described and the related results are discussed.

7.2.1 Motivation

One way of thinning the barrier layer is by argon sputtering with an IBE tool. Because argon-sputtering lacks the chemical assistance an IBE process typically exhibits lower etch rates in comparison to a RIE process. Beside the technical challenges imposed by handling hazardous chlorine gases in the case of a RIE approach RIE processes may suffer from an initial etch delay caused by native surface oxides [234]. An etch delay is not expected to be pronounced for pure sputtering processes because they feature only a minor material selectivity. The approach of recessing AlGaN/GaN HEMTs by argon-based IBE was reported before by Breitschädel et al. [86]. In their work [86] the authors claim to achieve a 25 nm-recess into a 50 nm barrier layer by argon sputtering which is accompanied by the expected increase in transconductance. However, the presented DC-characteristics are not consistent with a 25 nm-recess. Therefore the reference [86] should not be regarded as a successful example for an argon-sputter recess on AlGaN/GaN, especially if device variations due to an inhomogeneous epitaxy are considered what might well have been the case in the early years of GaN research.

In their follow-up publication [242] Breitschädel et al. investigate argon-based IBE in more detail. In their work [242] the authors found that channeling of argon ions is a significant phenomenon during the sputter process even at energies as low as 250 eV. The channeling of argon ions through the barrier causes a strong degradation of the 2DEG carrier mobility. According to reference [242] the channeling effect can be suppressed if ion incident angles of larger than 40 ° are chosen. Thus for argon sputter processes aimed at sufficiently tilted chucks, no degradation of the 2DEG mobility is expected [242]. The etching time in reference [242] was 30 s, corresponding to a $3 - 4$ nm thinning of a 36 nm barrier with an as-grown 2DEG mobility between 700 $\mathrm{cm}^2/\mathrm{Vs}$ and 1000 $\mathrm{cm}^2/\mathrm{Vs}$.

Haberer et al. also investigated the impact of argon sputtering on the GaN crystal by using an InGaN quantum well as a probe [243]. The etch damage is quantified by the degree of relative reduction in Photo-Luminescence (PL) intensity. In accordance to reference [242] the etch damage caused by argon ions hitting the GaN surface perpendicular is more pronounced than the damage caused under tilted sputtering. This is because the $\langle 0001 \rangle$ direction is the most likely channeling direction in wurtzite GaN (cf. chapter 2). Hence Haberer et al. also suggest channeling as a mechanism for sub-surface dry etch damage in GaN [243]. In contrast to Breitschädel et al. the group of Haberer also notices a pronounced sub-surface etch damage (indicated by reduced relative PL) for angles of incidence far greater than 40 ° [242]. The observed penetration depth of sputter damage was more than 100 nm below the surface. Simple ion stopping models predict a damage distribution depth of only 2 nm for 200 eV argon ions at 30 ° from normal incidence to the GaN [244]. Thus simple models do not explain the large depth of the observed damage distribution. As an explanation for the deep etch damage propagation in GaN a cooperative effect of channeling and defect diffusion might be considered [244].

Low-energy argon bombardment with ion energies of 70 eV or less is not expected to have a detrimental impact on mobility and sheet-carrier concentration of AlGaN/GaN

heterostructures [171]. But because sputter processes require acceleration voltages > 100 V to substantially remove material, their application as low-damage recess procedures seem questionable. Nevertheless, according to Breitschädel et al. [242] there might be a chance of thinning the AlGaN barrier without causing a degradation in 2DEG mobility, if a low acceleration voltage of 250 V and a large angle of incidence is chosen during sputtering.

7.2.2 Experimental

Figure 7.1 shows the schematic structure of the material stack used in this work as grown by CREE. As substrate material SiC was chosen. On top of a 2 μm semi-insulating GaN buffer an AlN spacer layer was grown followed by a 20 nm unintentionally doped AlGaN barrier layer with an aluminum content of 29 %. Processing of the devices consisted of two main steps. Firstly two different samples were thinned by argon-sputtering. During sputtering one edge of each sample was covered with AZ5214 photo resist to leave a reference surface on each sample. In the second step HEMTs together with common test structures were fabricated on these two samples in parallel. One reference sample, which was not subjected to sputter process, is referred to as sample A in the following. The recessed samples are labeled B and C with increasing recess depth, i.e. reduced $t_{barrier}$. The objective of this experiment is to study the impact of the thinning procedure on the electrical properperties of the material. Of course, a global thinning procedure is not suitalbe for the fabrication of high performance devices because the access resistances will increase if the sheet resistance increases due to a thinned barrier. For all large area characterization structures like van-der-Pauw fields, long-channel HEMTs and large area diodes the difference between a global recess approach and a local recess approach is not pronounced to due to the small percentage of the differently treated material. If in addition to large area structures short-channel devices are fabricated the global recess approach has the advantage that long-channel and short-channel device will exhibit the same barrier tickness. If short-channel and long-channel devices are locally recessed the resulting recess depth is expected to be different because etching/sputtering on large areas is generally faster then at the bottom of small resist grooves.

7.2.2.1 Barrier thinning by argon-sputtering

The acceleration voltage of the Ar^+-ions was chosen to be 250 V. The samples were clamped on a rotating chuck which was tilted by 30° with respect to the direction of the incident Ar^+-ions as shown in figure 7.1 in order to prevent a possible channeling-effect. The ion current density was 0.44 mA/cm^2. With these parameter an etch rate of about 3 nm/min was achieved. An etch delay was not observed. After the sputter process the samples were cleaned in acetone for > 12 h to remove the photo resist in the edges of the samples. Subsequently the samples were cleaned in a 300 W oxygen plasma in a plasma ashing tool for 10 min. Afterward the samples were dipped in an HF/H_2O solution (1:10) and an HCl/H_2O solution (1:2) for 2 min each to remove possible surface contamination caused by redeposition during the sputter process. A subsequent Atomic Force Microscopy (AFM) on the cleaned surface revealed that the root-mean-square surface roughness is about 0.7 nm for non-sputtered sample A and for the sputtered samples, i.e. the argon-sputter process did not roughen the AlGaN surface in a way measurable by the AFM used.

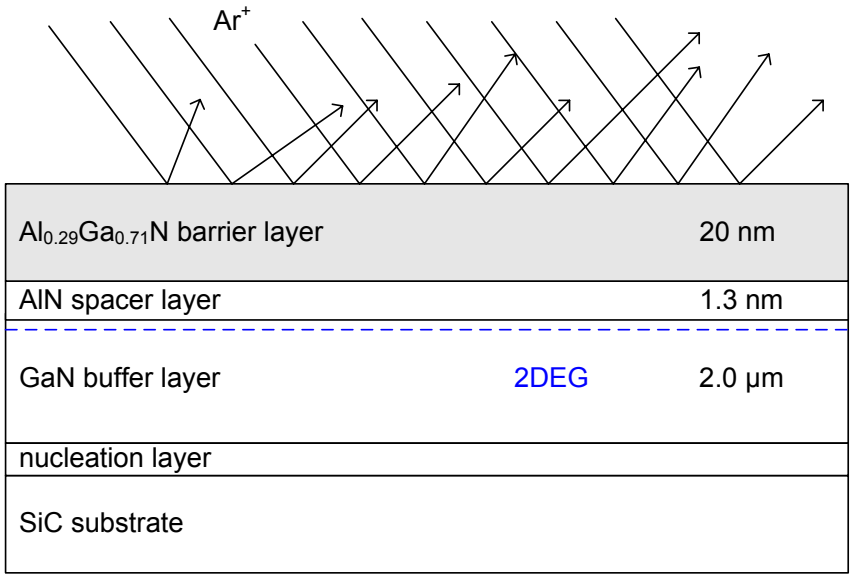

Figure 7.1: Argon-sputter process of the used material stack. During the sputter process the rotating chuck was tilted with respect to the incident Ar^+-ions by 30°.

7.2.2.2 Device processing

Device processing was similar to the standard HEMT process (cf. appendix A.3), but started with the marker layer developed in this work. Mesa insulation was performed with the same IBE-tool which was used for the initial barrier thinning. For ohmic contact formation a Ti/Al/Ni/Au was deposited by the means of electron beam evaporation and subsequently annealed at 885°C for 30 s in N_2 ambient. Each sample was processed with long-channel HEMTs ($L_G = 50\,\mu$m), so-called FATFETs, and short-channel HEMTs with an L_G between 80 nm and 300 nm. Gate metalization consisted of 25 nm Ni and 90 nm Au. The HCl dip of 10 s duration prior to gate metalization according to the standard HEMT technology was omitted in this experiment to avoid potential adhesion and lift-off problems of sub-100 nm gates investigated in parallel.

7.2.3 Results and discussion

Table 7.1 shows the sheet resistance R_{sheet}, n_s and μ_{Hall}, determined by Hall-measurements on ungated Van-der-Pauw patterns, as a function of recess depth. While n_s decreases by about 37 % and thus maintained above $0.5 \cdot 10^{13}\text{cm}^{-2}$ for a recess depth of about 8 nm, μ_{Hall} of sample C decreases by 62 % in comparison to sample A. Reduced n_s and μ_{Hall} cause an increase of R_{sheet} with increased recess depth as listed in table 7.1.

To confirm the results obtained by Hall-measurements C-V- and I-V-measurements were conducted on the FATFETs of samples A, B and C. Figure 7.2 shows the capacitance per unit area C_{area} and n_s as function of the applied voltage V_G. The values of n_s obtained from Hall-measurement are well in accordance with the values from CV-measurements for $V_{diode} = 0$ V. The observed reduction of n_s with thinner barrier layer is expected on basis of

prior work, e.g. [245, 246]. Additionally figure 7.2 depicts a clear increase of V_{th}. This shift of V_{th} toward positive voltages is especially interesting for power electronic applications as in this field normally-off devices are desired [87].

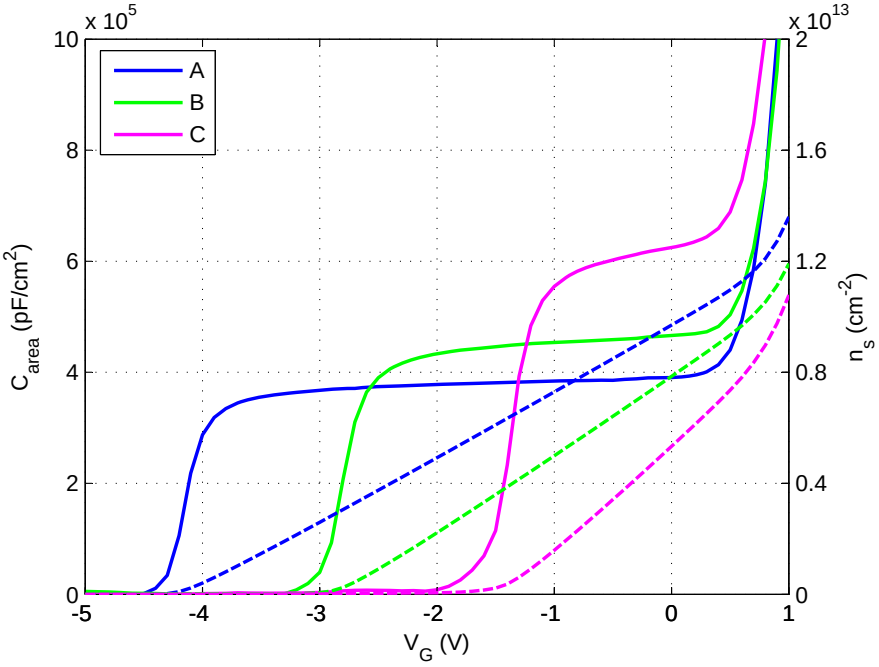

Figure 7.2: Capacitance per unit area C_{area} as determined from C-V-measurements (solid lines) together with the extracted sheet carrier concentration n_s (dashed lines) for samples A, B and C recessed by argon sputtering, both as a function of applied voltage V_G.

For the investigation of μ_{drift} the channel conductance G_{CH} was determined as a function of the gate potential V_G by measuring the drain current at a drain-source bias of 30 mV [247]. With G_{CH} the drift-mobility is calculated according to (7.1) where e denotes the elementary charge constant and W denotes the gate-width of the FATFETs.

$$\mu_{drift}(V_G) = \frac{G_{CH}(V_G) \cdot L_G}{e \cdot W \cdot n_s(V_G)} \tag{7.1}$$

The values of drift mobilities at $V_G = 0\,\mathrm{V}$ are in good agreement with those obtained from Hall-measurements as depicted by figure 7.3. All three mobility curves show a positive dependence on n_s at low n_s, i.e. an increase of mobility with an increase of n_s is observed. This effect is explained by increased screening from ionized impurities and dislocations [248, 249]. The channel mobility of the HEMT A fabricated on the as-grown

Sample	R_{sheet} $\Omega/\square$	n_s $10^{12}\,\mathrm{cm}^{-2}$	μ_{Hall} $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$	recess depth nm
A	392	8.09	1958	0.0
B	891	7.51	1011	3.7
C	1650	5.12	736	8.4

Table 7.1: Results of Hall-measurements for samples A, B and C with different recess depth achieved by argon sputtering.

material exceeds 2000 cm^2/Vs for a gate voltage around −2.5 V, a result as it is expected for AlGaN/GaN HEMTs grown on SiC substrate [250].

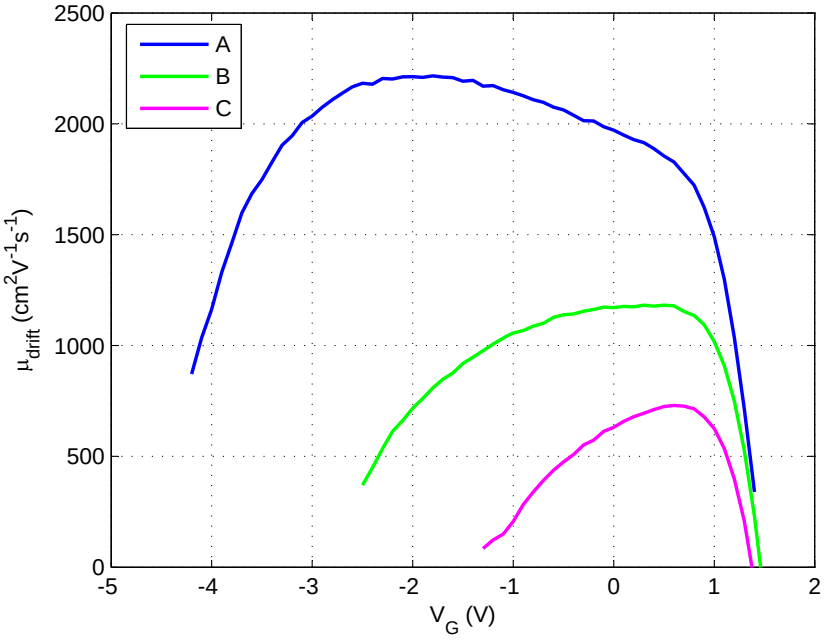

Figure 7.3: Drift mobility for samples A, B and C recessed by argon sputtering as a function of applied gate potential V_G.

Furthermore all three samples show a strong decrease in mobility for $V_G > 0.8\,V$. In this regime C_{area} increases rapidly and n_s reaches values greater than $10^{13}\,cm^{-2}$ as shown in figure 7.2, indicating a spill-over of electrons from the channel into the AlGaN barrier layer. The electrons in the AlGaN barrier layer build a parallel conduction path in addition to the 2DEG, meanwhile subjected to the low AlGaN bulk mobility instead of the high 2DEG mobility and hence explaining the strong decline of the measured mobility for $V_G > 0.8\,V$ [251]. Because the carrier confinement toward the GaN buffer weaker than toward the barrier a further penetration of carriers into the buffer might also be considered as a cause for the reduced drift-mobility. Another generally recognized reason for degrading mobility at higher V_{GS} is that the wave functions of the 2DEG shift toward the buffer-barrier interface and hence the electrons are subject to interface roughness scattering [249].

While sample A reaches its peak value of μ_{drift} for a gate potential of about −2 V samples B and C achieve their maximum drift mobility at a positive gate potential. The decrease of μ_{drift} of sample A for $V_G = -2\,V...0.8\,V$ is attributed to intersubband scattering [252] as electrons have to populate higher subbands in the well of the AlGaN/GaN heterojunction as n_s increases [247].

Obviously the effect of intersubband scattering is not pronounced for samples B and C although e.g. sample B reaches a sufficient high n_s for $V_G = -1\,V...0.8\,V$ in comparison to sample A as shown in figure 7.2. An explanation for this behavior is that samples B and C suffer from increased ionized-impurity and dislocation scattering which is the dominant scatter mechanism throughout until the spill-over into the AlGaN barrier layer occurs for $V_G > 0.8\,V$. It is assumed that the increased ionized-impurity and dislocation scattering is due to defects caused by the sputter process.

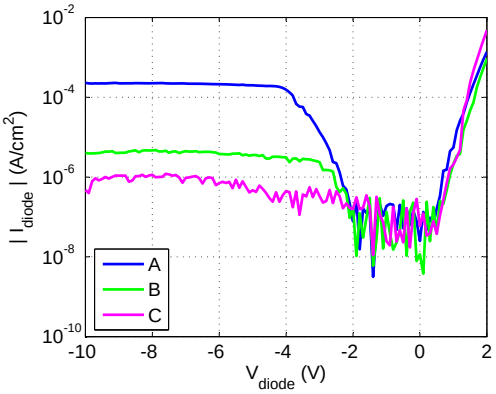

Figure 7.4: IV curves for samples A, B and C measured on $100 \times 100\,\mu m^2$ Schottky-diodes.

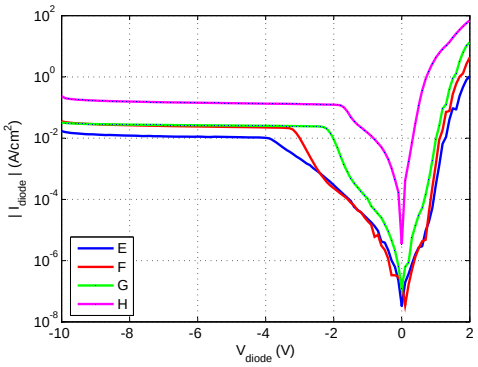

Figure 7.5: IV curves for samples E, F, G and H measured on $100 \times 100\,\mu m^2$ Schottky-diodes.

Figure 7.4 shows the Current-Voltage (IV)-characteristic of diodes for the samples A, B and C. Interestingly the diode reverse current decreases by about two order of magnitude if the barrier is thinned by argon sputtering. A reduction of reverse leakage current caused by 250 V argon sputtering was observed before [86]. However, AlGaN/GaN HEMTs with a thinned barrier layer typically suffer from an increased leakage current [167, 234, 130]. A possible explanation why argon sputtering reduces the reverse leakage current despite a thinned barrier might be as follows: Reverse current densities for Ni/Au Schottky-diodes fabricated on $Al_xGa_{1-x}N$ range between $10^{-4}\,A/cm^2$ and $10^{0}\,A/cm^2$ [253]. Ni/Au Schottky-diodes fabricated on GaN feature reverse current densities of about $10^{-5}\,A/cm^2$ [254]. However, reverse current densities of less than $10^{-5}\,A/cm^2$ are typically expected for Metal Insulator Semiconductor (MIS) diodes fabricated on AlGaN/GaN [255]. Hence the diodes investigated in this work are likely to have an insulation layer between the Ni and the AlGaN barrier. The insulating layer, probably consisting of Ga_xO_y and/or Al_xO_y, is expected to be thicker for those samples which were exposed longer to the argon-sputter procedure.

It is known from literature , that argon ions preferentially remove nitrogen during plasma etching, leading to a formation of N-vacancies in the AlGaN barrier layer [256]. The preferred etching of nitrogen during the sputter process is attributed to the factor of five difference in atomic masses between Ga and N [230], because ion mass is found to be an important factor in the preferential sputtering of nitrogen [257]. Due to the N-vacancies Ga an Al are readily oxidized in the subsequent processing steps leading to a formation of Ga_xO_y and Al_xO_y. In a sum samples which were sputtered longer are likely to exhibit more N-vacancies and consequently will have a denser and thicker Ga_xO_y/Al_xO_y oxide layer leading to a reduced reverse leakage current as observed in this work.

7.2.4 Conclusion

The investigated argon-sputter process features a slow etch rate without suffering from a pronounced etch delay. Although the sputter process was not found to increase the surface roughness of the samples a combined I-V/C-V analysis revealed a reduction of sheet carrier concentration and mobility. The reduction of mobility is attributed to an increased defects density in the barrier layer caused by the sputter process. The reduced reverse gate leakage

caused by the argon sputter process might be explained by the formation of oxides in the barrier layer due to preferential nitrogen sputtering and subsequent oxidation of the excess Ga and Al atoms. Because of strong degradation in mobility the more common approach of a chlorine-based dry etch process was investigated in addition to the argon-sputter recess procedure which is described in the following section 7.3.

7.3 Recessing AlGaN/GaN HEMTs by chlorine-based RIE

This section outlines the Cl_2 based recess process as developed in this work and describes related results.

7.3.1 Experimental

As a first approach the barrier layer of four samples was globally thinned by Cl_2 RIE prior to device processing. In this way the results of this chlorine-based RIE can be compared to the argon-sputter recess experiment, because both process flows are similar. Especially in both cases the RTP step for ohmic contact annealing takes place after the recessing process. In this way potential effects like defect diffusion or crystal structure annealing apply for both cases.

Processing started with an optical lithography leaving one half of four samples covered with AZ5214 resist for reference purpose. The other half of each sample is exposed to a low bias Cl_2/Ar RIE process. Prior to RIE the samples were dipped into an HCl/H_2O (1:2) solution for 1 min in order to remove native surface oxides which are known to cause etch delays [234, 235]. The chamber pressure was set to 20 μbar, the gas flows were 15 sccm each. The ICP power was set to zero, the effective RF-forward power was 24 W, resulting in a self-bias voltage of about -39 V. Etching times were 10 s, 20 s, 30 s and 40 s respectively. It is known from preliminary experiments of this work that the applied etching conditions might lead to an increase of mean surface roughness. AFM revealed a root-mean-square-roughness of 0.27 nm for the un-etched surface and 0.54 nm for the chlorine RIE etched surface. The fourth sample with an etch time of 40 s was over-etched leaving a reference, it the non-etched half of a sample, referred to as E, and three different recess depths, referred to as F (10 s etching time), G (20 s etching time) and H (30 s etching time) in this section.

After RIE the samples were cleaned with acetone and propanol and a 300 W O_2 plasma in a plasma ashing tool. In contrast to the argon experiment described in section 7.2 an extra cleaning procedure in a diluted HCl and HF solution was not carried out, because metallic contaminations are not expected to be caused by the used RIE tool. After global recessing the process flow was according to the one in the argon-sputter experiment. After e-beam marker definition the Ti/Al/Ni/Au ohmic contact were deposited. The RTP step lasted 30 s in N_2 ambient at a temperature of 885°C. The Ni/Au gates were defined by e-beam lithography. A HCl dip of 30 s duration was performed prior to gate metalization. Ni/Au pads were defined by optical lithography.

7.3.2 Results and discussion

Hall-measurements were conducted to study the impact of barrier thinning by chlorine RIE on Hall-mobility μ_{Hall} and sheet carrier concentration n_s. The accordant recess depth were

determined by CV-measurements as it was done in section 7.2. Table 7.2 lists the results of the Hall-measurements for the obtained recess depth. As for the argon-sputter recess experiment both, n_s and μ_{Hall}, decrease with reduced barrier thickness. As outlined in section 7.2 a reduction of the sheet carrier concentration n_s is expected on basis of prior work, e.g. [246].

Label	R_{sheet} $\Omega/\square$	n_s $10^{12}\,\mathrm{cm}^{-2}$	μ_{Hall} $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$	recess depth nm
E	382	8.29	1968	0.0
F	472	7.84	1681	3.0
G	647	6.16	1561	7.5
H	1212	4.12	1235	9.0

Table 7.2: Results of Hall-measurements for recess depth E, F, G and H achieved by chlorine RIE.

Figure 7.5 shows IV-characteristics of diodes for the samples E, F, G and H. In contrast to the diodes which were thinned by argon-sputtering the diode reverse-current of the Cl-recessed diodes increases by about one order of magnitude in comparison to the reference diode E.

Figure 7.6 shows typical CV-curves for the reference E and the different recess depth F, G and H. Due to the reduced barrier thickness the gate capacitance is increased which is accompanied by the expected threshold voltage shift. A detailed drift mobility profile for the chlorine-recessed samples is obtained from combined IV-CV-measurements as shown in figure 7.7. Qualitatively the curves for the drift mobility μ_{drift} are comparable to previous results known from literature [251] or to the curves obtained in the argon-recess experiment described in section 7.2.

The values for the drift mobilities at $V_G = 0\,\mathrm{V}$ depicted in figure 7.7 are lower than the values of the Hall-mobilities listed in table 7.2. However, differences in Hall-mobility and drift mobility have to be considered with care because generally Hall-mobility differs from drift mobility [181] and because the used van-der-Pauw structures do not have a gate metalization in contrast to the HEMTs of this experiment.

7.3.3 Conclusion

In this section the chlorine RIE recess developed in this work is characterized. The chlorine RIE process features a low self-bias of about $-40\,\mathrm{V}$. The etch rate is about 20 nm/min which should be lowered in future optimization steps to enhance the reproducibility of this procedure. The process conditions which are presently applied lead to an increase in mean surface roughness, but stays below 0.55 nm. Unfortunately, the Hall-mobility and the drift mobility reduce, too, but stay above $1200\,\mathrm{cm}^2/\mathrm{Vs}$ and $1000\,\mathrm{cm}^2/\mathrm{Vs}$ for a 9 nm recess, respectively.

7.4 Comparison of recess approaches

It is instructive to compare both recess approaches of this work. Because both experiments, the argon IBE and chlorine RIE recess, were not conducted simultaneously, any differences revealed by a comparative investigation have to be considered with caution. For example,

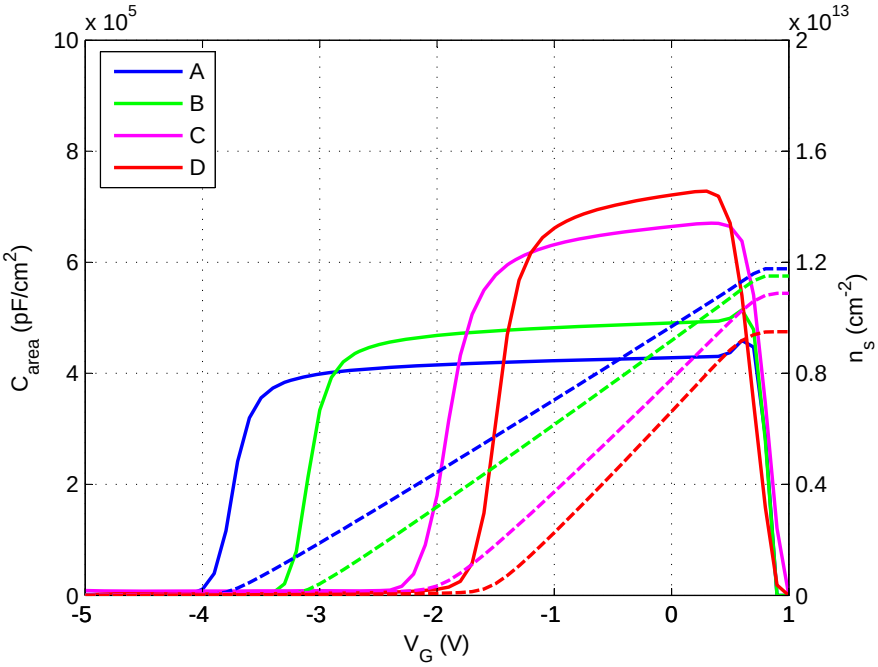

Figure 7.6: Capacitance per unit area C_{area} as determined from C-V-measurements (solid lines) together with the extracted sheet carrier concentration n_s (dashed lines) for recess depths E, F, G and H achieved by Cl_2 RIE, both as a function of applied voltage V_G.

both experiments utilized nominally identical epitaxy material, but the pieces used for the argon recess experiment were taken from another wafer than the samples for the chlorine recess. Hence, even inter wafer deviations would have been to be considered in a strict analysis. In contrast to argon recess experiment the samples of the chlorine recess experiment were not cleaned in a diluted HCl and HF solution after the recess procedure. However, diluted HCl and HF solutions do not etch AlN or GaN crystals at room temperature [240] and are found to cause insignificant changes to AlGaN or GaN surfaces as indicated by AFM [168]. In this sense no detrimental influence on the crystal quality caused by an HCl- or HF-based wet chemical cleaning is expected and therefore they are considered to be of minor relevance in a comparative study. The RTP step used for ohmic contact annealing, which is expected to have a strongest influence on the final crystal quality beside the recess procedure itself, was done after the specific recess etching in both cases under nominally the same conditions. Thus the results of both experiments may be compared to each to a certain degree of accuracy.

A first general difference between the results of the two experiments becomes apparent if the drift mobility as a function of sheet carrier concentration is compared for both reference sample A and E in figure 7.8 and in figure 7.9. For n_s values between 0 and $2 \cdot 10^{12}\mathrm{cm}^{-2}$ the drift mobility increases in both cases due to reduced shielding of ionized impurity [249] in similar way. However, in the case of reference device E of the chlorine recess experiment, the mobility does not surpass the $2000\,\mathrm{cm}^2/\mathrm{Vs}$ boundary in contrast to reference device A, when n_s exceeds $2 \cdot 10^{12}\mathrm{cm}^{-2}$. Thus for $5 \cdot 10^{12}\mathrm{cm}^{-2}$ the drift mobility of reference A is higher than the drift mobility of reference sample E. But for recessed devices there is an opposite situation, i.e. the drift mobility at $n_s = 5 \cdot 10^{12}\mathrm{cm}^{-2}$ is higher for those devices etched with chlorine RIE than for those thinned by sputtering, if the recess depths are taken into account accordingly to table 7.2 and table 7.1. Also

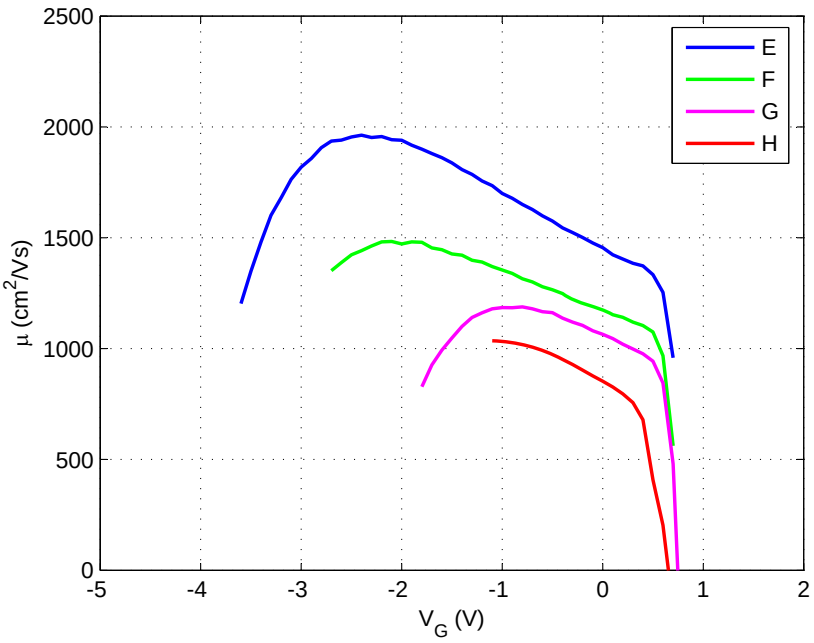

Figure 7.7: Drift mobility for samples E, F, G and H recessed by Cl_2 RIE as a function of applied gate potential V_G.

the values of the Hall-mobilities in table 7.2 are higher than those obtained for argon recessed samples listed in table 7.1. In a sum the chlorine recess procedure causes less degradation to Hall-mobility and to drift-mobility, if sheet carrier concentrations of less than $10 \cdot 10^{12}\mathrm{cm}^{-2}$ are considered. Unfortunately, the chlorine recess samples suffer from pronounced surface roughness and/or interface roughness scattering as indicated in figure 7.9 [258, 249]. The observed surface/interface roughness scattering mechanism [258, 249] is in accordance with the increase of mean-surface-roughness caused by RIE etching, although it should be emphasized that the drift mobility of reference sample E seems to suffer from this mechanism, too.

Because the results presented in figure 7.8 and in figure 7.9 base on measurements at a low V_{DS} value of 30 mV, the output characteristic of two long channel HEMTs corresponding to recess depths C and H are compared in figure 7.10 additionally. As shown in figure 7.10 the drain current I_D at $V_{GS} = -0.5\,\mathrm{V}$ in the argon recess case matches the drain current at $V_{GS} = -1.0\,\mathrm{V}$ for the chlorine case. Considering the CV-measurements (cf. figure 7.2 and figure 7.6) a higher sheet carrier concentration in the argon case than in the chlorine case is expected for these bias conditions, i.e. $n_{s,C}(-0.5\,\mathrm{V}) > n_{s,H}(-1\,\mathrm{V})$. Taking into account the fundamental HEMT equations described in section 3.4 the carrier mobility of the chlorine RIE recessed HEMT has to be higher than the carrier mobility of the argon recessed counterpart for all applied V_{DS} values between 0 V and 10 V. The observation of higher mobility in the case of the chlorine recessed device is especially interesting, if possible scatter mechanisms, caused by defects at the barrier-gate interface, are taken into account, because the distance to this interface is even slightly smaller in case H than in case C. (cf. table 7.1 and table 7.2). The contact resistance R_c (cf. section 3.5) was about 1.3 Ω·mm for recess depth H and about 1.1 Ω·mm for sample C. A systematic improvement of the contact resistance with recess depth, as it may be expected on the basis of literature results, e.g. [130], was not observed in this work. The contact resistance tended to worsen

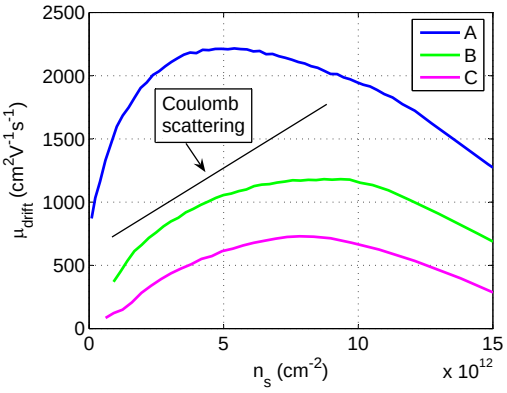

Figure 7.8: Drift mobility for samples A, B and C recessed by argon-sputtering as a function of sheet carrier concentration n_s.

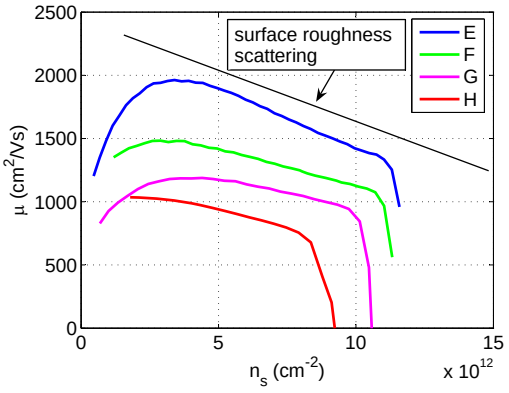

Figure 7.9: Drift mobility for samples E, F, G and H recessed by Cl_2 RIE as function of sheet carrier concentration n_s.

from about 0.6 Ω·mm to 1.2 Ω·mm with increased recess depth in both experiments. A clear systematic trend for R_c and ρ_c as a function of recess depth could not be extracted in this work.

7.5 Local chlorine-based RIE recess

Based on the discussion in section 7.4 the chlorine RIE recess process was preferred for experiments where HEMTs are locally recessed prior to gate metalization.

7.5.1 Device fabrication

The device fabrication started with a marker layer as developed in this work, followed by ohmic contact fabrication and mesa insulation similar to the standard HEMT technology. The epitaxial material used was same as for the Γ-gate experiment, i.e. it consists of a 2 μm GaN buffer, a 1.25 nm AlN spacer and a $Al_{0.29}Ga_{0.71}N$ unintentionally doped barrier layer of 20 nm thickness. Prior to gate metalization the HEMTs where recessed with the chlorine RIE process developed as described in section 7.3. One PMMA resist layer was used as etch mask and as mask for the gate metalization definition, so that the metalization was self-aligned with the recess etch profile. The effective RIE forward power was about 25 W, the self-bias voltage was −30 V. Chamber pressure was 20 μbar. The Cl_2 and argon gas flows were 15 sccm each. Gate metalization consisted of 25 nm Ni and 375 nm Au. The gate width W of the HEMTs was reduced to $2 \times 30\,\mu$m in order to achieve a high f_{max} value as shown in figure 7.18. The source-drain spacing was reduced to about 1 μm as depicted in figure 7.11. Non-recessed reference devices were processed in parallel in the direct vicinity of the chlorine-recessed devices in order to allow for comparing both devices.

Figure 7.12 shows a STEM image of a locally chlorine RIE recessed HEMT with an L_G of about 370 nm. The placement of the gate within the recessed barrier layer is clearly visible. In order to get an impression of the barrier-gate interface quality TEM pictures were taken and are shown in figure 7.13 and figure 7.14. Especially figure 7.14 illustrates

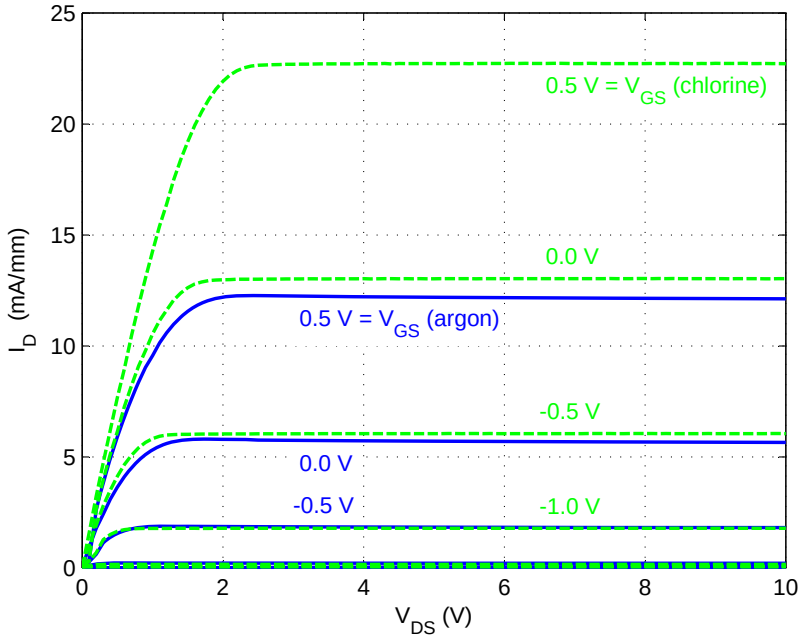

Figure 7.10: Comparison of output characteristics of sample C (argon-recessed, solid lines) and samples H (chlorine-recessed, dashed lines) as a function of applied gate-source voltage V_{GS}.

two aspects which are already indicated by results presented in section 7.3. Firstly, a good crystal quality of the remaining 10 nm barrier is maintained despite the applied chlorine recess procedure. Secondly, the interface of the AlGaN barrier to the polycrystalline Ni is relatively rough, potentially leading to increased surface roughness scattering.

7.5.2 Results of DC- and RF-characterization

Figure 7.15 compares the input characteristic of a chlorine recessed HEMT as depicted in figure 7.11 to a HEMT of the same dimensions fabricated on the as-grown material. First of all a clear threshold voltage shift can be observed in figure 7.15. Secondly, the chlorine recessed HEMT suffers from a larger off-current than the reference HEMT, what is attributed to higher gate reverse leakage current, as depicted in figure 7.16.

Although the recessed HEMT exhibits a lower drain-current at $V_{GS} = 0\,\mathrm{V}$, it achieves a much higher extrinsic mutual transconductance $g_{m,ext}$ than the reference device what it shown in figure 7.19. While the HEMT fabricated on the as-grown material achieves a maximum $g_{m,ext}$ of about 280 mS/mm, the transconductance of the chlorine RIE recessed HEMT surpasses the 400 mS/mm boundary. The value of 400 mS/mm ranges in the vicinity of the highest values for the extrinsic transconductance of AlGaN/GaN HEMTs as known from literature [129, 130, 169, 259, 260, 261].

Figure 7.17 compares the output characteristic of a recessed and as-grown 2x30 μm HEMT. Both devices show a good pinch-off behavior with an output transconductance of about 5 mS/mm in saturation.

The chlorine recessed HEMT and a reference sample were also compared regarding their RF-capabilities. Figure 7.20 shows the RF-data for both cases. The bias points for the

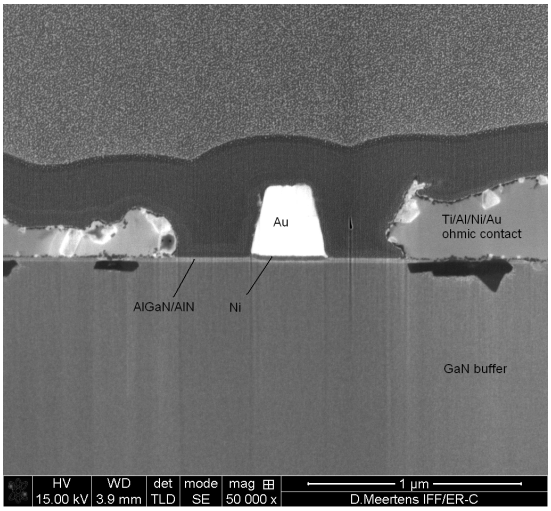

Figure 7.11: SEM picture of HEMT cross section. The device is locally recessed by Cl_2-based RIE.

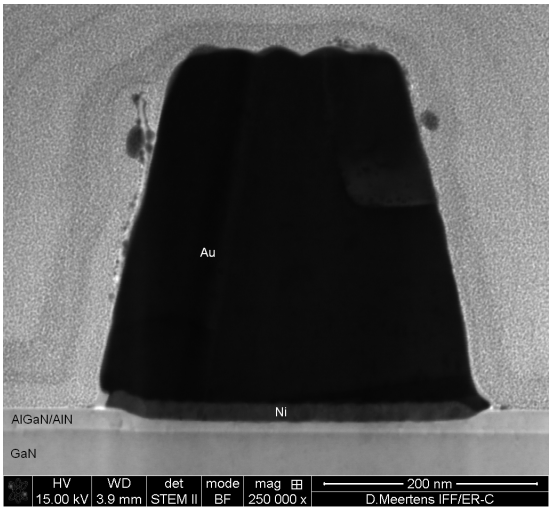

Figure 7.12: STEM picture of HEMT cross section. The device is locally recessed by Cl_2-based RIE.

recessed HEMT and the non-recessed HEMT are $(-1.5/6)$ V and $(-3.1/8)$ V for maximum f_T and $(-1.5/12)$ V and $(-3.2/12)$ V for maximum f_{max}, respectively. The gate length L_G for both devices is 370 nm. Hence the recessed HEMTs of this work achieve an f_T of 35 GHz, an f_{max} of about 105 GHz and consequently an $f_T \cdot L_G$ product of 13 GHz and an f_{max}/f_T ratio of 3.0. Assuming a saturation velocity of $1.1 \cdot 10^5$ m/s an electron transit frequency f_τ of about 47 GHz is expected for a device with 370 nm gate length according to the discussion in section 3.4.

In a sum the experimental data show, that devices subjected to the Cl-based recess procedure of the work deliver state-of-the-art DC- and RF-performance. Because devices with an L_G of 370 nm on a 21 nm barrier are at the borderline where AlGaN/GaN HEMTs start to suffer from short-channel effects, a clear benefit of applied recess-procedure is expected for gate-length of about 150 nm, as in this way a high aspect ration of about 15 can be maintained. Hence in future work the 2x30 μm HEMT should be improved by replacing the gate used by a free-standing T-gate or Γ-gate.

7.6 Summary

In this chapter two different approaches of recessing AlGaN/GaN HEMTs are presented. The first approach is recessing by argon sputtering. Recessing by argon sputtering features a slow etch rate and low material selectivity due to the absence of a chemical etch component. During argon recessing the mean surface roughness is not found to increase.Argon-recessed HEMTs exhibited a reduced gate leakage current what might be explained by an N-deficient and subsequently oxidized sites in the barrier caused by argon-sputtering and processing. Because the argon-sputter processed caused a clear reduction of mobility due to ionized impurity scattering a second recess approach was investigated in this work and the related results are presented.

The second approach is a low-bias and low-power Cl_2/Ar RIE recess. The Cl_2 RIE recess presents itself as a low-damage recess procedure, clearly less subjected to ionized impurity scattering than the argon-sputter recess approach. However, the Cl_2 recess developed in

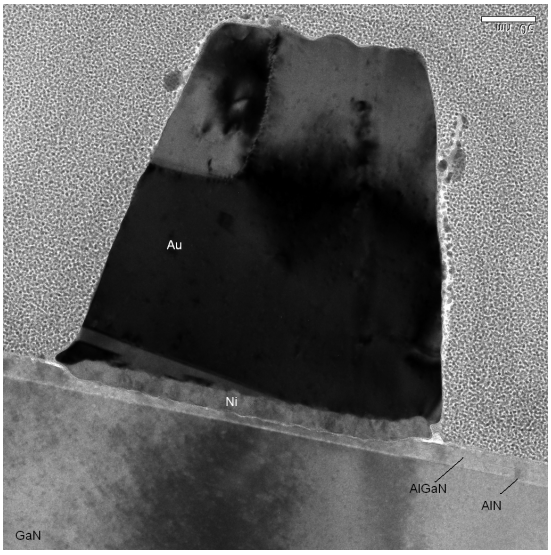

Figure 7.13: TEM picture of HEMT cross section. The device is locally recessed by Cl_2-based RIE.

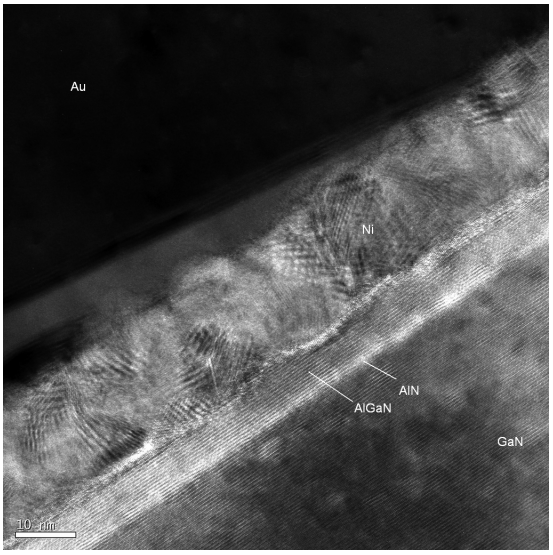

Figure 7.14: TEM picture of HEMT cross section. The device is locally recessed by Cl_2-based RIE.

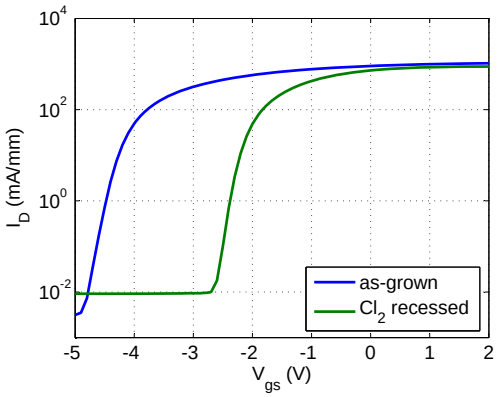

Figure 7.15: I_D for a locally recessed device and for a device fabricated on as-grown material. $V_{DS} = 5\,\mathrm{V}$.

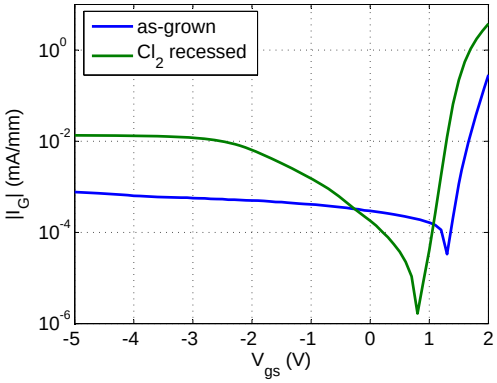

Figure 7.16: I_G for a locally recessed device and for a device fabricated on as-grown material. $V_{DS} = 5\,\mathrm{V}$.

this work increases the mean surface roughness during recessing. Consequently, HEMT recessed by the Cl_2 RIE process, suffer from reduced mobility due to surface/interface roughness scattering, which is only relevant for high sheet carrier concentrations around $10^{13}\,\mathrm{cm}^2$. Also an increased gate reverse leakage was found for Cl_2 recessed HEMTs in comparison to non-recessed counterparts, which can be explained by a the reduction of the barrier thickness. In a sum the Cl_2 RIE process is regarded as the more appropriate recess approach because of its low-damage character.

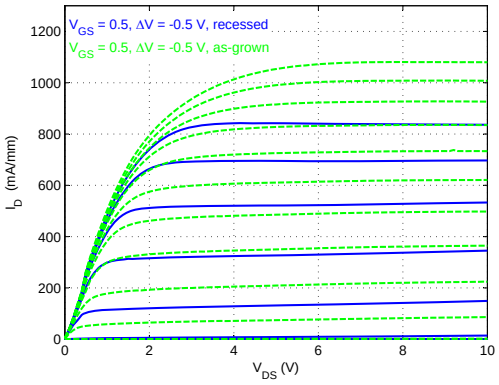

Figure 7.17: Comparison of output characteristics of 2x30 μm HEMTs, recessed and as-grown.

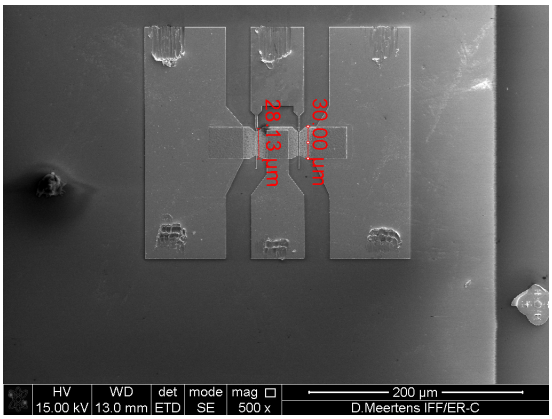

Figure 7.18: SEM picture of a 2x30 μm HEMT.

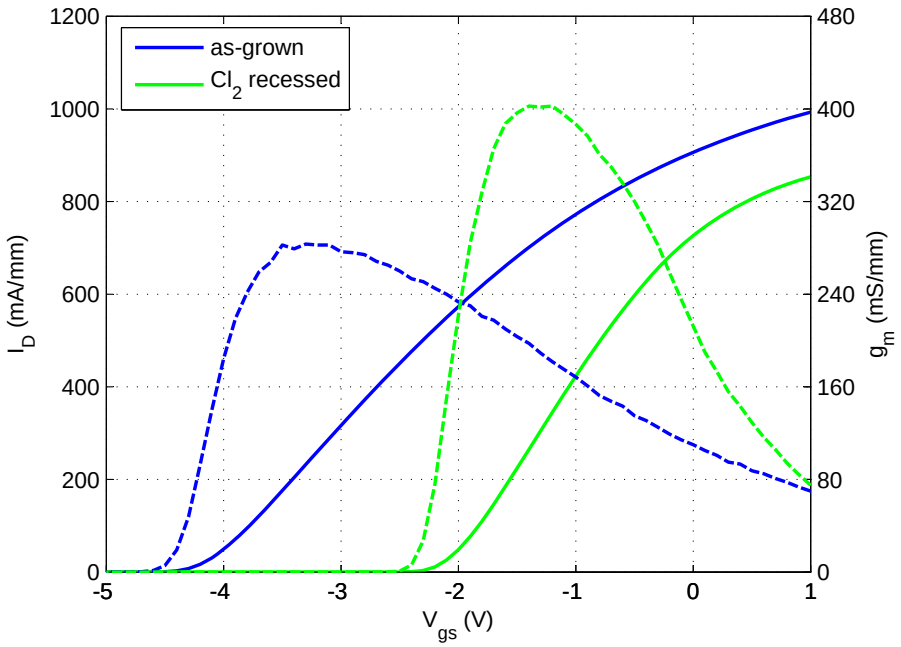

Figure 7.19: Comparison of recessed to as-grown HEMTs. While the non-recessed device exhibits a higher I_D (solid lines), the recessed HEMT achieves a maximum g_m of more than 400 mS/mm (dashed lines). $V_{DS} = 5$ V.

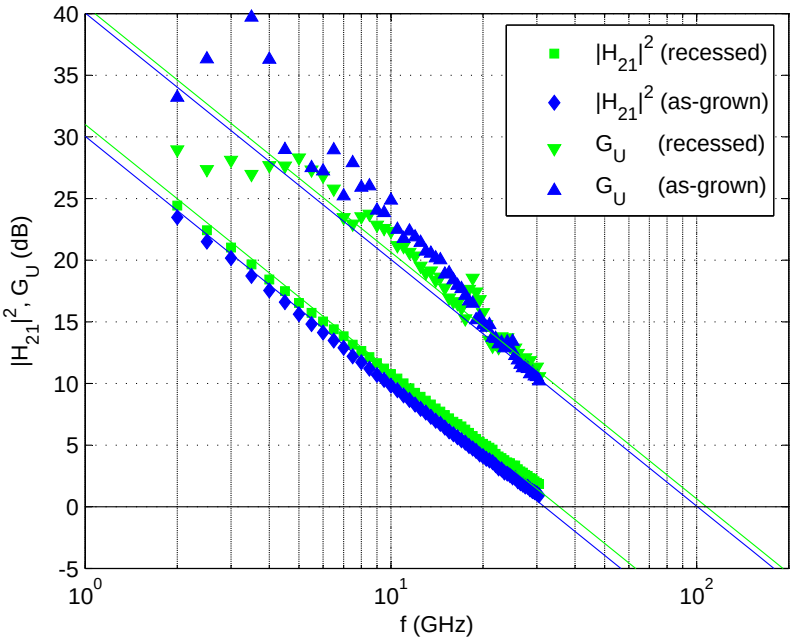

Figure 7.20: Current-gain $|{H_{21}}^2|$ and Unilateral Power Gain G_U for a Cl_2 recessed HEMT and HEMT processed on as-grown material. The bias points for the recessed HEMT and the non-recessed HEMT are $(-1.5/6)\,\mathrm{V}$ and $(-3.1/8)\,\mathrm{V}$ for maximum f_T and $(-1.5/12)\,\mathrm{V}$ and $(-3.2/12)\,\mathrm{V}$ for maximum f_{max}, respectively.

CHAPTER 8

Oscillator Structures

This chapter begins with some general considerations regarding the design of the RF-power oscillators. The objective of the first section 8.1 of this chapter is to explain why a MMIC is the most suitable design approach if a compact, light and hence cheap RF-source should be built. In the subsequent section 8.2 the results of a literature research regarding AlGaN/GaN HEMT based MMIC oscillators are presented. In the remainder of this chapter the design of interdigital capacitances and the oscillator structures are described and the corresponding experimental results are outlined.

8.1 General considerations regarding power oscillator design

An oscillator is a DC- to RF- energy converter, i.e. it generates electromagnetic radiation at a certain frequency spectrum if a DC-bias is applied to its terminals. Microwave and millimeter-wave power oscillators are typically used as RF-sources in communication, radar and electronic warfare systems. As already mentioned in the introducing chapter 1 traditional microwave oscillator sources are TWT like the klystron, the BWO, the magnetron and the gyrotron. Although these traditional RF-sources are able to deliver very high RF-output-power at high frequencies, e.g. 200 kW continuous-wave at 106 GHz or 120 kW pulsed at 375 GHz [27], they are replaced in many fields of application by solid-state power oscillators. The reason for this replacement is that sources based on solid-state devices feature low production cost, small size and weight, low operating voltages and high reliability in comparison to the traditional sources [13].

Solid-state power oscillators employ a variety of active elements which may be categorized in three-terminal devices, i.e. transistors, and two-terminal devices, i.e. diodes. Three-terminal devices dominate power applications up to approximately 30 GHz, while two-terminal devices are typically used at millimeter-wave frequencies [13]. However, solid-state oscillators employing InGaP/InGaAs HBTs as three terminal devices can also achieve a fundamental oscillation frequency of 146 GHz with an output power of about −18 dBm [262].

Two basic approaches may be considered for the design of a solid-state oscillator: the cavity-based approach and the approach of designing the oscillator as a planar Integrated Circuit (IC), i.e. as a Microwave Integrated Circuit (MIC) or MMIC. The device type strongly influences the decision which approach to take. Two-terminal devices are generally employed in cavity based setups. Three-terminal devices are readily fabricated in a planar process technology. Table 8.1 lists the advantages and disadvantages of the cavity-based approach and the planar IC approach according to reference [13].

As already outlined in this section solid-state oscillators are the preferred RF-sources today because they feature low production costs, small size and weight in comparison to traditional tubes. Sticking to the paradigm that approaches, which lead to low cost, small size and light weight solutions, are generally preferred the planar IC is clearly beneficial

approach	fabrication skill	costs	size	weight
planar (MIC, MMIC)	low	low	$\approx 10^{-2} - 1\,\mathrm{cm}^3$	light
cavity-based	high	high	$\approx 10 - 20\,\mathrm{cm}^3$	$\approx 250\,\mathrm{g}$

Table 8.1: Advantages and disadvantages of the cavity-based approach and the planar IC approach for the design of solid-state power oscillators according to [13].

in comparison to the cavity-based approach according to table 8.1. According to reference [13] one draw-back, a planar IC has in contrast to cavity oscillators, is lower power handling capability. But considering that table 8.1 was published in 1992 [13], the nitride material system as basis for a MIC or a MMIC was probably not taken into account in those days. As discussed in the introduction [13] the nitride material system is the semiconductor material of choice if high-power and high-frequency devices and circuits are objected.

While the benefits of a planar IC over a cavity-based circuit are clear by now the last decision to be made is whether to choose a MIC or a MMIC approach. MIC typically exhibits a dielectric resonator which is coupled to the planar circuit in order to achieve a better stability of the oscillation frequency. However, if the requirements regarding the oscillator output can be met with a pure MMIC a further reduction of size and weight in comparison to a MIC is possible. Additionally the costs per MMIC are expected to be less than the costs for a MIC, if more than 100 circuits are to be manufactured [263].

Consequently a MMIC approach is chosen for the oscillator design of this work. Coplanar waveguides are chosen as on-chip transmission lines, because they allow for simple on-wafer measurements techniques and they do not require sophisticated backside processing and a related via-hole technology whose development is expected to be extraordinarily challenging in the case of SiC substrates. A detailed discussion of the advantages and disadvantages of a coplanar waveguide technology in comparison to other transmission line concepts, like for instance the microstrip lines, is given in reference [264].

8.2 Overview over AlGaN/GaN MMIC oscillators

Table 8.2 lists some basic characteristics of AlGaN/GaN MMIC oscillators as found in literature. Beside the fundamental frequency of oscillation f_0 and the achieved output power, the gate length L_G, the gate width W as well as the f_T and f_{max} of the used HEMTs are given in the case these parameters could be extracted from the specific reference. All listed output powers are obtained directly from the oscillator circuit without being amplified by an additional amplifier buffer stage. Nevertheless output powers in excess of 3 W are achieved at a frequency of 9 GHz [265] by using a $10 \times 150\,\mu$m AlGaN/GaN HEMT as active device. A $4 \times 125\,\mu$m AlGaN/GaN HEMT with a field-plate gate achieved an output power of about 1.9 W. Both results demonstrate again the high-power and high-frequency capabilities of AlGaN/GaN HEMTs.

Only a few oscillator circuits with a frequency of oscillation greater than 10 GHz could be found in literature. Until the year 2010 no GaN HEMT oscillators has been reported with a frequency higher than 60 GHz [274]. At the time of writing a sinusoidal output at 74.5 GHz, which is assumed to be the fundamental frequency in this case, is regarded as the highest frequency delivered by a GaN HEMT oscillator today according to table 8.2. By the means of an additional two-stage buffer Nakasha et al. could build an AlGaN/GaN

No.	f_0	P_{out} (dBm)	P_{out} (mW)	L_G	W	f_T (GHz)	f_{max} (GHz)	reference
1	4.2	22.90	195.0	0.70	200	–	–	[266]
2	5.0	32.80	1905.5	0.70	500	15	–	[267]
3	5.3	20.50	112.2	0.70	200	20	–	[268]
4	8.2	28.00	631.0	–	–	–	–	[269]
5	9.0	35.00	3162.3	0.15	1500	–	–	[265]
6	9.6	32.31	1700.2	0.25	1500	27	36	[270]
7	9.9	20.00	100.0	0.25	150	40	100	[271]
8	13.3	10.00	10.0	0.20	220	50	50	this work
9	39.1	25.00	316.2	0.20	400	–	–	[272]
10	53.0	11.00	12.6	0.20	400	65	–	[273]
11	74.5	3.38	2.2	0.12	100	70	240	[274]

Table 8.2: Characteristics of various AlGaN/GaN MMIC oscillators as known from literature.

HEMT based RF-source which delivers 85 mW at 70.75 GHz. As discussed in section 1.2 of the introduction state-of-the-art THz-multiplier-chains require approximately 100 mW as feeding power at a frequency range of $94 - 106$ GHz [32]. Thus the buffered oscillator circuit presented by Nakasha et al. [274] comes close to the requirements imposed by a first stage of a THz-multiplier-chain. Table 8.2 does not consider all figures of merit which might be relevant for bench marking an oscillator circuit. Other common figure of merits for an oscillator, which are not directly focused in the preliminary investigation of this work, are: DC to RF conversion efficiency, phase noise, tune-ability, bias-point stability, temperature stability and mechanical robustness.

8.3 Design of interdigital feedback capacitance

Interdigital capacitors are intensively used in microstrip and coplanar technology to couple an RF-signal from one transmission line to another which is biased at a different potential. The capacitor itself is defined as the multi-finger structure between two reference planes RP_1 and RP_2 as depicted in figure 8.1. Also indicated in figure 8.1 are the various geometry parameters which might be altered to modify the coupling behavior of the interdigital capacitor. The number of fingers is one of the most fundamental parameters which determine the properties of the capacitor. Beside the number of fingers their spacing S_f, their width W_f and their length L_f are important design parameter. Of course, the gap width at the finger ends S_e influences the signal transmission, too. The parasitic coupling of the interdigital structure to the ground plane of the coplanar wave guide is strongly determined by the gap between ground plane and the outer fingers of the interdigital capacitor denoted as S_g in figure 8.1 [264]. The metalization thickness t_m might vary between a few hundred nanometers to about 3 μm if a galvanic process is employed and also determines the actual characteristic of the interdigital capacitor. In a sum there are several parameters to alter the behavior of the capacitor.

A typical interdigital capacitor can be described by a simple lumped element equivalent circuit shown in figure 8.2 [27]. For applications in the millimeter-wave range the model has to be augmented by taking into account distributed effects and a extended equivalent circuit which consists of more elements [264].

Because for this work a well-established design bibliography, which determines the values

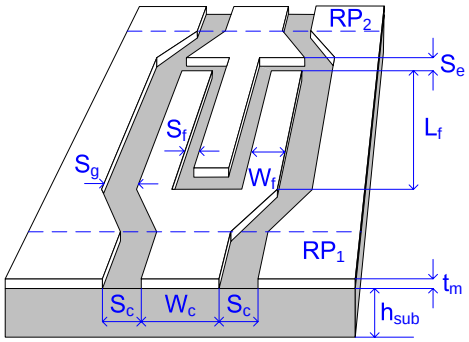

Figure 8.1: Sketch of an inter-digital capacitor in coplanar technique with labeling of relevant dimensions of the capacitor layout.

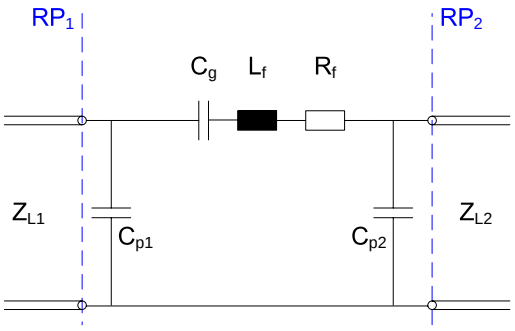

Figure 8.2: Lumped element equivalent circuit for a coplanar inter-digital capacitor.

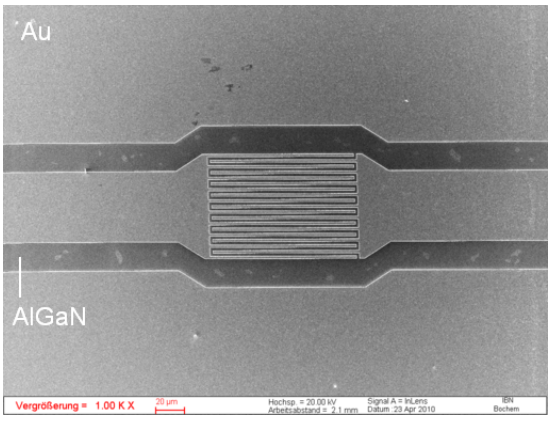

Figure 8.3: SEM picture of inter-digital capacitor with dimensions according to layout A2.

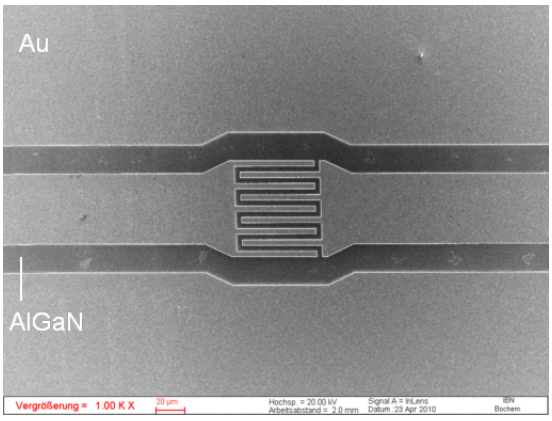

Figure 8.4: SEM picture of inter-digital capacitor with dimensions according to layout B3.

of the lumped elements on the basis of the geometrical parameters of figure 8.1, was not available the behavior of the feedback capacitors was determined by measuring the corresponding S-parameters. To get an idea what dimensions of a feedback capacitor are required to make it applicable at a certain frequency range six different interdigital capacitors were fabricated with their dimensions according to table 8.3. The input and output port of the interdigital capacitor were extended by coplanar transmission lines in order to consider transmission line losses in addition. The lengths of the coplanar L_{cpw} transmission line extensions are listed in the corresponding column of table 8.3. Figure 8.3 and figure 8.4 show SEM pictures of the fabricated interdigital capacitors A2 and B3, respectively.

Figure 8.5 and figure 8.6 the magnitude and the phase of the transmission coefficient S_{21} as a function of frequency for various inter-digital capacitors are plotted, respectively. Accordingly the capacitor B3 shows the strongest the damping of 5 dB or more over the whole measured frequency range. The coupling could readily be increased by either increasing the number of fingers adjoined with a reduction of S_f or by increasing the finger length L_f. Consequently the capacitor A1 with 19 fingers and a finger length of 160 μm exhibits

	A1	A2	A3	B1	B2	B3
S_f (μm)	2	2	2	4	4	4
W_f (μm)	2	2	2	4	4	4
S_g (μm)	20	20	20	40	40	40
S_e (μm)	2	2	2	4	4	4
No. of fingers	19	19	19	9	9	9
L_f (μm)	160	110	60	160	110	60
L_{cpw} (μm)	1045	1070	1095	1045	1070	1095

Table 8.3: Dimension for six different layouts of inter-digital coplanar capacitors. The metalization thickness t_m is 370 nm for all layouts. The calculated coupling capacitance $C_{p,calc}$ is also listed for each capacitor.

the best transmission properties. But also capacitor A1 causes a relatively high damping of about 4 dB at 10 GHz which must be compensated by a sufficiently high output power of the active device in the final circuit environment.

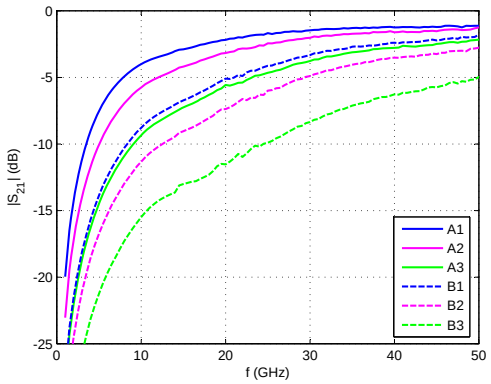

Figure 8.5: Magnitude of the transmission coefficient S_{21} as a function of frequency for various inter-digital capacitors.

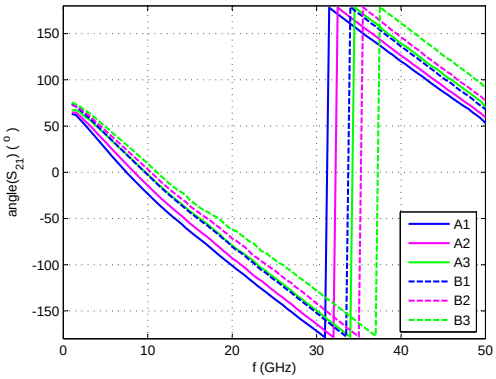

Figure 8.6: Phase of the transmission coefficient S_{21} as a function of frequency for various inter-digital capacitors.

For a better understanding the interdigital capacitor A1 was modeled. Basis for the model was the simple lumped element equivalent circuit in figure 8.2. The capacitive elements C_{p1} and C_{p2} were assumed to be 15 fF each. C_g is estimated to be about 140 fF. L_f was considered to be 100 pH and R_f was considered to be 15 Ω. The coplanar wave guides are modeled as simple lossless 50 Ω transmission lines with a phase velocity of $3 \cdot 10^8/\sqrt{\epsilon_{r,eff}}$ m/s, where $\epsilon_{r,eff}$ is the effective permittivity of about 5.4 for GaN on SiC [1].

Figure 8.7 shows that the modeled and measured S-parameters are in good agreement with each other.

8.4 Oscillator structures

Motivated by the discussion of section 8.1 this work focuses a MMIC approach for the oscillator with a GaN HEMT as active three-terminal device. In order to maintain a

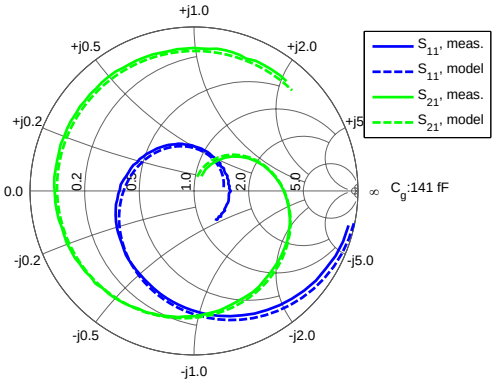

Figure 8.7: Modeled and measured S-parameters for interdigital capacitor A1. f = 1..50 GHz.

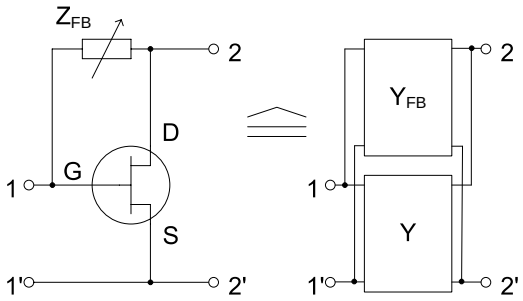

Figure 8.8: Schematic of the investigated oscillator structure of this work linked to the corresponding Y-parameters.

constant oscillation some of the output RF-signal power generated by the active device needs to be fed back to its input port. Generally this feedback can be provided by means of a parallel or a serial feedback structure [27, 275]. In this work the parallel feedback approach is investigated while the HEMT as active device is used in a common source configuration. Figure 8.8 shows the schematic of the parallel feedback approach according to reference [276]. The schematic itself can be modeled as two two-port networks in parallel, where the two-port network $\boldsymbol{Y}$ describes the FET and the two-port network $\boldsymbol{Y_{FB}}$ corresponds to the feedback circuit as depicted in figure 8.8.

The RF-feedback from the drain-source terminal, i.e. the output, to the gate-source terminal, i.e. the input, is provided by a 50 Ω coplanar transmission line , with $W_c = 50\,\mu$m and $S_c = 24\,\mu$m, and an interdigital capacitor (cf. section 8.3).

Figure 8.9 shows a microscope picture of a typical oscillator structure investigated in this work. For the sake of simplicity the design and fabrication of bias networks was omitted. The bias was applied through common RF-probes which were connected to external bias-T-circuits with a 50 Ω-transmission-lines. While the transmission line at the gate side of the HEMT was left open, the transmission line at the drain side was connected to a spectrum

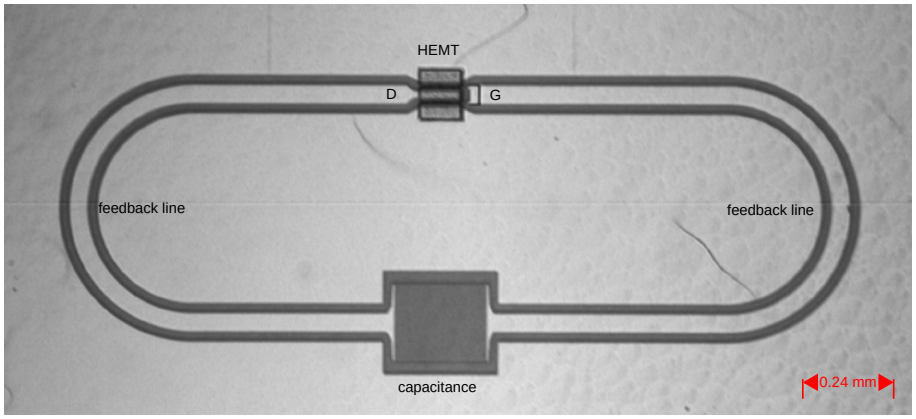

Figure 8.9: Microscope picture of a typical oscillator structure of this work.

analyzer. The interdigital feedback capacitor was made of 51 fingers and was designed such that $S_f = W_f = S_e = 2\,\mu$m (cf. figure 8.1). The finger length L_f was 240 μm and the metalization thickness t_m was about 320 nm. A microscope picture of this interdigital capacitor is shown in figure 8.15. The chosen capacitor was not separately characterized. Its coupling capacitance C_g is expected to increase approximately linearly with the number of fingers and the finger length [27]. Accordingly the coupling capacitance C_g is estimated to be larger than the 140 fF of capacitor A1 by a factor of about $51/19 \cdot 240/160 \approx 4$, i.e. $C_g = 4 \cdot 140\,\text{fF} = 560\,\text{fF}$.

According to basic oscillator theory [27] the real part of the output impedance of oscillator must compensate the real part of the load circuit for oscillation to occur. In this work this condition corresponds to $\Re(Z_{22}) + 50\,\Omega = 0$. Additionally the imaginary parts have to compensate, i.e. $\Im(Z_{22}) = 0$ for the set up investigated in this work. The oscillator structures were simulated for four different feedback circuits. All feedback circuits exhibited the same interdigital capacitor as described in this section. It was modeled with a simple equivalent circuit according to figure 8.2 with $C_g = 560\,\text{fF}$ and $L = 100\,\text{pH}$. The parasitic elements are assumed to be $C_{p1} = C_{p2} = 40\,\text{fF}$ and $R_f = 20\,\Omega$. The coplanar wave guides are modeled as simple lossless 50 Ω transmission lines with a phase velocity of $3 \cdot 10^8/\sqrt{\epsilon_{r,eff}}\,\text{m/s}$. A detail modeling of the feedback structure including parameter extraction maybe part of future work. The phase of the feedback loop can be altered by the dimensioning of the feedback capacitance or by adjusting the length of the feedback line. In this work a variation of feedback capacitance is not investigated but the influence of the length of the feedback line is studied. The length of the coplanar feed back line L_{cpw} of the oscillator layout depicted in figure 8.9 was varied in order to modify the phase of the feedback loop. The chosen lengths for oscillator structure A, B, C and D are listed in table 8.4.

Oscillator	f_0 (GHz)	f_2 (GHz)	L_{cpw} (μm)
A	9.78	29.35	5401
B	10.91	32.82	4601
C	11.53	34.66	4201
D	13.29	39.88	3601

Table 8.4: Oscillator structures A, B, C and D with different length of coplanar feedback line L_{cpw} and their measured fundamental frequency f_0 as well as their harmonic frequency f_2 corresponding the three times f_0.

The HEMTs which were employed as active devices in the oscillator structures had a gate width of $2 \times 110\,\mu$m. The gate-length L_G was about 200 nm. The used HEMTs exhibited a balanced f_T and f_{max} of about 50 GHz each. The S-parameters of such a HEMT were used to model the two-port network $\boldsymbol{Y}$ as depicted in figure 8.8. After adding up both two-ports in parallel the resulting output impedance of the circuit can be investigated.

Figure 8.10 shows the simulated output impedance Z_{22} for oscillator structure A, B, C and D as function of frequency. The minimum $\Re(Z_{22})$ for each structure is between $-50\,\Omega$ and $-60\,\Omega$, so that the resistive load of 50 Ω imposed by the spectrum analyzer can be compensated. Also the second oscillator condition is fulfilled as $\Im(Z_{22})$ is about zero for the frequency where $\Re(Z_{22})$ achieves its minimum. Figure 8.11 shows the simulated output impedance in the complex plane. The square markers indicate the minimum of $\Re(Z_{22})$. Hence the fundamental frequency of oscillation for oscillator A, B, C and D is expected to be at 10 GHz, 11 GHz, 11.5 GHz and 12.5 GHz, respectively.

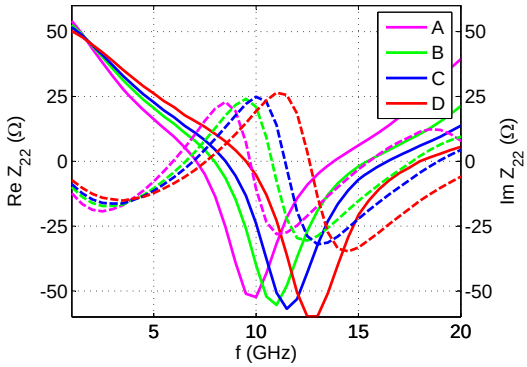

Figure 8.10: Modeled output impedance Z_{22} for oscillator structure A, B, C and D as function of frequency. Dashed lines correspond to $\Im(Z_{22})$.

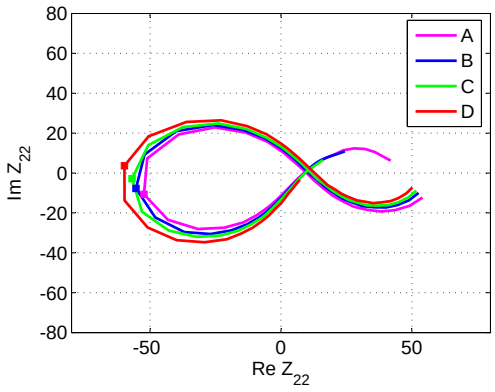

Figure 8.11: Modeled output impedance Z_{22} for oscillator structure A, B, C and D. Marker indicate the minimum of $\Re(Z_{22})$.

Table 8.4 lists four different oscillator structures A to D with their measured fundamental frequency of oscillation f_0 and the corresponding length of the coplanar feedback line L_{cpw}.

Figure 8.12 shows the measured spectra of the four oscillator structures. While the oscillators typically achieved an initial output power of about 10 dBm, i.e. 10 mW, their power performance stabilized during operation to a value of about 8 dBm. Figure 8.13 shows the peak of oscillator D measured with an increased resolution band width of 30 kHz. The margin between the peak of the harmonic output and the remaining spectrum is 30 dB.

The fabricated oscillator structures also generated RF-output power at the specific harmonic frequencies. Figure 8.14 shows the spectrum of the oscillator A, B, C and D from 28 GHz to 40 GHz. The peaks correspond to the second and third harmonic of the fundamental frequency of oscillator A and to the second harmonic of the fundamental frequency of oscillator B, C and D, respectively. In this way signal generation at the mm-wave regime could be achieved. The signal with the highest frequency of oscillation which was measured in this work achieved an output power of −20 dBm at 39.9 GHz. The highest frequency, which was measurable by the spectrum analyzer used, is 40 GHz.

In order to study the dependence of the fundamental frequency f_0 on the length of the feedback line L_{cpw} the corresponding values were plotted and linearly interpolated as shown in figure 8.16. The dependence of $f_0(L_{cpw})$ is governed by (8.1).

$$f_0 = 37.7\,\text{GHz} \cdot \text{mm}/L_{cpw} + 2.7\,\text{GHz} \tag{8.1}$$

Consequently an oscillator with a fundamental frequency of about 40.0 GHz is expected for an L_{cpw} of 1 mm, if the employed HEMT can deliver sufficient gain at this frequency. The dependence of f_0 on the length of the feedback line L_{cpw} originates from the phase condition of the parallel feedback approach. A steady-state oscillation requires the total loop gain to be unity and the signal feedback from the output to the input port of the active device to be constructive, i.e. in phase [107]. Thus adjusting L_{cpw} is a simple way to alter the phase condition of the oscillator.

In a sum the observed dependence of the fundamental frequency on the length of the

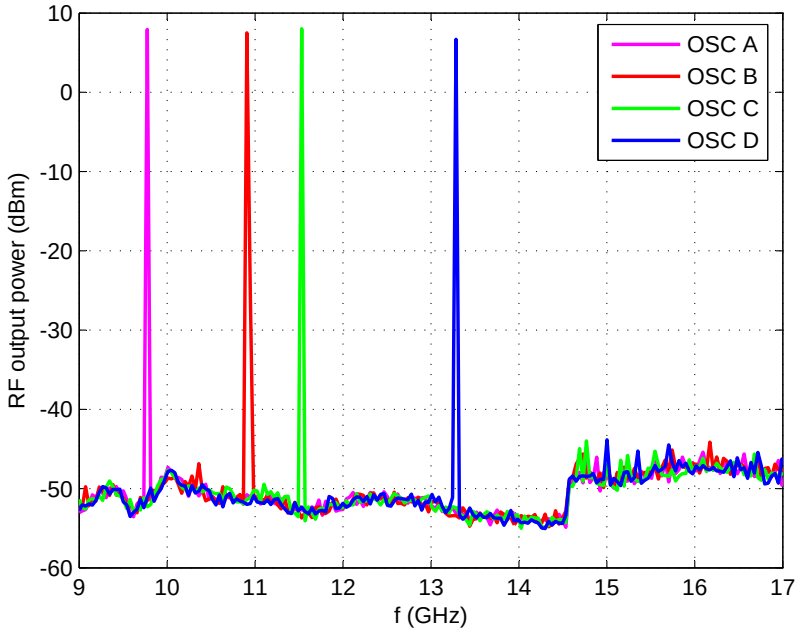

Figure 8.12: Spectra of four oscillators A, B, C and D. Spikes correspond to fundamental oscillator frequency.

feedback line is well in accordance to the simulations of the oscillator structures discussed in this section. More detailed simulations considering large signal behavior the active device and/or electromagnetic-field simulations of passive components maybe considered in future work.

8.5 Summary

In this chapter the design and the corresponding experimental results of the oscillator of this work are presented. A fundamental frequency of oscillation of 13.3 GHz was achieved which is one of the highest found in literature. But its output power of 10 mW is relative low in comparison to other AlGaN/GaN HEMT oscillators operating in the spectrum around 10 GHz and leaves room for improvement. A measured output of about -20 dBm at 39.9 GHz represents the successful generation of a mm-wave signal.

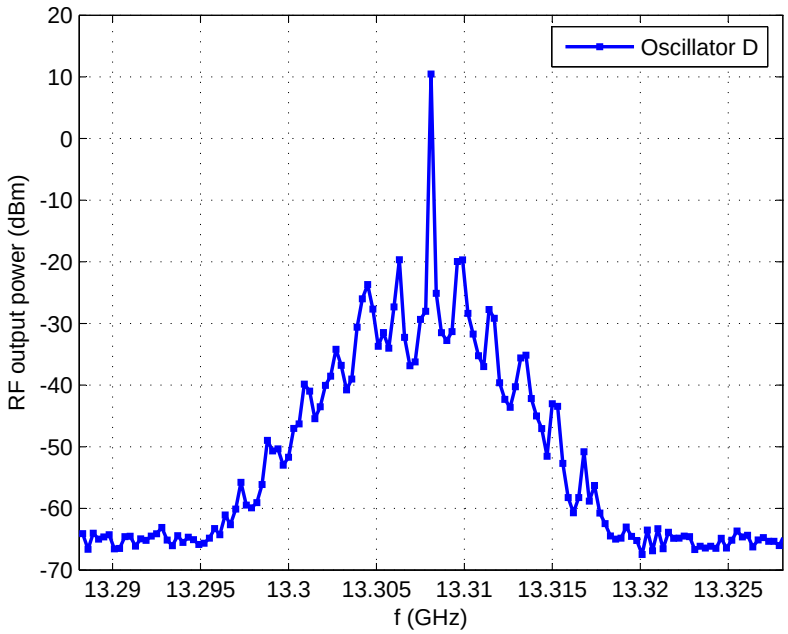

Figure 8.13: Spectra of oscillator D. The fundamental frequency f_0 is shown.

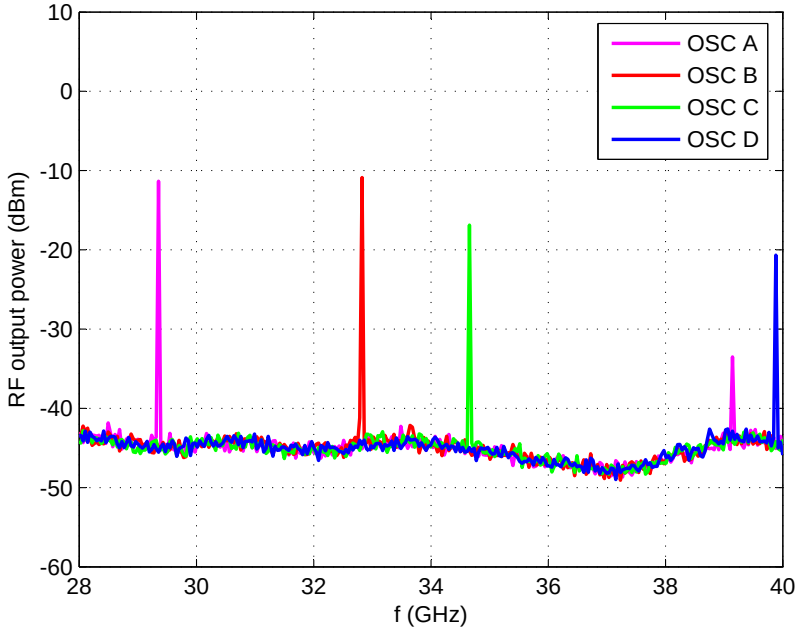

Figure 8.14: Spectra of four oscillator A, B, C and D. Spikes correspond to the second and third harmonic.

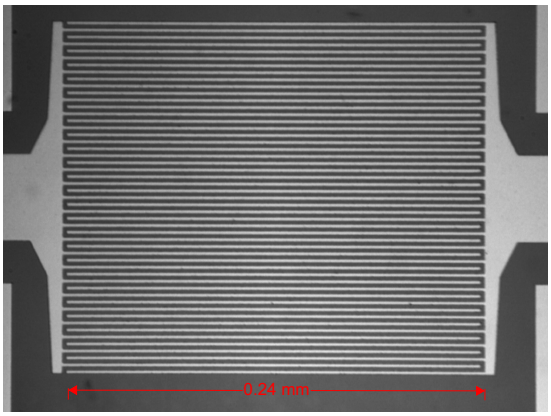

Figure 8.15: Microscope picture of feedback capacitance used in oscillator structures.

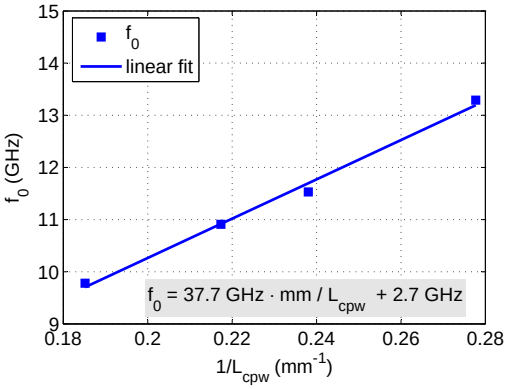

Figure 8.16: Dependence of fundamental oscillator frequency f_0 on the length of the coplanar feedback line L_{cpw}.

CHAPTER 9

Summary and Conclusion

In the following the major accomplishments of this work are summarized and a conclusion is drawn on the basis of the presented results of this work.

9.1 Summary

The following research objectives were accomplished in this work:

1. Starting from the standard GaN-HEMT technology of the Peter Grünberg Institute 9 (PGI-9) at the Research Center Jülich, this technology was optimized in order to obtain passivated HEMTs with a current-gain cut-off frequency f_T of 60 GHz and a maximum frequency of oscillation f_{max} of 125 GHz what allows using them for mm-wave applications, i.e. applications targeting a frequency regime above 30 GHz. These HEMTs exhibited an gate-drain breakdown voltage of 35 V and a drain saturation current of 0.92 A/mm at zero gate-source voltage.

2. A monolithically integrated GaN-HEMT-oscillator, which achieved a harmonic output at 39.9 GHz, was designed and built as a first investigation with respect to a potential application as driving stage of a THz-frequency-multiplier-chain.

In detail the optimization process involved the following experiments and contributions:

- The standard GaN HEMT technology was augmented by a Pt-marker-layer which maintains excellent line edge definition and morphology during ohmic contact anneal and hence makes high yield two-step T-gate processes possible.

- The ohmic contact lithography was transferred to e-beam lithography which allowed a reduction of the source-drain spacing from a minimum of 3 μm of the standard HEMT technology to 1 μm meanwhile ensuring reproducibility, high yield and increased design flexibility.

- The integration of the low-k dielectric HSQ into the GaN HEMT technology was investigated. This integration is motivated by a T-gate process which features a low gate-drain feedback capacitance.

- A metal-mask T-gate process for passivated GaN HEMTs was developed which has the capability to fabricate gates with sub-100 nm gate length L_G without the need for costly special resists.

- The influence of fluorine gas RIE on mobility and sheet carrier concentration of AlGaN/GaN heterojunction was investigated in detail. In this way low-damage plasma conditions could be identified which allowed to open a SiN surface passivation without significantly degrading the electrical properties of the epitaxial material, a corner stone of the metal-mask T-gate process.

- The gate lithography of the standard HEMT technology was optimized in order to process HEMTs with a gate length of 100 nm in a high yield and reproducible way. Passivated short-channel HEMTs achieved a current-gain cut-off frequency f_T of 86 GHz ranging amongst the highest literature values for non-recessed AlGaN/GaN HEMTs.
- A low-damage chlorine-based RIE procedure for gate recessing purpose was developed and successfully applied to GaN HEMTs. Chlorine recessed HEMTs achieved an extrinsic transconductance of greater than 400 mS/mm, an extrinsic maximum frequency of oscillation of 105 GHz and an extrinsic current-gain cut-off frequency of 35 GHz while having a gate length of 370 nm.
- A second recess procedure based on argon-sputtering was experimentally investigated and the advantages and disadvantages of both recess approaches of this work were discussed.
- The pad lithography of the standard HEMT technology was transferred from optical to e-beam lithography in order to achieve the required flexibility for a MMIC design.
- Interdigital capacitors in coplanar technique were designed, fabricated and characterized. The influence of geometrical parameters of interdigital capacitors on their transmission behavior were studied in order to determine designs which are suitable for sufficiently high feedback in oscillator circuits.
- MMIC oscillator structures with a GaN HEMT as active device were designed and built. The oscillators achieved a harmonic output of 10 dBm at 13.3 GHz and −20 dBm at 39.9 GHz.

In addition to the afore mentioned core contributions and achievements preliminary studies with Au/Pt/$GdSc_3$ Metal Insulator Semiconductor Heterojunction Field Effect Transistor (MISHFET)s were conducted. Furthermore the Z_{11}-impedance spectroscopy [277, 74] was successfully applied to round Schottky-diodes for the first time. Also experiments regarding the gate-position within the access region and the length of the gate access region were conducted. These results and results regarding $GdSc_3$ MISHFETs and Z_{11}-impedance spectroscopy for round Schottky-diodes are not presented here because they are not in the focus of the major research objectives of this thesis.

9.2 Conclusion

The results of this work clearly support the hypothesis that AlGaN/GaN HEMTs are promising active devices for mm-applications. While the RF-performance of the HEMTs of this work limits their potential circuit applications to the lower frequency regime of the mm-wave spectrum, a few research groups and institutions managed to extend their field of application to the W-band (75 GHz to 110 GHz) [33, 138, 130, 129] in the last years. The optimization of the high-frequency properties of a GaN HEMT technology for W-band applications is already challenging and requires much knowledge, skill and efforts. But as it shown by experiments of this work and by other research groups many improvements regarding the RF-properties typically come at the cost of high-voltage and/or high-power capabilities. Common trade-off situations are:

- The reduction of the gate-drain access region clearly improves the over-all electron transit time and hence RF-performance [278, 152, 156, 151], but it comes at the cost

of a reduced breakdown voltage [146].

- An appropriate surface passivation reduces DC-to-RF dispersion and thus it allows for higher output powers [47, 56]. But at the same time it causes an increase in parasitic capacitance and hence reduces the high-frequency performance [224].
- The application of a field-plate improves the high-voltage capabilities of AlGaN/GaN HEMT [196] but dramatically increases the gate-drain feedback capacitance, resulting in a reduced RF-performance, as it was shown in this work.

Consequently the major challenge is not solely related to an improvement of the RF-performance of AlGaN/GaN HEMTs, but it is seen in maintaining their high-voltage and high-power capabilities in addition. Without the feature of high-voltages operation the application of GaN HEMTs in the mm-wave regime has to be carefully reconsidered, because many competing technologies are available for mm-wave applications. These alternative technologies base on the InP pseudomorphic-High Electron Mobility Transistor (p-HEMT), the GaAs p-HEMT and metamorphic-High Electron Mobility Transistor (m-HEMT), the InP and GaAs HBT, the SiGe HBT and Si CMOS FET [279]. Especially today's Si CMOS technology is a promising candidate for mm-wave communication ICs up to 60 GHz and beyond [280]. Nevertheless, GaN based HEMTs are expected to be the semiconductor devices of choice for all fields of future RF-application which require high-frequency and high-power performance.

Appendix

A.1 Definition of absorbed and available power

The absorbed power P_{abs} of an arbitrary N-port network is the sum of the power of all incident waves a_n, i.e. P_n, minus the sum of the power of all reflected waves b_n, i.e. P_r.

$$P_{abs} = P_n - P_r = \sum_{n=1}^{N} \frac{1}{2}|a_n|^2 - \sum_{i=n}^{N} \frac{1}{2}|b_n|^2 \tag{A.1}$$

$$= \frac{1}{2}\boldsymbol{a}^{*T}\left(\boldsymbol{I} - \boldsymbol{S}^{*T}\boldsymbol{S}\right)\boldsymbol{a} \tag{A.2}$$

The following power definitions are established [112] (cf. figure 4.1):

- power absorbed by the load P_L

$$P_L = \frac{|b_2|^2}{2} - \frac{|a_2|^2}{2} = \frac{|b_2|^2}{2}(1 - |\Gamma_L|^2) \tag{A.3}$$

- power absorbed by port 1 P_1

$$P_1 = \frac{|a_1|^2}{2} - \frac{|b_1|^2}{2} = \frac{|a_1|^2}{2}(1 - |\Gamma_S|^2) \tag{A.4}$$

The available power from the source is the maximum power which can be transfered from the source to port 1 of the network. This is achieved, when the load connected to the source is matched to the source, i.e. $Z_L = Z_S{}^*$ or $\Gamma_L = \Gamma_S{}^*$. The available power at port 2 is defined accordingly and so

- available power from the source $P_{S,av}$

$$P_{S,av} = \frac{|b_S|^2}{1 - |\Gamma_S|^2} \tag{A.5}$$

- available power from port 2 $P_{2,av}$

$$P_{2,av} = \frac{|b_2|^2}{2}(1 - |\Gamma_{out}|^2) \tag{A.6}$$

A.2 Material parameters and constants of binary III-nitride compounds

Table A.1 lists material parameters and constants of binary III-N compounds.

Parameter	GaN	AlN	InN	reference
$E_{g,300K}$ (eV)	3.4	6.2	0.8	[1]
P_{sp} (C/m^2)	-0.029	-0.081	-0.032	[34, 1]
e_{33} (C/m^2)	0.73	1.46	0.97	[34, 1]
e_{31} (C/m^2)	-0.49	-0.60	-0.57	[34, 1]
$\epsilon_{r,11}$	9.5	9.0	–	[36]
$\epsilon_{r,33}$	10.4	10.7	14.6	[36]
a_0 (nm)	0.3189	0.3112	0.3540	[36, 35]
c_0 (nm)	0.5185	0.4982	0.5705	[36, 35]
C_{13} (GPa)	103	108	92	[35]
C_{33} (GPa)	405	373	224	[35]

Table A.1: Material parameter and constants of III-nitride compounds.

A.3 Standard HEMT process

- Mesa insulation
  - Dehydrate sample at 180 °C for 10 min
  - Spin photo resist AZ5214 at 4000 rpm
  - Solvent evaporation at 90 °C for 5 min
  - Rehydrate > 5 min in clean room ambient
  - UV-exposure side resist with 7 mW/cm^2 for 30 s
  - Develop resist in AZ400K/H_2O (1:4) for 2 min
  - Rinse in de-ionized water and dry in N_2 flow
  - UV-exposure mesa-layer with 7 mW/cm^2 for 5 s
  - Developing resist in AZ400K/H_2O (1:4) for 50 s
  - Rinse in de-ionized water and dry in N_2 flow
  - De-scum with O_2-plasma-asher at 300 W for 2 min
  - Resist harden at 120 °C for 10 min (cf. A.1 in figure A.1)
  - Argon Sputter with IBE-tool at 500 V, 88 mA, 30 °C tilted and rotating (cf. A.2 in figure A.1)
  - Cleaning acetone/ isopropanol and dry in N_2 flow
  - Cleaning with O_2-plasma-asher at 300 W for 2 min (cf. A.3 in figure A.1)
- Ohmic contact fabrication
  - Dehydrate sample at 180 °C for 10 min
  - Spin photo resist AZ5214 at 4000 rpm
  - Solvent evaporation at 90 °C for 5 min
  - Rehydrate > 5 min in clean room ambient

  - UV-exposure side resist with 7 mW/cm^2 for 30 s
  - Develop resist in AZ400K/H_2O (1:4) for 2 min
  - Rinse in de-ionized water and dry in N_2 flow
  - UV-exposure ohmic-layer with 7 mW/cm^2 for 5 s
  - Developing resist in AZ400K/H_2O (1:4) for 50 s
  - Rinse in de-ionized water and dry in N_2 flow
  - De-scum with O_2-plasma-asher at 300 W for 2 min (cf. B.1 in figure A.1)
  - Metal deposition with initial Argon-sputter: 35 nm Ti, 200 nm Al, 40 nm Ni, 100 nm Au
  - Lift-off in acetone
  - Cleaning acetone/ isopropanol and dry in N_2 flow
  - Cleaning with O_2-plasma-asher at 300 W for 2 min
  - RTP anneal for 30 s at 900 °C in N_2 ambient (cf. B.2 in figure A.1)
- Gate fabrication
  - Dehydrate sample at 180 °C for 10 min
  - Spin PMMA 600K at 6000 rpm
  - Solvent evaporation at 180 °C for 10 min
  - Spin PMMA 200K at 6000 rpm
  - Solvent evaporation at 180 °C for 10 min
  - Spin PMMA 600K at 6000 rpm
  - Solvent evaporation at 180 °C for 10 min
  - Metal deposition: 10 nm Cr
  - E-beam exposure 180 μC/cm^2 with proximity correction
  - Remove chrome with chrome-etch-solution
  - Rinse in de-ionized water and dry in N_2 flow
  - Develop resist in AR-600-55 for 2.5 min
  - Stop developing in isopropanol
  - De-scum with O_2-plasma-asher at 300 W for 2 min (cf. C.1 in figure A.1)
  - HCl/H_2O dip for 10 s
  - Metal deposition: 25 nm Ni, 100 nm Au
  - Lift-off in acetone
  - Cleaning acetone/ isopropanol and dry in N_2 flow
  - Cleaning with O_2-plasma-asher at 300 W for 2 min (cf. C.2 in figure A.1)
- Pad fabrication

- Dehydrate sample at 180 °C for 10 min
- Spin photo resist AZ5214 at 4000 rpm
- Solvent evaporation at 90 °C for 5 min
- Rehydrate > 5 min in clean room ambient
- UV-exposure side resist with 7 mW/cm^2 for 30 s
- Develop resist in AZ400K/H_2O (1:4) for 2 min
- Rinse in de-ionized water and dry in N_2 flow
- UV-exposure pad-layer with 7 mW/cm^2 for 5 s
- Reverse bake for 90 s at 120 °C
- Flood exposure with 7 mW/cm^2 for 15 s
- Developing resist in AZ400K/H_2O (1:4) for 20 s
- Rinse in de-ionized water and dry in N_2 flow
- De-scum with O_2-plasma-asher at 300 W for 2 min (cf. D.1 in figure A.1)
- Metal deposition: 20 nm Cr, 400 nm Au
- Lift-off in acetone
- Cleaning acetone/ isopropanol and dry in N_2 flow
- Cleaning with O_2-plasma-asher at 300 W for 2 min (cf. D.2 in figure A.1)

A.4 Cr-mask T-gate process

- Marker definition
  - Dehydrate sample at 180 °C for 10 min
  - Spin PMMA 50K at 6000 rpm
  - Solvent evaporation at 180 °C for 10 min
  - Spin PMMA 950K at 6000 rpm
  - Solvent evaporation at 180 °C for 10 min
  - Metal deposition: 5 nm Cr
  - E-beam exposure 250 μC/cm^2
  - Remove chrome with chrome-etch-solution
  - Rinse in de-ionized water and dry in N_2 flow
  - Develop resist in AR-600-55 for 2.0 min
  - Stop developing in isopropanol
  - Metal deposition: 50 nm Pt
  - Lift-off in acetone

  - Cleaning acetone/ isopropanol and dry in N_2 flow

- Ohmic contact fabrication
  - Dehydrate sample at 180 °C for 10 min
  - Spin PMMA 600K at 6000 rpm
  - Solvent evaporation at 180 °C for 10 min
  - Spin PMMA 950K at 6000 rpm
  - Solvent evaporation at 180 °C for 10 min
  - Metal deposition: 5 nm Cr
  - E-beam exposure 280 $\mu C/cm^2$
  - Remove chrome with chrome-etch-solution
  - Rinse in de-ionized water and dry in N_2 flow
  - Develop resist in AR-600-55 for 2.5 min
  - Stop developing in isopropanol
  - Metal deposition with initial Argon-sputter: 35 nm Ti, 200 nm Al, 40 nm Ni, 100 nm Au
  - Lift-off in acetone
  - Cleaning acetone/ isopropanol and dry in N_2 flow
  - Cleaning with O_2-plasma-asher at 300 W for 2 min
  - RTP anneal for 30 s at 900 °C in N_2 ambient
- Mesa insulation
  - Dehydrate sample at 180 °C for 10 min
  - Spin photo resist AZ5214 at 4000 rpm
  - Solvent evaporation at 90 °C for 5 min
  - Rehydrate $>$ 5 min in clean room ambient
  - UV-exposure side resist with 7 mW/cm^2 for 30 s
  - Develop resist in AZ400K/H_2O (1:4) for 2 min
  - Rinse in de-ionized water and dry in N_2 flow
  - UV-exposure mesa-layer with 7 mW/cm^2 for 5 s
  - Developing resist in AZ400K/H_2O (1:4) for 50 s
  - Rinse in de-ionized water and dry in N_2 flow
  - De-scum with O_2-plasma-asher at 300 W for 2 min
  - Resist harden at 120 °C for 10 min
  - Argon Sputter with IBE-tool at 500 V, 88 mA, 30 °C tilted and rotating
  - Cleaning acetone/ isopropanol and dry in N_2 flow

  - Cleaning with O_2-plasma-asher at 300 W for 2 min

- Gate foot definition
  - SiN PECVD: e.g. 150 nm at 200 °C
  - Metal deposition: 15 nm Cr
  - Dehydrate sample at 180 °C for 10 min
  - Spin PMMA 950K at 6000 rpm
  - Solvent evaporation at 180 °C for 10 min
  - E-beam exposure 250 $\mu C/cm^2$ and 380 $\mu C/cm^2$
  - Develop resist in AR-600-55 for 2.0 min
  - Stop developing in isopropanol
  - Descum RIE O_2 plasma 5 s
  - Argon Sputter with IBE-tool at 500 V, 44 mA
  - RIE CHF_3 plasma 100 W
  - RIE CF_4/O_2 plasma 15 W
- Gate Head definition
  - Dehydrate sample at 180 °C for 10 min
  - Spin PMMA 50K at 6000 rpm
  - Solvent evaporation at 180 °C for 10 min
  - Spin PMMA 600K at 6000 rpm
  - Solvent evaporation at 180 °C for 10 min
  - Spin PMMA 950K at 6000 rpm
  - Solvent evaporation at 180 °C for 10 min
  - E-beam exposure 280 $\mu C/cm^2$ and 400 $\mu C/cm^2$
  - Develop resist in AR-600-55 for 2.5 min
  - Stop developing in isopropanol
  - Descum RIE O_2 plasma 5 s
  - HCl/H_2O dip 15 s
  - Metal deposition: 25 nm Ni, 375 nm Au
  - Lift-off in acetone
  - Cleaning acetone/ isopropanol and dry in N_2 flow
  - Cleaning with O_2-plasma-asher at 300 W for 10 min
  - Remove residual chrome-mask with chrome-etch-solution

A.5 RF-gains for various values of small-signal equivalent circuit elements

The values of the small signal equivalent circuit are as follows: $W = 0.050\,\text{mm}$, $g_m = 369.8\,\text{mS/mm}$, $R_s = 0.42\,\Omega\cdot\text{mm}$, $R_d = 0.57\,\Omega\cdot\text{mm}$, $R_g = 0.23\,\Omega\cdot\text{mm}$, $R_i = 0.045\,\Omega\cdot\text{mm}$, $1/g_d = 95.7\Omega\cdot\text{mm}$, $C_{gs} = 740.8\,\text{fF/mm}$, $C_{gd} = 42.6\,\text{fF/mm}$. Elements of the small-signal equivalent circuit as depicted in figure 3.9 which are not given are assumed to be zero in this analysis. Figures A.2, A.2, A.3, A.4, A.5, A.6, A.7, A.8, A.9, A.10 show the results.

A.6 Modeled RF-gains Gamma- and T-gate

Figure A.11 shows the calculated RF-gains on the basis Γ-gate and T-gate of the discussed models.

A.7 Maximum current-gain cut-off frequency

One of the highest measured current-gain cut-off frequencies of this work is about 86 GHz. It was achieved by devices with $2 \times 220\,\mu\text{m}$ gate width and a gate length L_G of about 90 nm. The source-drain spacing was about $1.5\,\mu\text{m}$ and the devices were passivated with SiN. Figures A.12 and A.13 show the corresponding input and the output characteristic, respectively.

Figure A.14 shows typical RF-data. While the device achieves an f_T of 86 GHz a much lower f_{max} of 32 GHz is achieved. The origin of the much lower f_{max} is caused by a high R_g and a high drain transconductance g_d. A technique to increase R_g while maintaining a short L_G is the application of T-gates. A method to increase g_d while maintaining a short L_G is recessing the barrier layer under the gate. Motivated by the example of this section both approaches, T-gate processes and Recess processes, are discussed and investigated in this work.

A.8 SEM picture of gamma-gate

Figure A.15 shows a SEM picture characterized in this work.

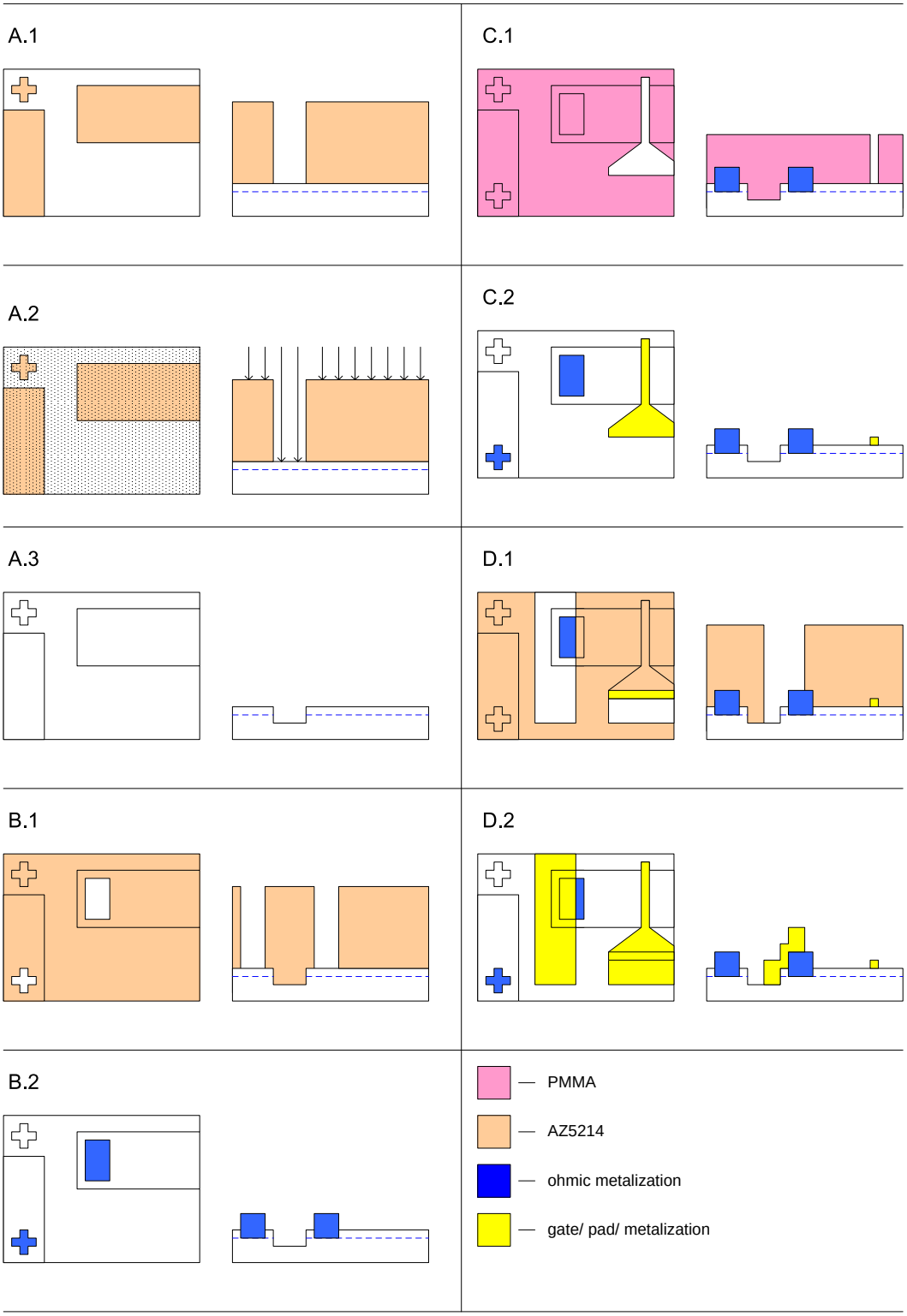

Figure A.1: Schematic illustration of the standard HEMT process. Only one ohmic contact of the gate-symmetric structure is depicted to avoid the illustration of redundant information.

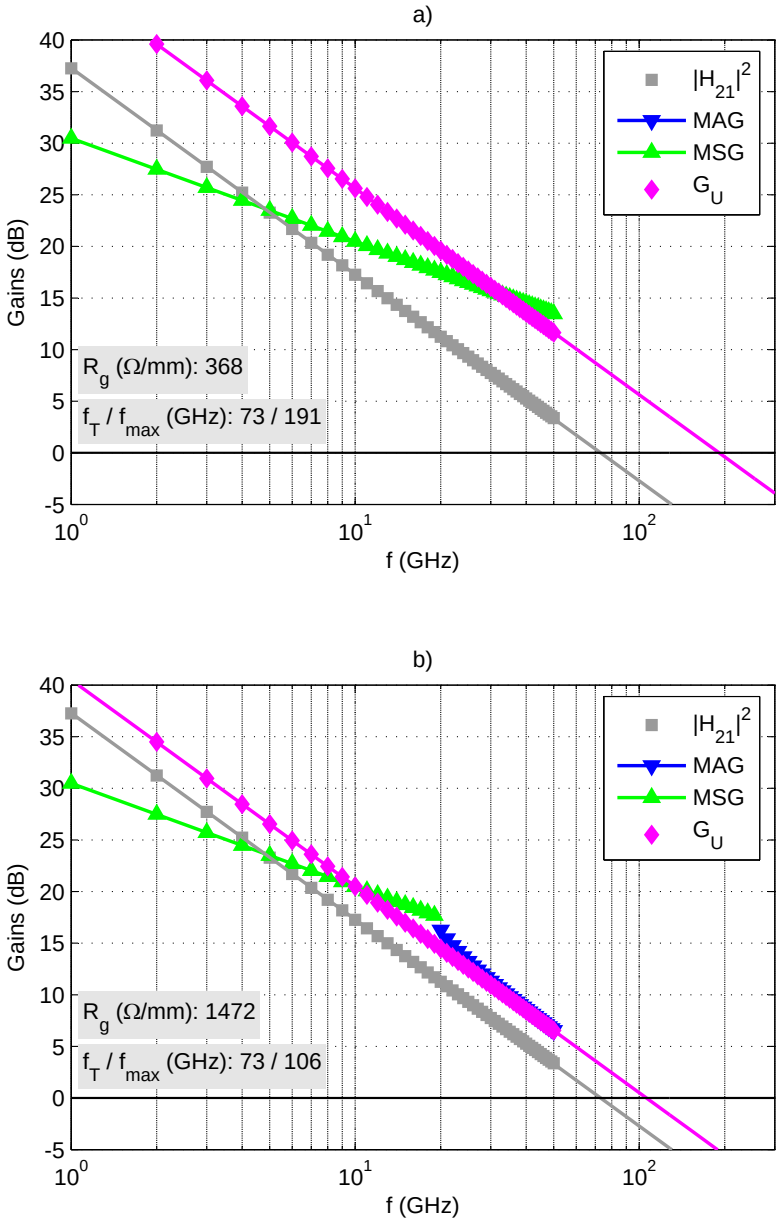

Figure A.2: RF-gains calculated on the basis of the values for the small-signal equivalent circuit elements with varying R_g.

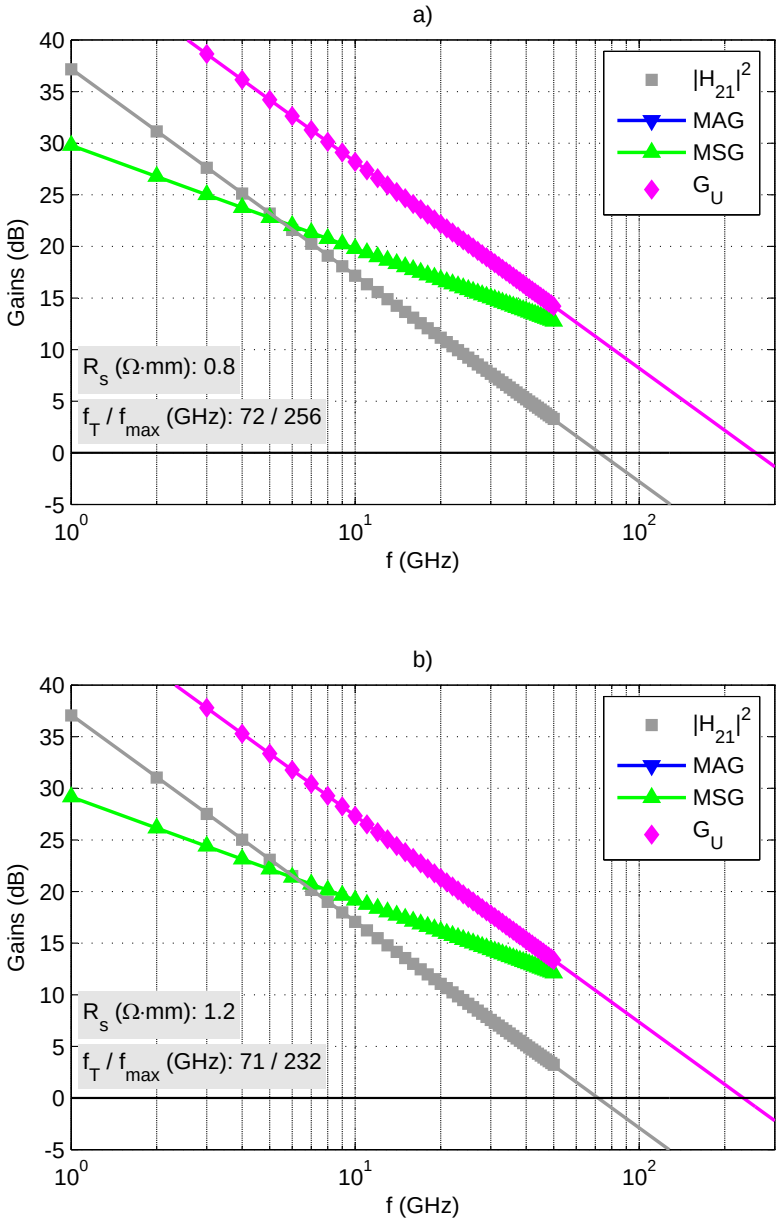

Figure A.3: RF-gains calculated on the basis of the values for the small-signal equivalent circuit elements with varying R_s.

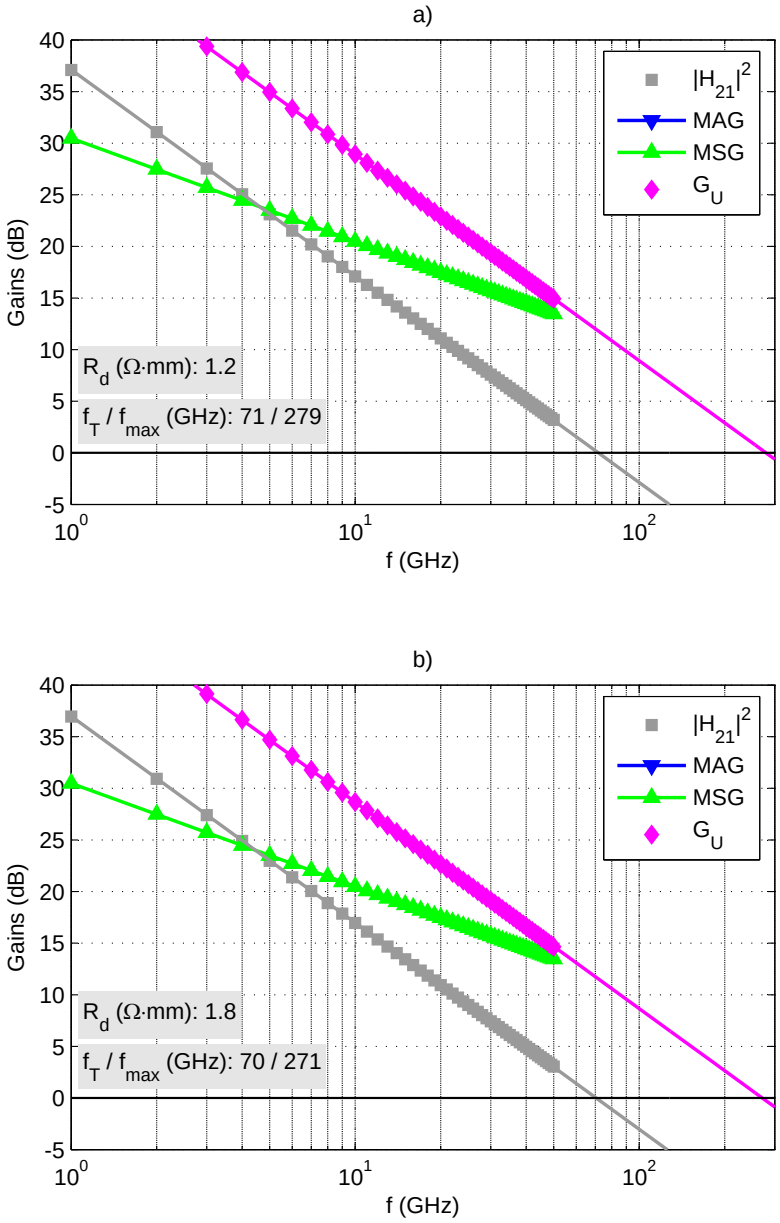

Figure A.4: RF-gains calculated on the basis of the values for the small-signal equivalent circuit elements with varying R_d.

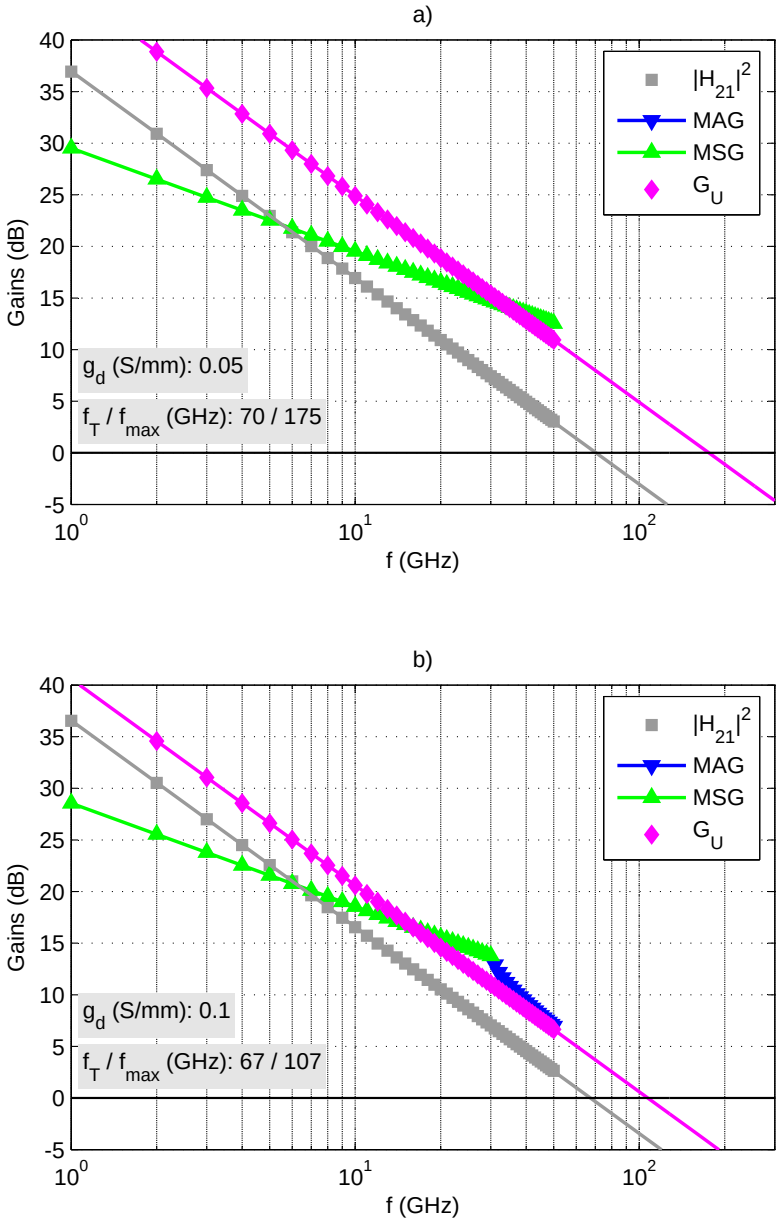

Figure A.5: RF-gains calculated on the basis of the values for the small-signal equivalent circuit elements with varying g_d.

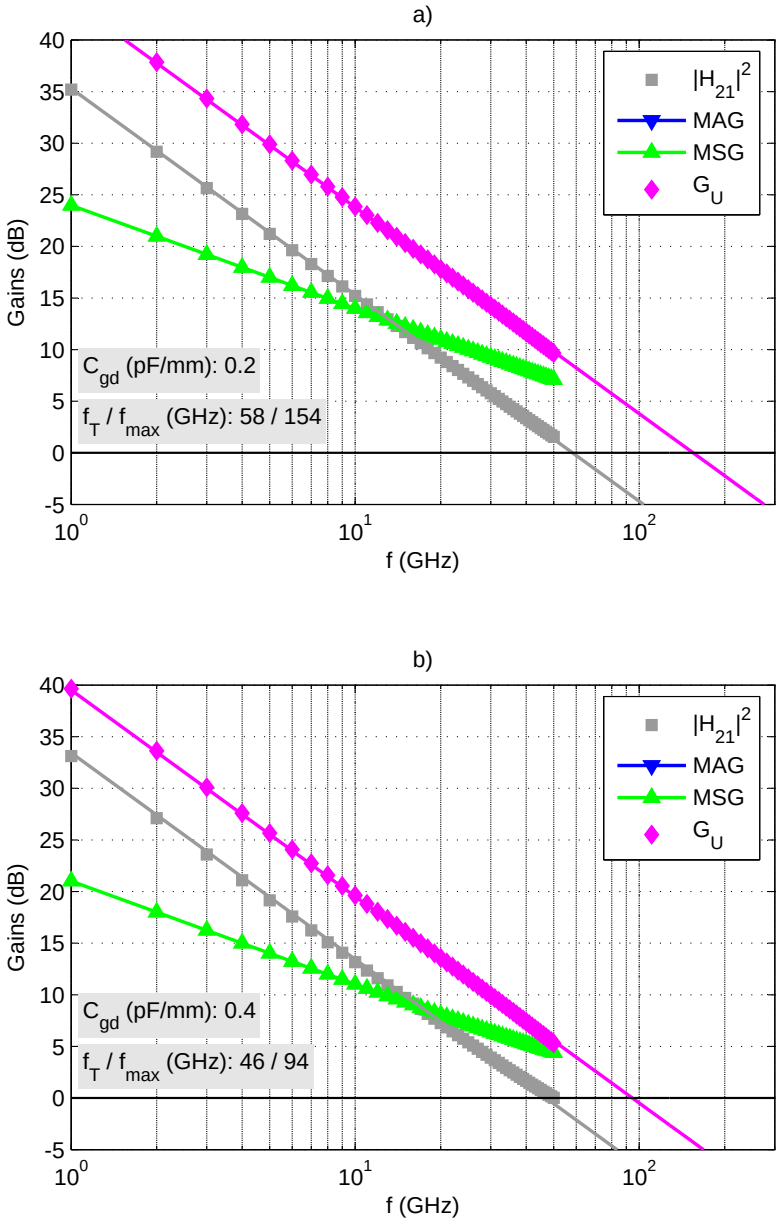

Figure A.6: RF-gains calculated on the basis of the values for the small-signal equivalent circuit elements with varying C_{gd}.

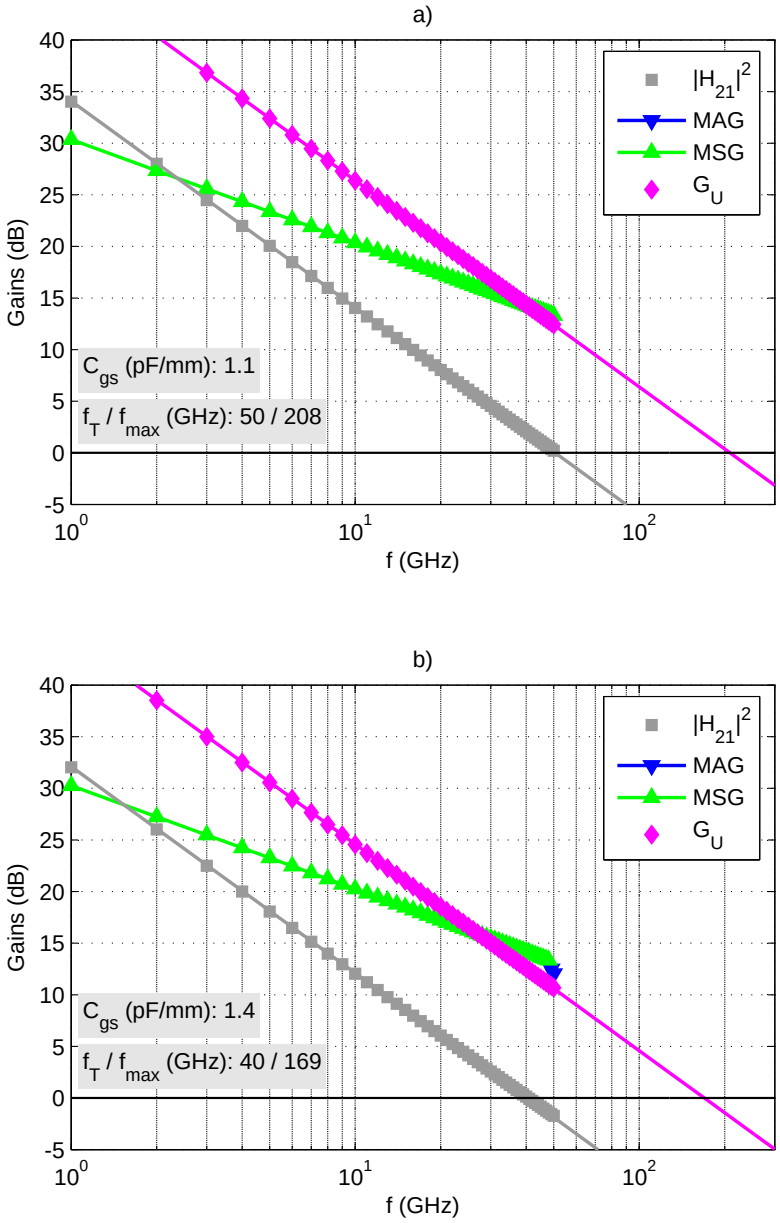

Figure A.7: RF-gains calculated on the basis of the values for the small-signal equivalent circuit elements with varying C_{gs}.

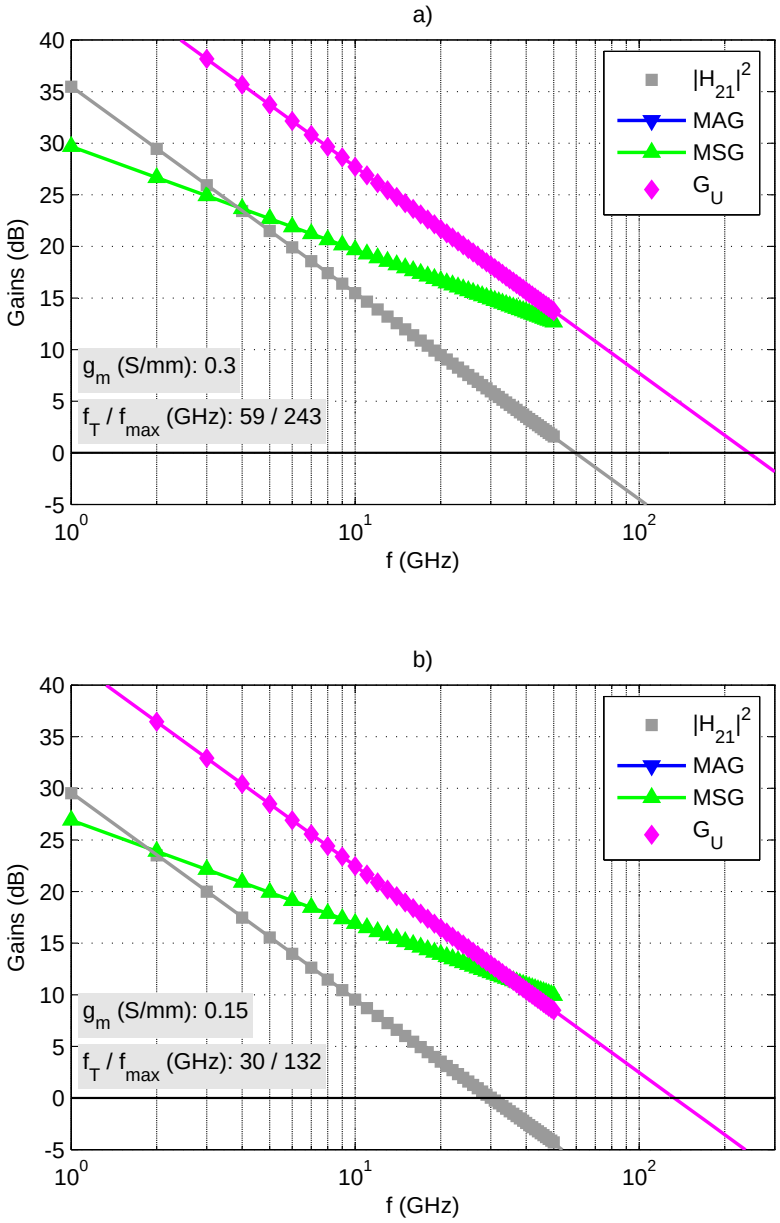

Figure A.8: RF-gains calculated on the basis of the values for the small-signal equivalent circuit elements with varying g_m.

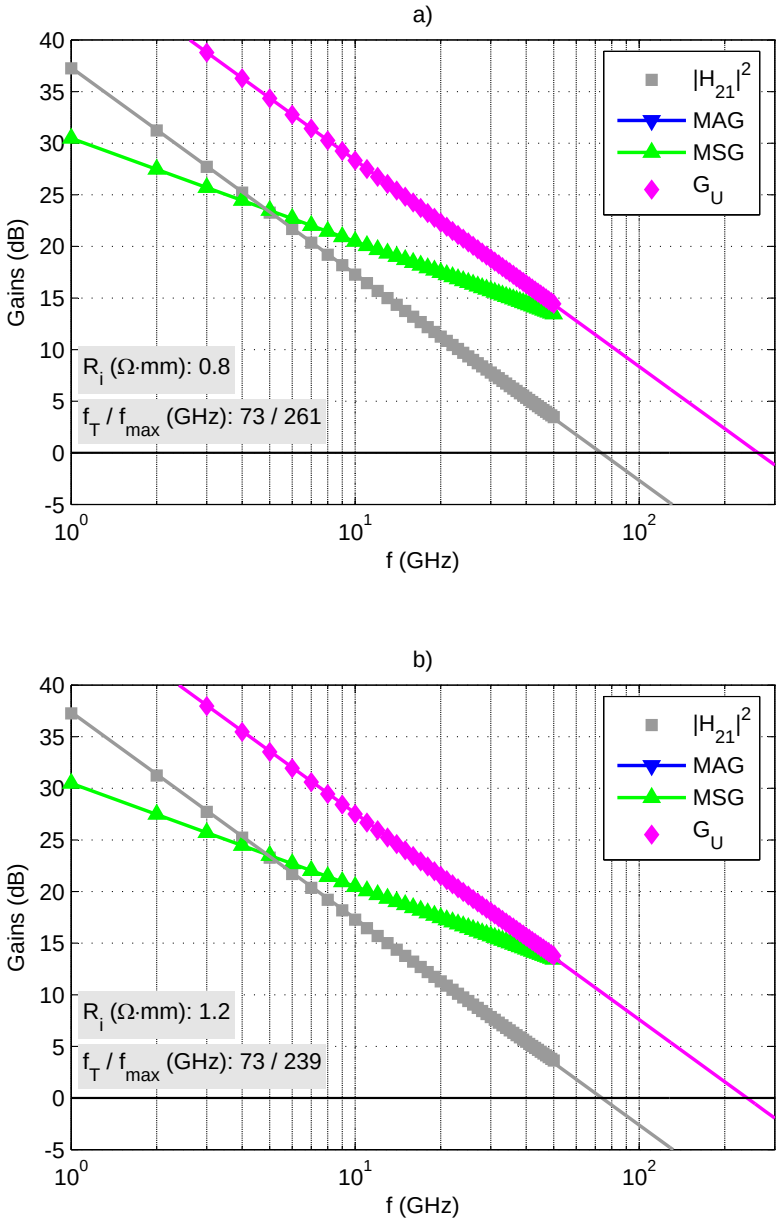

Figure A.9: RF-gains calculated on the basis of the values for the small-signal equivalent circuit elements with varying R_i.

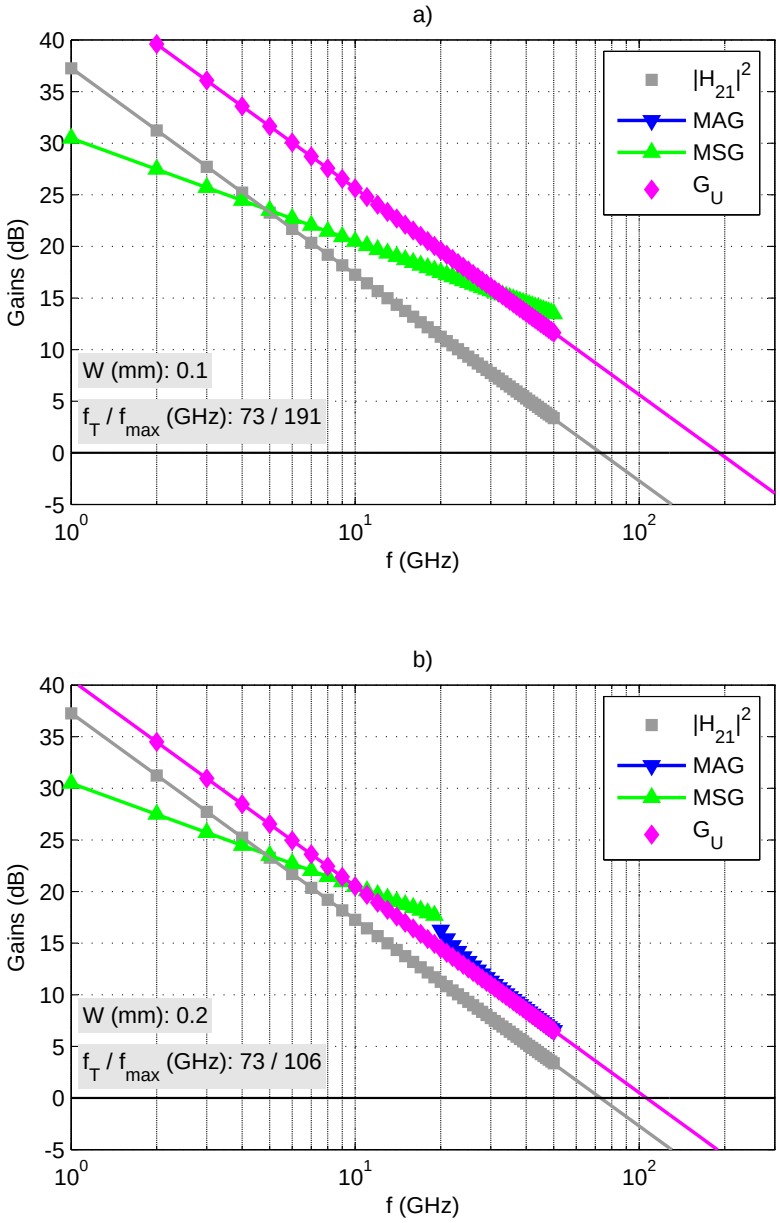

Figure A.10: RF-gains calculated on the basis of the values for the small-signal equivalent circuit elements with varying W.

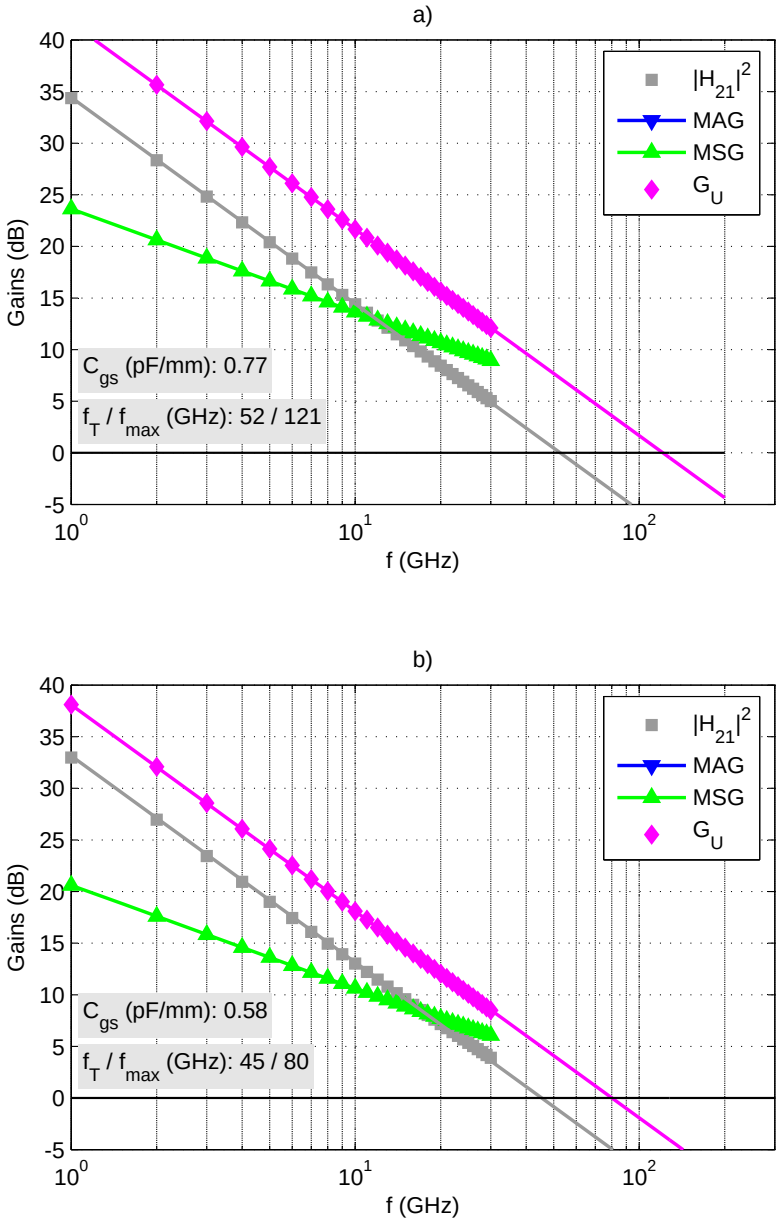

Figure A.11: RF-gains calculated on the basis of the values for the small-signal equivalent circuit elements, a) Γ-gate, b) T-gate.

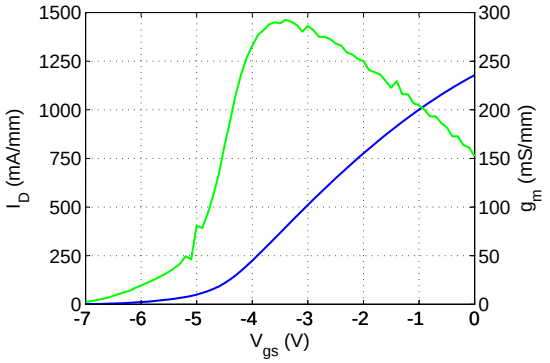

Figure A.12: Input characteristic of a $2 \times 220\mu$m HEMT with L_G of about 90 nm. $V_{DS} = 5\,\mathrm{V}$

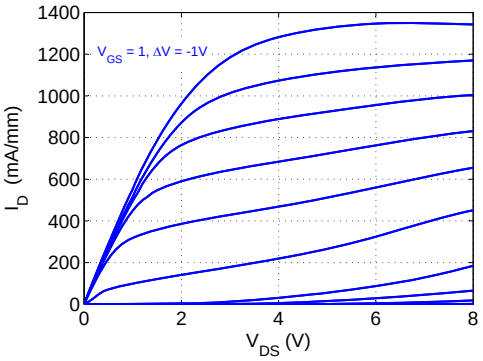

Figure A.13: Output characteristic of a $2 \times 220\mu$m HEMT with L_G of about 90 nm.

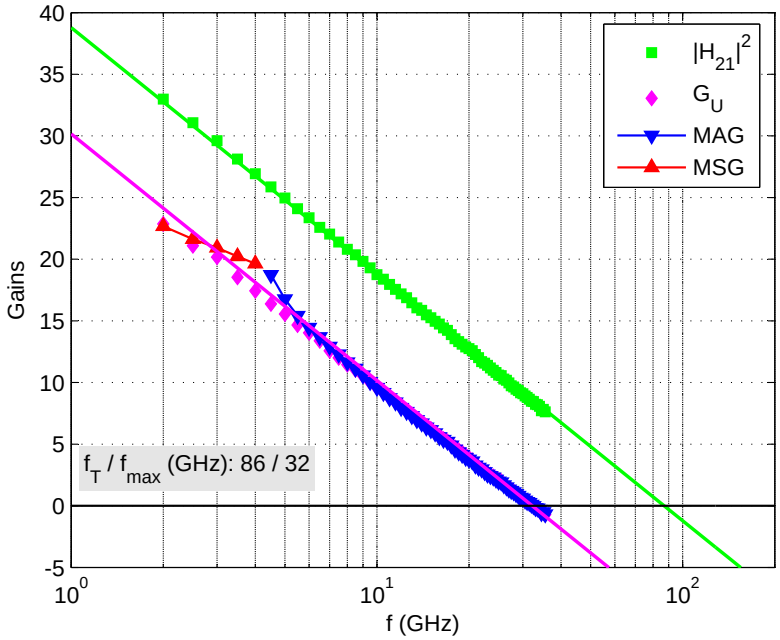

Figure A.14: Measured S-parameters for $V_{GS} = -4.5\,\mathrm{V}$ and $V_{DS} = 8\,\mathrm{V}$.

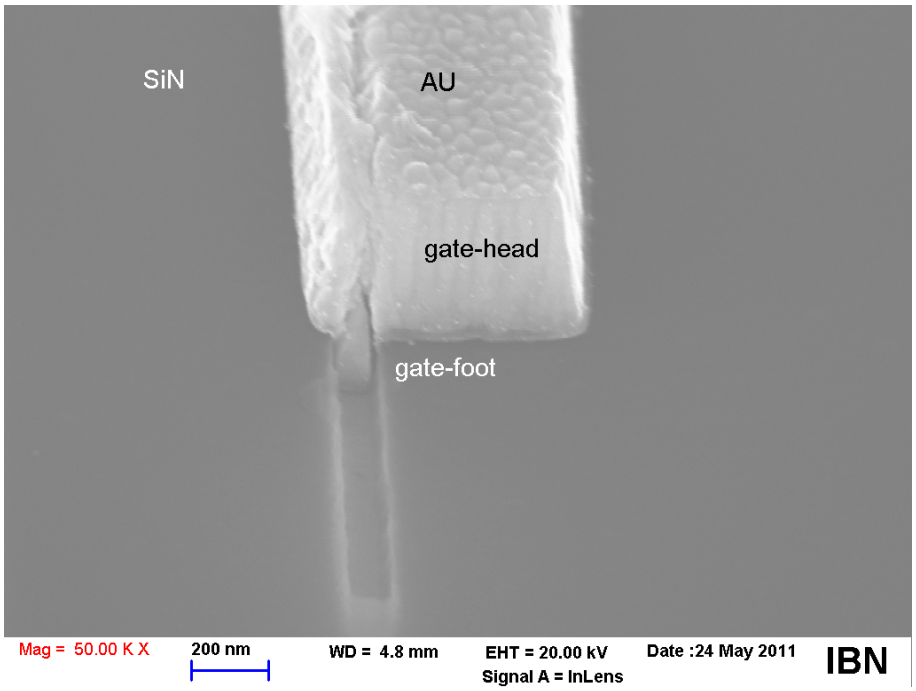

Figure A.15: SEM picture of a Γ-gate characterized in this work.

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

2DEG Two-Dimensional Electron Gas

A

AFM Atomic Force Microscopy

AZ-PF-514 a photo resist

AZ1350 a photo resist

AZ400K a basic developer

AZ5206 a photo resist

AZ5214 a photo resist

B

BFoM Baliga's Figure of Merit

BWO Backward-Wave Oscillator

C

CAD Computer Aided Design

Cat-CVD Catalytic - Chemical Vapor Deposition

CV Capacitance-Voltage

CMOS Complementary Metal Oxide Semiconductor

D

D-mode Depletion-mode

DC Direct Current

DFG Difference Frequency Generation

DUT Device Under Test

E

e-beam electron-beam

E-mode Enhancement-mode

F

FET Field Effect Transistor

FIB Focused Ion Beam

G

GP Gradual Pinch-off

GS Gradual Saturation

H

H-parameters Hybrid-parameters

HBT Heterojunction Bipolar Transistor

HEMT High Electron Mobility Transistor

HFET Heterojunction Field Effect Transistor

HIGFET Heterostructure Insulated Gate Field Effect Transistor

HSQ Hydrogen Silses-Quioxane

I

IBE Ion Beam Etching

IC Integrated Circuit

ICP Inductively Coupled Plasma

IV Current-Voltage

J

JFoM Johnson's Figure of Merit

L

LED Light Emitting Diode

LOR Lift-Off Resist

M

MAG Maximum Available Gain

MESFET Metal Semiconductor Field Effect Transistor

m-HEMT metamorphic-High Electron Mobility Transistor

MIC Microwave Integrated Circuit

MIBK Methyl Iso-Butyl Ketone

MIS Metal Insulator Semiconductor

MISHFET Metal Insulator Semiconductor Heterojunction Field Effect Transistor

MMA Methyl-MethAcrylat

MMIC Monolithic Microwave Integrated Circuit

MODFET Modulation Doped Field Effect Transistor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

ME Modulation Efficiency

MSG Maximum Stable Gain

P

PAE Power Added Efficiency

PECVD Plasma-Enhanced Chemical Vapor Deposition

p-HEMT pseudomorphic-High Electron Mobility Transistor

PL Photo-Luminescence

PMMA Poly-Methyl-MethAcrylat

PMGI Poly-di-Methyl-Glutar-Imide

Q

QCL Quantum Cascade Laser

R

RF Radio Frequency

RIE Reactive Ion Etching

RTD Resonant Tunneling Diode

RTP Rapid Thermal Process

S

S-parameters Scattering-parameters

SDHT Selectively Doped Heterojunction Transistor

SEDFET Separately-Doped-Field Effect Transistor

ST Sub-Threshold behavior

SEM Scanning Electron Microscope

STEM Scanning Transmission Electron Microscopy

T

TEGFET Two-Dimensional-Electron-Gas Field Effect Transistor

TEM Transmission Electron Microscopy

TLM Transmission Line Model

TMAH Tetra-Methyl Ammonium Hydroxide

TWT Traveling-Wave Tube

U

UV Ultra Violet

W

WiMAX Worldwide Interoperability for Microwave Access

Y

Y-parameters admittance-parameters

Z

Z-parameters impedance-parameters

ZEP electron-beam resist of Nippon Zeon Co.

LIST OF SYMBOLS

Table B.1: List of used mathematical symbols.

Symbol	Units	See Page	Meaning
a	m	14	dimension of wurtzite cell
a_0	m	14	dimension of relaxed wurtzite cell
a_m	$\mathrm{V}/\sqrt{\Omega} = \sqrt{W}$	32	incident wave in context of S-parameters
b_n	$\mathrm{V}/\sqrt{\Omega} = \sqrt{W}$	32	reflected wave in context of S-parameters
BV_{GD}	V	76	gate-drain breakdown voltage
BV_{on}	V	55	breakdown voltage of the on-state device
c	m	14	dimension of wurtzite cell
c_0	m	14	dimension of relaxed wurtzite cell
C_{area}	$\mathrm{F/m^2}$	68	capacitance per unit area
C_{xy}	Pa	14	elastic constants xy
C_{dg}	F	28	small-signal drain-gate capacitance
$C_{GS,ext}$	F	26	extrinsic gate-source capacitance
C_{gd}	F	28	small-signal gate-drain capacitance
C_{gs}	F	28	small-signal gate-source capacitance
C_{pds}	F	28	small-signal pad drain-source capacitance
C_{pgd}	F	28	small-signal pad gate-drain capacitance
C_{pgs}	F	28	small-signal pad gate-source capacitance
C_{sd}	F	28	small-signal source-drain capacitance
Δd	m	20	mean distance from 2DEG to heterojunction
d	m	20	thickness of the barrier layer
d_i	m	20	thickness of the spacer layer
d_{SD}	m	78	distance between source and drain contact
d_{SG}	m	25	distance between source contact and gate
ϵ_r	–	8	permittivity constant
e	$1.602 \cdot 10^{-19}\,\mathrm{C}$	20	elementary charge constant
e_{xy}	$\mathrm{C/m^2}$	14	piezoelectric constants xy
E	V/m	22	electric field
$\boldsymbol{E}$	–	32	unity matrix in context of two-port theory
E_c	V/m	22	critical electric field in the context of carrier velocity
E_{cr}	V/m	8	critical electric breakdown field
E_f	eV	15	Fermi-potential
E_g	eV	8	band gap
f_0	Hz	101	fundamental frequency of oscillation
f_2	Hz	105	second harmonic frequency of oscillation
f_{max}	Hz	31	maximum frequency of oscillation
f_τ	Hz	24	intrinsic transit frequency
f_T	Hz	31	current-gain cut-off frequency
Γ	–	35	refection coefficient
γ	$\mathrm{m^{-1}}$	25	propagation constant
G_A	–	36	available power gain
G_{CH}	S	85	channel conductance
g_d	S	26	drain transconductance
g_m	S	23	mutual transconductance
$g_{m,ext}$	S	23	extrinsic mutual transconductance
$g_{m,sat}$	S	23	mutual transconductance under saturation condition
G_T	–	35	transducer power gain

Table B.1: List of used mathematical symbols (continued)

Symbol	Units	See Page	Meaning
G_{TU}	–	35	unilateral transducer power gain
$G_{TU,max}$	–	36	maximum unilateral transducer power gain
G_U, U	–	35	unilateral power gain, Masons's U
H_{mn}	–, Ω, S	32	H-parameter mn
$\bar{H}_{mn}$	–	32	normalized H-parameter mn
I_D	A	22	drain current
i_d	A	27	phasor of the small-signal drain current
$I_{D,sat}$	A	22	saturation drain current
i_g	A	27	phasor of the small-signal gate current
K	–	32	Rollet's stability factor
L_c	m	25	length of ohmic contact metalization
L_{cpw}	m	102	length of coplanar transmission line
L_f	m	102	dimension of interdigital capacitor
L_G	m	22	gate length
L_{GD}	m	22	gate length extension at the drain side
$L_{G,eff}$	m	22	effective gate length
L_T	m	26	characteristic transfer length
μ_{Hall}	$\mathrm{cm^2V^{-1}s^{-1}}$	67	Hall-mobility
μ_n	$\mathrm{cm^2V^{-1}s^{-1}}$	8	election drift mobility
n_s	$\mathrm{cm^{-2}}$	19	electron sheet carrier concentration
η	–	24	Modulation Efficiency
$P_{S,av}$	W	34	available power of a source S
$P_{out,RF}$, P_{out}	W	55	RF output power
$\boldsymbol{P}_{sp}$	$\mathrm{C/m^2}$	14	vector of the spontaneous polarization
P_{sp}	$\mathrm{C/m^2}$	14	value of the spontaneous polarization
$\boldsymbol{P}_{pz}$	$\mathrm{C/m^2}$	14	vector of the piezoelectric polarization
P_{pz}	$\mathrm{C/m^2}$	14	value of the piezoelectric polarization
Q_{CH}	C	24	channel carrier stored charge
Q_{SV}	C	24	channel carrier moving with v_{sat}
Q_{GC}	C	24	channel carrier moving with $v < v_{sat}$
Q_{BL}	C	24	parasitic charge in barrier layer
R_c	Ω·m	25	contact resistance
ρ_c	$\Omega\cdot\mathrm{m^2}$	25	specific contact resistance
R_D	Ω	26	drain resistance under DC conditions
R_d	Ω	30	small-signal drain resistance
R_g	Ω	28	small-signal gate resistance
R_i	Ω	28	small-signal channel resistance
R_S	Ω	25	source resistance under DC conditions
R_s	Ω	30	small-signal source resistance
$R_\square$	Ω	25	sheet resistance
σ_{int}	$\mathrm{C/m^2}$	15	fixed interface charge density
σ_{sur}	$\mathrm{C/m^2}$	17	fixed surface charge density
$\boldsymbol{S}$	–	32	matrix of S-parameters
S_e	m	102	dimension of interdigital capacitor
S_f	m	102	dimension of interdigital capacitor
S_g	m	102	dimension of interdigital capacitor
S_{mn}	–	32	S-parameter mn
τ	s	28	parameter of small-signal equivalent circuit
τ_t	s	24	average electron gate transit time
T	K	20	temperature
t_m	m	102	metalization thickness
$t_{barrier}$, t_b	m	41	barrier thickness

Table B.1: List of used mathematical symbols (continued)

Symbol	Units	See Page	Meaning
Θ	W K^{-1} m^{-1}	8	thermal conductivity
V_{DS}	V	23	drain-source voltage
v_{ds}	V	27	phasor of the small-signal drain-source voltage
$\tilde{v}_{ds}$	V	27	small-signal drain-source voltage
$V_{DS,sat}$	V	23	drain-source voltage at which $I_D = I_{D,sat}$
V_G	V	19	gate potential
V_{GS}	V	22	gate-source voltage
v_{gs}	V	27	phasor of the small-signal gate-source voltage
$\tilde{v}_{gs}$	V	27	small-signal gate-source voltage
v_{sat}	m/s	8	saturation velocity
v_{peak}	m/s	20	peak velocity (under steady state)
V_{th}	V	20	threshold voltage
W	m	22	total gate width
W_f	m	102	dimension of interdigital capacitor
$\bar{\boldsymbol{Y}}$	–	32	normalized admittance matrix
$\boldsymbol{Y}$	–	32	admittance matrix
Y_{mn}	S	32	Y-parameter mn
$\bar{\boldsymbol{Z}}$	–	32	normalized impedance matrix
$\boldsymbol{Z}$	–	32	impedance matrix
Z_0,Z_{01},Z_2	Ω	32	reference impedance
Z_{mn}	Ω	32	Z-parameter mn

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