Simulation and Analysis of Analog Circuit and PCM (Process Control Monitor) Test Structures in Circuit Design

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Abstract

PCM test structures are commonly used to check the produced wafers from the standpoint of the technologist. In general these structures are managed inside the FAB and are focused on standard device properties. Hence their development and analysis is not driven by analog circuit blocks, which are sensitive or often used. Especially for DFM/Y of analog circuits the correlation between design and technology has to be defined. The knowledge of electrical behavior of test structures helps to improve the designer's sensitivity to technological questions.

This paper presents a method to bring the PCM methodology into the analog circuit design to improve design performance, yield estimation and technology correlation. We show how both analog circuit and PCM blocks can be simulated and analyzed in the design phase.

1 Introduction

Design for manufacturing and yield (DfM/Y) techniques become more important for cooperation of wafer fabrication (FAB) and circuit design. Technology characterization is essential for both sides. But in general this topic is only driven by FAB. If design of analog/mixed signal circuits is coming to technology limits this topic becomes more interesting for the design. It is interesting for both company structures with in-house FAB and FAB less.

Process control monitor (PCM) test structures are part of the SPC (statistical process control). They are used to characterize and to control the technology in reference to the technology specification such as threshold voltage V_{th} or internal parameter for special technology steps which are confidential. So the PCM test structures are developed and optimized for technology purposes. The PCM test structures are located beside the chip area of the customer on the wafer and are processed by the same technology steps.

The validation of circuit performance in reference to circuit specification is divided into two main parts. Verification and test stages are located before and after wafer fabrication respectively. Verification of the circuit during the design stage is based on simulation, whose results depend particularly on the accuracy of models. The test stage is used to validate every fabricated chip and to sort all chips into categories (e.g. pass/fail).

Especially if the results of verification via simulation and chip test does not match then the technology performance is checked. So results of PCM test structures becomes interesting for the analog designer too. PCM data experiences are necessary for efficient analysis.

Correlation between technology and design is the basis for successful DfY methods. This correlation can be proven by suitable test structures.

The paper is divided into four parts. First we give a short introduction to PCM test structures in fabrication process and circuit design. The methodology to recognize defined PCM test structures is presented in section 3. The methodology part of the paper is followed by three subsections of practical examples, in detail that are mismatch of capacitors, latch-up and bulk current of nmos transistors.

2 PCM Test Structures

2.1 PCM Test Structures for FAB

Only few PCM areas which covers a lot of single PCM test structures are used for SPC by FAB. Figure 1 shows a example of five PCM areas which are distributed over the wafer. PCM test structures cost wafer area and measurement time. Hence the PCM area is reserved for concerns of the FAB but is not provided for circuit design issues.

Number and measurement effort of the test structures depend on specification and complexity of the technology. In general the measuring is extracting some properties of every test structure. Thus a couple of hundred up to thousands of data are measured and analysed during wafer fabrication.

Criteria for PCM test structures from the view of the FAB are

- Technology sensitive to control and verify the specification,
- Correlation to technology steps to support debugging,
- Less area consumption and
- Fast and efficient measurement to save costs.

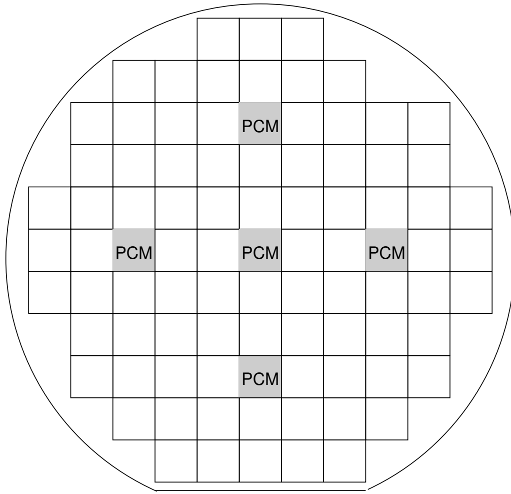

Figure 1: Wafer with five PCM areas which contain the test structures.

2.2 PCM Test Structures for Design

Circuit performance parameters are sensitive to technology which can be seen on single yield. An analysis of yield lost [1] shows how performance parameter sensitivities of analog circuits can help to detect problems in the fabrication process. The wafer map in Figure 2 shows low yield strips of a mixed signal chip. It could be found that these strips are the so-called finger print of the implanter equipment used. As a result of the problem analysis a construction gap of the implanter was found and could be solved together with the tool manufacturer.

The example in Figure 2 clarifies the following items:

- Test structures have to be sensitive to technology.
- Circuit properties have to be covered with test structures.
- Test structures have to be distributed over wafer (finger print of equipment or technology).
- Area limitation constraints the size of test structures (see Figure 3).
- Fast and efficient measuring principles are necessary to save cost.
- Powerful wafer analyser and map tool for automatic and optical inspection is basis for analysis (e.g. ZMD inhouse tool: WaferAnalyser [2]).

Because the analog performance parameter reviewed in [1] is sensitive to a number of process parameters the analysis was expensive and has to be an exception. Other strategies can help to simplify such an analysis. The basic idea of the strategies is the implementation of test structures of key devices (e.g. coils) or sensitive circuit parts (see section 4). Such test structures are area optimized to squeeze them inside a pad ring (see Figure 3a) or between the chips (see Figure 3b), also called scribe line monitors (SLM).

Device models are the connection from design to the technology. Accuracy and coverage of the device models are limited in reference to possible effects. This fact divides the test structures into two categories:

- Simulation and mesurement or
- Measurement only.

Correlation between technology and design can be retraced when results extraction of network simulation in design stage and property measurement in test stage are supported. In this case the used models cover the observed effects. So it is possible to develop the test structures and the measurement method in a similar manner as circuit design (cf. section 4.1 and 4.3).

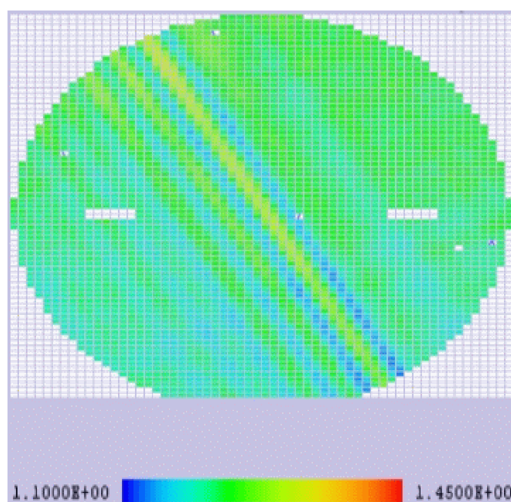

Figure 2: Wafer map shows low yield strips coming from defective implanter equipment. Process steps leave finger print at the wafer which can be seen at circuit parameters of sensitive circuits.

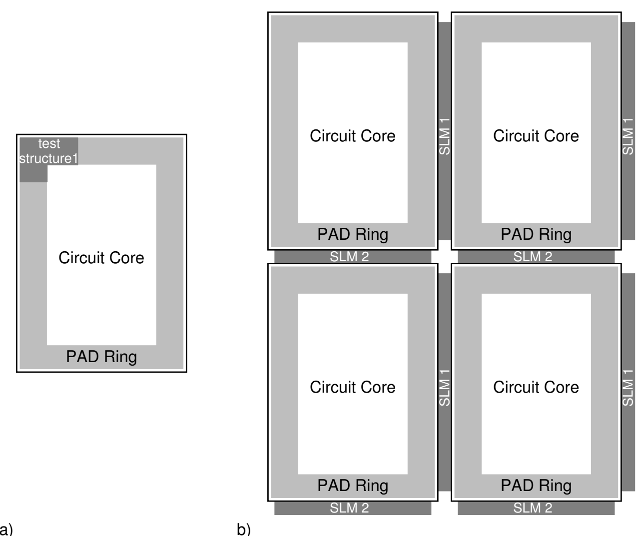

Figure 3: Area-saving strategies for test structures of chips. a) Part of the PAD ring. b) Scribe line monitor (SLM) for utilization of the saw area.

The second category containts test structures for effects which are not covered by provided models like latch up (see section 4.2).

3 PCM Test Structures Flow

The choice of the right test structures is not obvious. Some ways are possible:

- General/standard configuration for analog circuits,
- Individual selected by analog designer and
- Circuit relevant for critical performance parameters (e.g. tool supported).

The third way provides a method to choose test structures which are interesting for the used circuitry. Due to the area limitation for test structures, it is important to choose sensitive test structures. We only want to give some details for that point.

Figure 4 shows a tool supported flow to consider test structures and analog/mixed signal circuits. This flow helps the choice and definition of test structure sets during design.

Circuit design inside the design environment Cadence [3] is done by the Schematic Entry. Next the simulation is configured and checked with the Analog Design Environment (ADE). Basic analysis such as transient, AC, DC are used at this step.

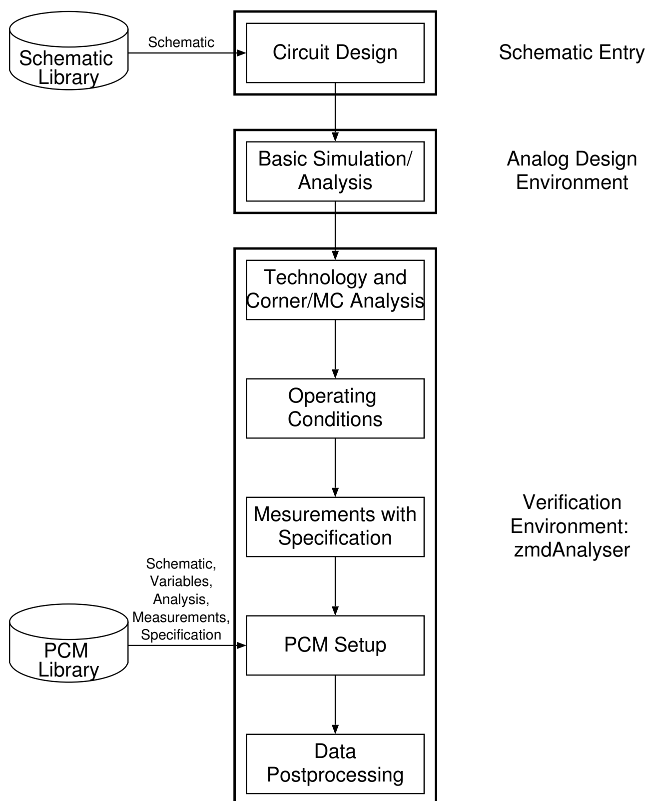

Figure 4: Tool supported flow to consider PCM test structures in circuit design.

The verification is carried out with the ZMD in-house verification environment called zmdAnalyser [4]. zmdAnalyser is a design tool driven by analog/mixed signal designers to improve the design work. This tool extends the Analog Design Environment from Cadence. zmdAnalyser supports advanced corner and Monte Carlo analysis as well as special analysis like sensitivity and trimming analysis [5, 6] which are adapted to our design challenges.

The circuit performance measurements with specifications in reference to technology and operating conditions are the focus of the verification environment. Figure 4 shows that this methodology can be expanded to consider test structures and the circuit. Data post processing inside the analysis step can be used to investigate e.g. correlation of circuit and test structure results together. Monte Carlo analysis with global and local parameter variation is partially interesting for such an analysis, too.

Advantages of the implementation inside the verification environment are

- Known design stage of analog circuit design is not affected.
- Test bench and analog circuit need no changes.
- Analog circuit and test structures can be simulated together over technology sets and operating conditions .
- PCM library contains for every test structure all necessary data e.g. schematic, analysis, measurements and specification.
- Analysis (e.g. correlation) between circuit performance and test structure results are possible.
- Reuse of simulation management and analyses of data post processing.

You should be aware the acceptance of any system like that presented depends on the quantity and quality of elements in the test structure library. This library has to contain elements to cover main design problems and different effects (see section 3). Next section 4 introduces three examples of test structures.

4 Examples

Examples for test structures are published in connection with different analog properties. Behzard Razavi gives a wide overview in [7] to technology characterization for analog purposes with simple and effective test circuits. Articles on the topic design for test (DfT) are interesting sources (e.g. [8]), too.

Next sections presents three examples of test structures. If mismatch of capacitors is critical for circuitry the test structure in section 4.1 should be used. A latch up test structure in section 4.2 was developed to investigate parasitic effects. Finally the last example shows how bulk current can be used for technology characterization.

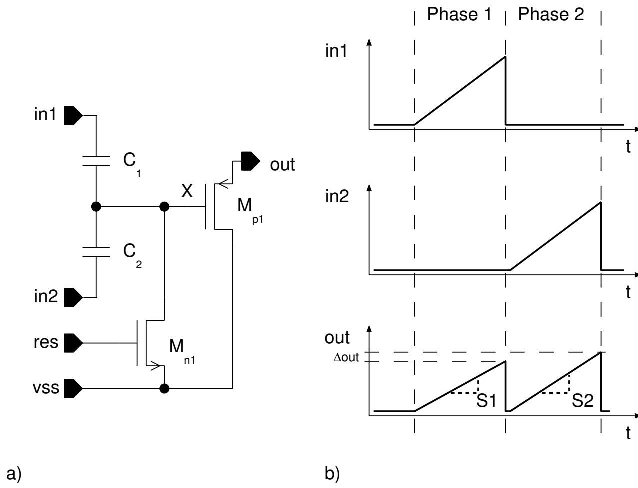

Figure 5: Test structure to measure mismatch between capacitors. a) Circuit of the test structure. b) Input voltage signals in1 and in2 and output voltage signal out of the measuring principle.

4.1 Capacitor Mismatch

Mismatch problems of devices are known by designers. But it is sometimes underestimated because current tools and process design kits (PDK) are based on several assumptions. Mismatch influence can be simulated by Monte Carlo simulation. The statistical models used are generated with golden mismatch layout rules. Hence a correlation between simulation and test results of analog parameters depends on layout realisation.

For small capacitors used in most analog circuits characterization of mismatch is difficult. A simple test circuit and measurement principle is presented in [9]. Figure 5a illustrates the schematic. The relative mismatch between the capacitor c_1 and c_2 can be measured. Transistor M_{p1} is used as a source follower to buffer the voltage signal at node X. Node X can be reseted via the transistor M_{n1}.

Signals of the measurement principle are shown in Figure 5b. An interchanged ramp signal is applied at the ports in_1 and in_2. During ramp signal at one port the other port is grounded. The structure forms a capacitive divider for the input ramp signal. A mismatch between C_1 and C_2 can be expressed with ΔC. ΔC has an affect on the slew rate S_1 and S_2 in the phase 1 and 2. This relation can be expressed by

$$\Delta C = C_1 \frac{\Delta S}{S_1} \quad \text{with} \quad \Delta S = S_2 - S_1, \Delta C = C_2 - C_1 \qquad (1)$$

Parasitic capacitance at node X are canceled due to the differential measurement principle which is carried out sequentially in phase 1 and 2.

The layout of a test chip to analyse mismatch of different capacity values is shown in Figure 6. The SLM structure with $C_1 = C_2 = 0.25pF$ is marked.

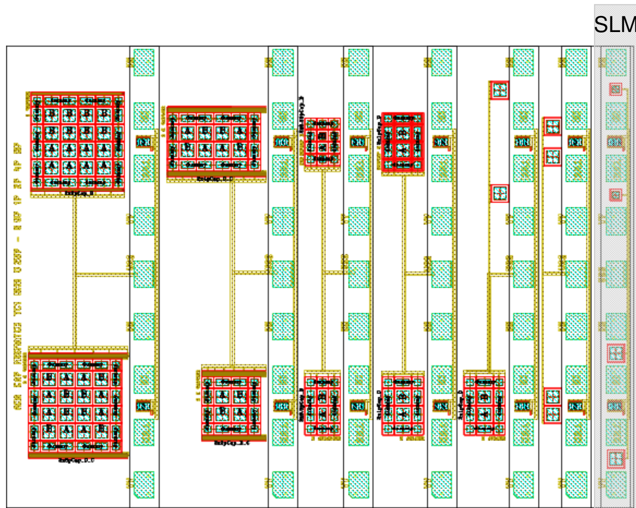

Figure 6: Layout of a test chip for development of capacitor mismatch test structures. The SLM structure is marked for comparison.

4.2 Latch-up

Latch-up is defined as creation of a low-impedance path between the power supply rails by triggering on a parasitic four layer (NPNP) bipolar structure. Latch-up immunity is important and specifications are strong, especially for circuits for automotive and sensor applications. Latch-up behaviour

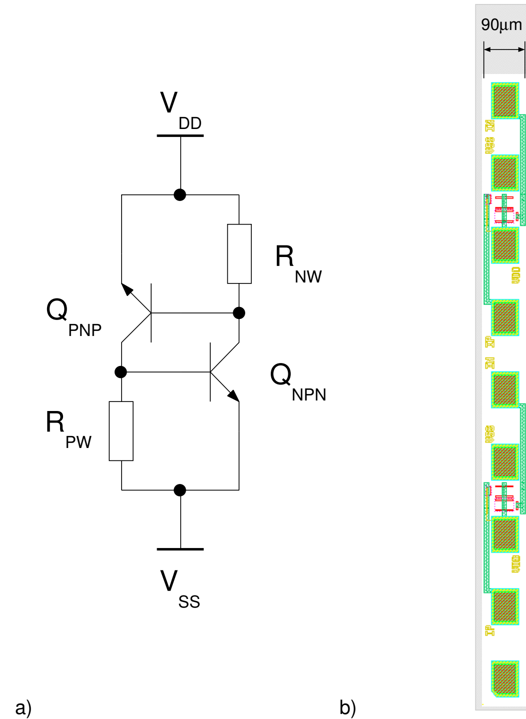

Figure 7: Test structure to review latch-up behaviour. a) Equivalent circuit of the SCR structure with lateral BJT Q_{NPN}, vertical BJT Q_{PNP}, nwell resistance R_{NW} and pwell resistance R_{PW} of the substrate. b) Layout of the SLM test structure.

depends on wafer material, general layout and guard techniques. These factors of influence are unaccounted in device models. Hence the latch-up influence can not be simulated offhand in standard design flows.

Beside the designed devices a number of unavoidable parasitic devices are built in a CMOS technology. These devices are interconnected and form bipolar structures (cf. Figure 7a) which are called silicon controlled rectifier (SCR).

An example layout is shown in Figure 7b. In general network simulation is insufficient supported in the PDKs. For a fixed layout it is possible to extract an equivalent circuit by hand and create device models via device simulation.

The latch-up behaviour can be characterized by test structures. Investigation and development of guard structures is described in [10]. The developed and optimized floating guard structures ensure a trigger current greater then $400mA@150°$.

That design capability is key know-how to design for automotive applications. Floating guard structures are also successfully implemented in circuits of the AS-interface product family [11, 12].

4.3 Bulk Current

Bulk current of MOS devices is sensitive to technological changes. An overview is given in [13]. It can be measured by the help of a simple test configuration which is illustrated in Figure 8a. The qualitative characteristic of the bulk current I_B vs. gate voltage V_G for fixed source V_S and drain V_D voltages is shown in Figure 8b.

A tolerance tube can be defined to distinguish between specified or problematic technology conditions. Important properties are the maximum bulk current I_{Bmax} at the related gate voltage V_{Gimax} and the shape of the characteristic. These parameters are shifted outside of the specified tube if for instance the tolerance of implantation or oxide thickness are violated.

The accuracy of device models (e.g. BSIM3v3) is not focused at the range of bulk current measurement. The marked area in Figure 8b shows the range of reduced accuracy of the bulk current.

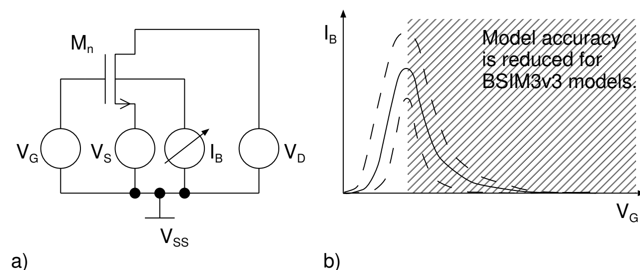

Figure 8: Test structure to measure bulk current. a) Measurement circuit. b) Schematic diagram of the bulk current with tolerance tube and area of reduced model accuracy.

5 Summary and Outlook

A method to consider PCM test structures in circuit design has been presented. This tool-supported flow helps to select the circuit's most important test structures. Main advantages are network simulation and data post processing analyses of the circuit design together with the test structures. Basis for the system is a library of test structures. Single devices and test circuits are supported.

Restrictions of the described way can be seen in accuracy and coverage of the device models. Not modeled effects like latch-up can not be simulated and analysed. These test structures need equivalent circuit and additional device models.

Taking into account the sensitivity of analog circuitry to technology we are striving to define the correlation of technology to analog design in an early design status. Our way is to utilize special SLMs for this purposes. Additional SLMs for checking the influence of physical phenomena (here latch-up) complete this methodology. In this way the early prediction of parameter yield will help us to decrease measurement costs.

Our intention is directed especially to the substrate current, which we take as a more integral parameter, which experiences the influence of certain technology processing steps. Here our goal is to define a tolerance tube, covering the so-called bell-shape curve.

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