Normally-off Transistor Topologies in Gallium Nitride Technology

Von der Fakultät für Elektrotechnik und Informationstechnik der
Rheinisch-Westfälischen Technischen Hochschule Aachen zur Erlangung des
akademischen Grades eines Doktors der Ingenieurwissenschaften genehmigte
Dissertation

vorlegt von

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Tag der mündlichen Prüfung: 13.02.2020

Diese Dissertation ist auf den Internetseiten der Universitätsbibliothek online verfügbar.

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1. Introduction

Digitalization is rapidly evolving with an ever-growing pace. Information technology is nowadays omnipresent in our everyday life starting from the smartphones in our pockets, over Internet-of-Things (IoT) devices [1] in our homes, to smart grids on a European level [2]. While one part of the emerging products drive an increasing demand for electrical energy, e.g. electric vehicles, CPU-intensive concepts like blockchain [3] or industry 4.0 solutions [4], another part is focused on clean power generation, distribution, storage and efficient conversion to fulfill the grand quest for green and sustainable energy.

III/V compound semiconductors offer a high flexibility in terms of material properties [5] and are perfectly suited for these demands. By mixing different compounds, a wide range of bandgaps, electron mobilities and saturation velocities can be achieved. Particularly the group III nitride semiconductors (GaN, InN, AlN) are a key enabler for compact and efficient high-power applications.

Driven by the GaN LED market [6, 7], constant progress in deposition and substrate technology was made and the maturity of the whole GaN process chain increased significantly in the past decades. During this development, the invention of lateral AlGaN/GaN heterostructure field-effect transistors (HFET) [8] was then seen as the next step in the radar and wireless communications sector [9, 10]. Today, GaN RF power amplifiers are commercially available and are also expected to be a backbone of the new 5G infrastructure [11]. These devices rely on the strong internal polarization of the nitrides to create a two-dimensional electron gas (2DEG) with high carrier densities and mobilities, which enable RF devices with high RF power densities.

For high-voltage power amplifiers however, which are needed in e.g. DC/DC converters, GaN technology has a major drawback. Lateral heterostructure devices are inherently normally-on, i.e. they conduct current when no gate voltage is applied. This raises safety concerns because in case of a gate driver malfunctioning, the GaN transistor is not automatically switched off and uncontrolled current flow can damage the entire system. Furthermore, normally-on transistors make circuit designs more complex because a negative-voltage supply is required. Thus, a lot of research was focused on creating normally-off devices in recent years. Different topologies have been established: a cascode configuration of a silicon normally-off MOSFET and a normally-on GaN HFET [12, 13], HFET with fluorine implantation under the gate [14, 15], gate-recessed (metal-insulator-semiconductor, MIS)-HFET with partial [16–18] or complete AlGaN barrier removal [19, 20], and the p-GaN-gated HFET [21–23].

All of these concepts are aimed at stable positive threshold voltages V_{th}, while retaining the benefits of the AlGaN/GaN heterostructure, with their individual pros and cons: The advantage of the cascode is the avoidance of normally-off GaN HFET by controlling the device through a normally-off silicon MOSFET, while the GaN transistor blocks high voltages in OFF-state. The drawback is an overall limitation by using silicon regarding e.g. operation temperature, radiation hardness and increased ON-resistance.

For the fluorine-implanted HFET, a major concern is the limited long-term stability of the threshold voltage due to fluorine diffusion and the introduction of additional defects in the AlGaN barrier due to the implantation.

Gate-recessed devices require a gate insulator to suppress gate leakage currents. But at the same time, theses gate insulators introduce additional challenges. At the interface between insulator and semiconductor, fixed charges and trap states are formed, which influence the threshold voltage of the devices. Depending on the charge condition at the interface, the insulator can shift the threshold voltage in positive or negative direction, which is either beneficial or detrimental for normally-off operation, respectively. Due to the transient nature of trap states, these effects can also lead to threshold voltage instabilities. Thus, methods to improve this interface are vital for device operation.

Another normally-off topology without a gate insulator is the p-GaN-gated HFET, effectively avoiding the challenges imposed by the insulator/AlGaN interface. In these devices, the 2DEG is depleted by a p-GaN capping layer as long as the AlGaN barrier thickness is below a certain limit. This leads to a trade-off between large positive threshold voltages (thin AlGaN barrier) and low ON-resistances (thick AlGaN barrier). Therefore, it is important to remove the p-GaN outside of the gate area to accumulate the 2DEG without further thinning of the underlying AlGaN. Additionally, this device shows higher gate leakage currents than the insulated-gate devices.

In this work, three out of these five topologies are investigated: the two gate-recessed MISHFET and the p-GaN-gated HFET. Core aspects are analyzed and processes to improve specific device properties are developed. For the two MISHFET, this involves techniques to optimize the insulator/AlGaN interface, while the p-GaN removal and gate module are focal for the p-GaN-gated HFET.

In the following, the structure and content of this work are outlined. First, an introduction into gallium nitride technology, a simple electrostatic model for the electron channel and its relation to the threshold voltage is given. This model is then modified to account for the gate insulator and the insulator/AlGaN interface charge density. In chapter 3, the characterization methods are explained and parameter definitions, particularly for the threshold voltage, are given.

Chapter 4 extends the electrostatic model by interface trap states, which change their charge condition during operation, and it is explained, how these effects impact the device properties of MISHFET. In the following, methods to improve the insulator/semiconductor interface are presented. A gate-recessed device, in which the threshold voltage is shifted in positive direction by the dielectric, is shown and the limitations of this shift are discussed. In the end of this chapter, a memory device concept is shown, which uses the interface trap states as charge storage.

In chapter 5, devices with a completely removed AlGaN barrier, so called MIS-hybrid HFET, are investigated. Due to the removed AlGaN under the gate, the electrons are conducted directly at the insulator/GaN interface which significantly reduces their mobility. To enhance the mobility, an amorphous AlN spike is introduced. For this process, a plasma-enhanced atomic layer deposition (PEALD) method is developed, which is then used for a MIS-hybrid HFET.

Chapter 6 discusses the p-GaN-gated HFET, its basic working principle and how different parameters influence the threshold voltage. A self-aligned device process with selective removal of the p-GaN cap layer is developed enabling reliable and reproducible manufacturing. Furthermore, elevated-temperature operation of the devices is investigated, since they are particularly suited for this application due to the lack of an insulator. At the end of this chapter, advanced concepts for further performance improvements are introduced and evaluated.

In the final chapter 7, the best suitable application for the different normally-off topologies presented in this work are evaluated.

2. Fundamentals of Group III Nitride Technology

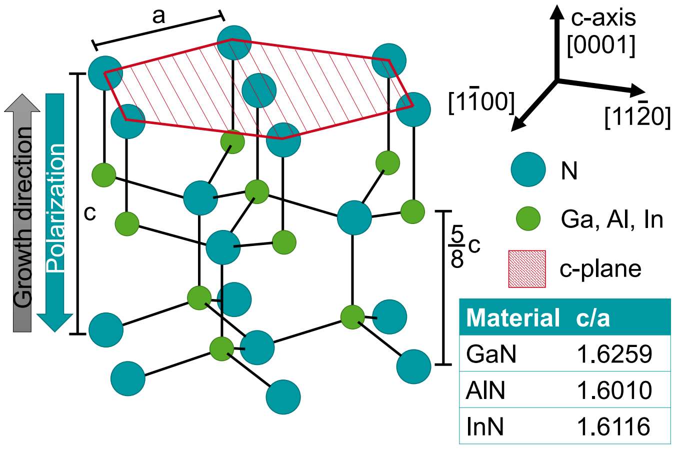
This chapter gives a brief introduction to the field of group III nitride semiconductors. First, their crystal structure and relevant properties are discussed. The unique polarization effects of group III nitrides are elaborated, which can be used in heterostructures to form a two-dimensional electron gas (2DEG). An electrostatic model is derived to show the dependence of the sheet carrier density inside the 2DEG on the layer design. Additionally, the scattering mechanisms, which limit the 2DEG electron mobility, are presented.

Afterwards, the working principle of a normally-on heterostructure field-effect transistor (HFET) is explained, how its threshold voltage can be determined from the electrostatic model, and how to achieve normally-off operation. In the end, the impact of a gate dielectric and surface passivation on the device properties is discussed and which parameters of the gate dielectric are important for normally-off HFET.

2.1. Crystal Structure

The group III nitrides GaN, AlN and InN can form three different crystal structures, the two cubic structures, zincblende and rocksalt, and the hexagonal wurtzite. The main focus of research and industry is on the thermodynamically-stable wurtzite, which is shown in Fig. 2.1.

A single layer of atoms in this structure consists either of the metal species (Ga, Al, In) or nitrogen. The lattice constant a describes the shortest distance between two atoms of the same layer, whereas the periodicity of the crystal in [0001]-direction is denoted by the lattice constant c. The crystal consists of two hexagonal close-packed arrangements (hcp), one for the metal species and one for nitrogen, which are shifted by 5/8 c in [0001]-direction. In this arrangement, one atom is tetrahedrally coordinated by four atoms of the other element.



Material	c/a
GaN	1.6259
AlN	1.6010
InN	1.6116

Figure 2.1.: Crystal structure of the wurtzite structure, typically grown in [0001] direction (metal polar). Blue spheres symbolize nitrogen atoms and the green spheres the metal species [24]. The table shows the c/a ratios for GaN, AlN and InN [25].

For an ideal hcp arrangement, in which all nearest-neighbor bond lengths are equal, the ideal ratio between the lattice constants c and a is given by $c_0/a_0 = 1.6330$ [25]. In the case of the group III nitride crystal, this hcp arrangement deviates from the ideal tetrahedral coordination and the wurtzite lacks inversion symmetry. In combination with the ionic character of the bond between metal atom and nitrogen, this results in the largest spontaneous polarization $\mathrm{P_{sp}}$ among the III-V semiconductors. The structures discussed in this work are all metal polar [26] for which the polarization points downward from top to bottom along the c-axis (in [000$\bar{1}$] direction, see Fig. 2.1).

The individual c/a ratios for GaN, AlN and InN are shown in the table of Fig. 2.1. As AlN shows the largest deviation from the ideal c/a ratio ($c_{\mathrm{AlN}}/a_{\mathrm{AlN}} = 1.6010$) and the Al-N bond has the highest ionicity, it has the strongest $\mathrm{P_{sp}}$. The Ga-N bond has the lowest ionicity and is the closest to the ideal c/a ($c_{\mathrm{GaN}}/a_{\mathrm{GaN}} = 1.6259$), thus it has the weakest $\mathrm{P_{sp}}$.

Since $\mathrm{P_{sp}}$ is related to the c/a ratio, it is influenced by applied mechanical strain which changes the lattice constants. Fig. 2.2 shows an unstrained (a), a compressively (b) and a tensely biaxially strained crystal (c). In the case of compressive biaxial strain, the lattice constant a decreases while lattice constant c increases. This brings c/a closer to the ideal ratio, which reduces the total polarization. Vice versa, tensile strain increases a while decreasing c, leading to a higher total polarization. This effect is called piezoelectric polarization $\mathrm{P_{pz}}$ [26].

The total polarization leads to fixed sheet charge densities $\mp\sigma_{\mathrm{x}} = \mathrm{P_{sp}} + \mathrm{P_{pz}}$ at the top and bottom c-plane surface of the group III nitride layers, respectively. Consequently, a

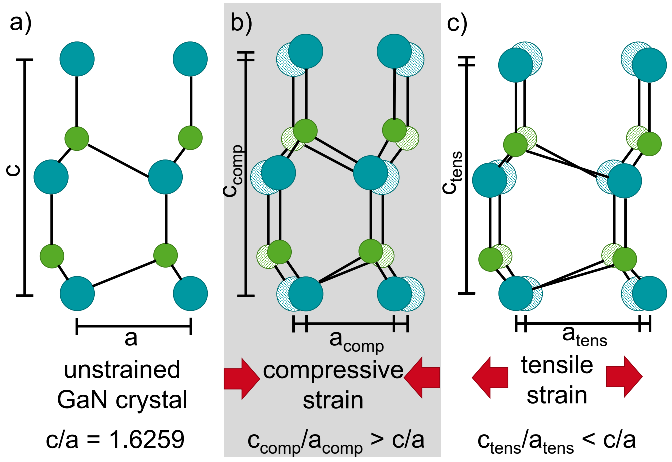


Figure 2.2.: Impact of mechanical strain on a GaN crystal and its lattice constants. Blue spheres symbolize N atoms and green spheres Ga atoms. a) Unstrained GaN crystal. b) Compressive biaxial strain increases the *c*/*a* ratio (closer to ideal) and therefore decreases the total polarization. c) Tensile biaxial strain lowers the *c*/*a* ratio (further away from ideal) which increases the total polarization.

single layer shows an internal electrical field $\mathscr{E}_x$ in c-direction [27]:

$$\mathscr{E}_x = \frac{\sigma_x}{\varepsilon_x} \tag{2.1}$$

where ε_x represents the layer permittivity.

2.2. Bandgap and Polarization

As lattice constant *a*, bandgap and polarization are important for predicting device behavior, the theory to calculate these parameters is presented in this section. A high degree of freedom of the group III nitrides originates from the possibility to tune the bandgap and polarization over a wide range. This can be achieved by switching from the binary compounds GaN, AlN and InN to the ternary compounds AlGaN, InGaN, AlInN. They show similar properties to their two binary components, depending on the respective content of each species.

The lattice constant *a* of ternary compounds can be calculated as a function of its composition x by linear interpolation bet ween the lattice constants of the individual binary compounds. This relation is expressed by Vegard's Law [28]:

$$a_{\mathrm{A_xB_{1-x}N}}(\mathrm{x}) = a_{\mathrm{AN}} \cdot \mathrm{x} + a_{\mathrm{BN}} \cdot (1-\mathrm{x}) \tag{2.2}$$

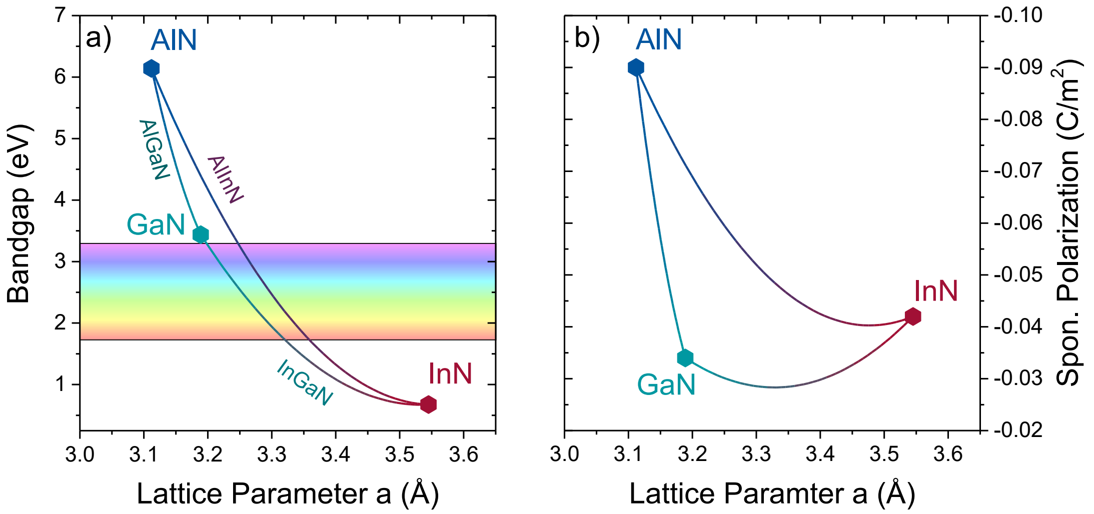


Figure 2.3.: Bandgap and the visible spectrum a) and spontaneous polarization b) of the group III nitrides vs. the lattice constant *a*. The points represent the binary compounds and the lines represent the different ternary compounds.

where A and B are the respective metal species of the ternary compound and N stands for nitrogen.

The bandgap and spontaneous polarization as a function of x are estimated by a similar expression with the addition of a bowing parameter *b* to account for non-linearities [29]:

$$X_{A_xB_{1-x}N}(x) = X_{AN} \cdot x + X_{BN} \cdot (1-x) - b_{ABN} \cdot x(1-x) \tag{2.3}$$

where X is the bandgap or spontaneous polarization, respectively.

By combining Eq. (2.2) + (2.3), the bandgap and the polarization can be expressed as functions of the lattice constant *a*, which is depicted in Fig. 2.3. The parameters of the binary compounds as well as the respective ternary bowing parameters, which were used in the calculations, are summarized in Tab. 2.1.

Fig. 2.3(a) shows that the InGaN bandgaps cover the entire visible spectrum (indicated by the colored area), which makes this compound particularly interesting for optoelectronic devices [35]. For power and radio-frequency (RF) applications, the wider bandgap and high polarization [see Fig. 2.3(b)] of the Al-containing compounds AlGaN and AlInN on top of a GaN layer are used. This layer combination forms a heterostructure, in which an electron channel can be accumulated without extrinsic doping, the so-called two-dimensional electron gas (2DEG). This is a unique characteristic of group III nitride semiconductors and represents a basic building block for transistors.

Table 2.1.: Lattice constant, bandgap and polarization of the binary nitride compounds as well as the bowing parameters for the ternary compounds [29–34].

Mat.	**Latt. Par. *a***	**Bandgap**	**Bandgap Bow. *b***	**Spon. Pol. P_{sp}**	**Pol. Bow. *b***
Units	(Å)	(eV)	(eV)	(C/m^2)	(C/m^2)
GaN	3.189	3.438	-	–0.034	-
AlN	3.112	6.140	-	–0.090	-
InN	3.545	0.675	-	–0.042	-
AlGaN	-	-	0.94	-	–0.021
InGaN	-	-	2.96	-	–0.037
AlInN	-	-	5.30	-	–0.070

2.3. Heterostructures and the Two-Dimensional Electron Gas

A widely-used heterostructure for electronic devices in the group III nitrides is AlGaN/GaN, in which a thin biaxially strained AlGaN layer is coherently deposited on a relaxed GaN layer (called pseudomorphic growth). The two layers are commonly referred to as AlGaN barrier and GaN buffer, respectively.

Fig. 2.4 shows the conduction band diagram of an AlGaN/GaN heterostructure and the individual fixed sheet charge densities σ_x, which are related to the polarization. The metal-polar surface of the structure is on the left, while the backside (substrate) is on the right, thus the polarization is directed from left to right. The triangular potential well of the 2DEG, which is populated by the mobile sheet carrier density n_s, is located at the heterointerface.

To explain the formation of the 2DEG, the derivation of an analytical expression from basic electrostatic equations is presented. This derivation is performed in analogy to [36]. Similar expressions will be used to explain various effects of investigated devices with more complex structures. It will be shown later that the sheet carrier density n_s is directly connected to the threshold voltage V_{th} of a HFET, which is the central aspect of this work.

First, Gauss' law is applied to the AlGaN/GaN interface which leads the following expression:

$$\varepsilon_{GaN}\mathscr{E}_{GaN} - \varepsilon_{AlGaN}\mathscr{E}_{AlGaN} = \sigma_{AlGaN} - \sigma_{GaN} - q \cdot n_s \qquad (2.4)$$

This gives the relation of n_s to the fixed sheet charges σ_{AlGaN} and $-\sigma_{GaN}$ and the electric

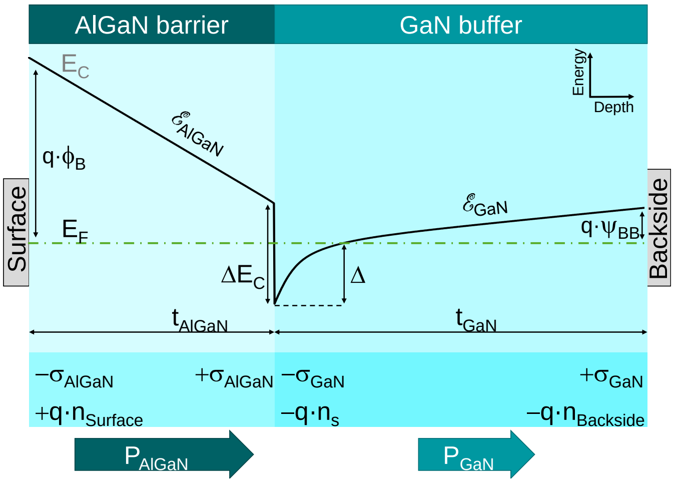


Figure 2.4.: Conduction band diagram of an AlGaN/GaN heterostructure, the individual fixed sheet charge densities σ_x and the 2DEG sheet carrier density n_s. $\mathscr{E}_{AlGaN}$ and $\mathscr{E}_{GaN}$ denote the electric fields in the respective layers, ΔE_C the conduction band offset between AlGaN and GaN, Δ the 2DEG quantum well depth, ϕ_B the surface potential, Ψ_{BB} the backside potential, and t_{AlGaN} and t_{GaN} the respective layer thicknesses.

fields $\mathscr{E}_{AlGaN}$ and $\mathscr{E}_{GaN}$ of the AlGaN barrier and GaN buffer, respectively. Here, q is the elementary charge and ε_x the respective permittivity.

σ_{AlGaN} and σ_{GaN} can be calculated by the theory given in section 2.2, whereas the electric fields are unknown. To determine $\mathscr{E}_{AlGaN}$ and $\mathscr{E}_{GaN}$, two Fermi level reference equations are formulated by following the conduction band edge in the respective layers and considering the surface potential ϕ_B and backside potential Ψ_{BB}. The quantum well thickness is neglected ($\ll t_{GaN}$).

For the AlGaN barrier, this leads to the following expression:

$$\phi_B - t_{AlGaN} \cdot \mathscr{E}_{AlGaN} - \Delta E_C/q + \Delta/q = 0 \tag{2.5}$$

The distance of the conduction band edge to the Fermi level at the surface is expressed by the surface potential ϕ_B. Then, the potential decreases linearly over the AlGaN barrier. The total potential drop is given by the product of the AlGaN barrier thickness t_{AlGaN} and its electric field $\mathscr{E}_{AlGaN}$. At the interface between AlGaN and GaN, the potential is lowered by the conduction band offset $\Delta E_C/q$ between the two materials. From the bottom of the quantum well, the distance back to the Fermi level is expressed by Δ/q [36]:

$$\Delta = \frac{n_s \cdot \pi\hbar^2}{m^*} \tag{2.6}$$

under the assumption that all electrons within the quantum well occupy the lowest sub-band [37]. Here, m^* represents the effective mass of electrons in GaN.

From there, the expression for the GaN buffer is given by:

$$t_{GaN} \cdot \mathscr{E}_{GaN} - \Psi_{BB} = 0 \tag{2.7}$$

The potential is linearly increased over the GaN buffer by the product of its thickness t_{GaN} and its electric field $\mathscr{E}_{GaN}$ and lowered back to the Fermi level at the backside by the potential Ψ_{BB}.

The remaining sheet charge densities $q \cdot n_{Surface}$ and $-q \cdot n_{Backside}$ ensure charge neutrality:

$$q \cdot n_{Surface} - q \cdot n_{Backside} - q \cdot n_s = 0 \tag{2.8}$$

Finally, combining Eq. (2.5) - (2.6) and solving for n_s leads to the following expression:

$$q \cdot n_s = \frac{\sigma_{AlGaN} - \sigma_{GaN} - \frac{\varepsilon_{AlGaN}}{t_{AlGaN}}(\phi_B - \Delta E_C/q) - \frac{\varepsilon_{GaN}}{t_{GaN}}\Psi_{BB}}{1 + \frac{\varepsilon_{AlGaN}}{t_{AlGaN}} \cdot \frac{\pi\hbar^2}{q^2 m^*}} \tag{2.9}$$

The first part of the equation shows an accumulation term, which is originating from the difference of the fixed sheet charge densities at the AlGaN/GaN interface $\sigma_{AlGaN} - \sigma_{GaN}$.

Next, two depletion terms can be identified which reduce n_s, the front side depletion by the surface potential and AlGaN barrier $\frac{\varepsilon_{AlGaN}}{t_{AlGaN}}(\phi_B - \Delta E_C/q)$ and the backside depletion by the GaN buffer and the backside potential $\frac{\varepsilon_{GaN}}{t_{GaN}}\Psi_{BB}$. The front side depletion is significant for most of the GaN heterostructure devices, whereas the backside depletion can often be neglected due to thick GaN buffers ($t_{GaN} \gg 1\,\mu m$, so-called thick-buffer approximation). The denominator accounts for band bending at the AlGaN/GaN interface and has a relatively small effect.

To illustrate the influence of the parameters from Eq. (2.9), Fig. 2.5 displays n_s calculated for different Al contents and thicknesses of the AlGaN Barrier. Fig. 2.5(a) shows n_s vs. AlGaN barrier thickness t_{AlGaN} for a typical Al content of 25%. As apparent from Eq. (2.9), its shape follows the function $f(t_{AlGaN}) = 1 - 1/t_{AlGaN}$, which saturates at $(\sigma_{AlGaN} - \sigma_{GaN})/q$ for $t_{AlGaN} \rightarrow \infty$ and is zero for $t_{AlGaN,crit} = 5.4\,nm$, i.e. the 2DEG is fully depleted. In the case of small t_{AlGaN}, n_s is more sensitive to variations of t_{AlGaN}.

For different Al contents in the barrier shown in Fig. 2.5(b), an individual critical thickness t_{crit} with $n_{s,Al_xGa_{1-x}N}(t_{crit}) = 0$ and saturation sheet carrier densities can be identified. The higher the Al content in the barrier, the smaller t_{crit} and the larger σ_{AlGaN} leading to large n_s.

In real heterostructures, the maximum barrier thickness is limited by the strain in the Al(Ga)N barrier, which is introduced by the lattice mismatch between barrier and buffer.

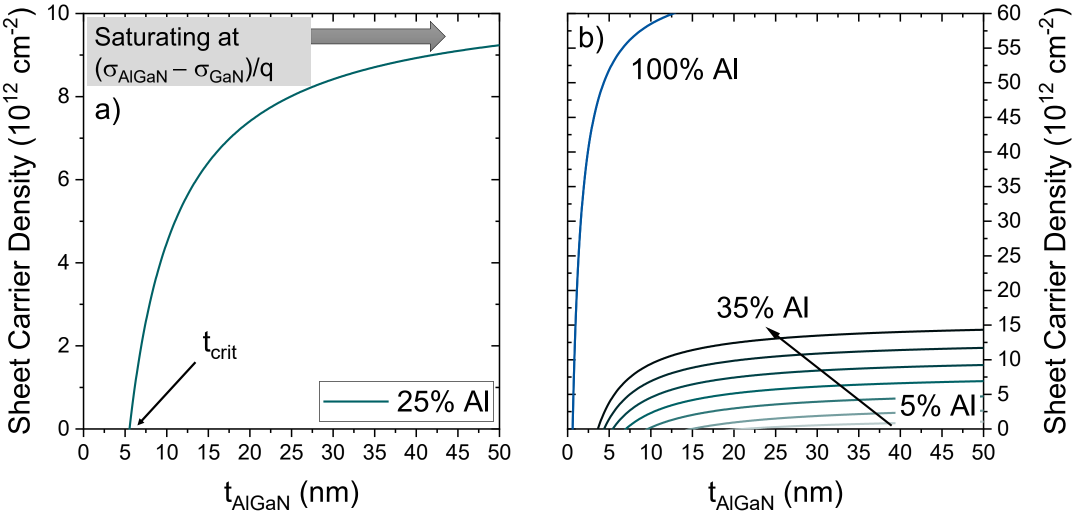


Figure 2.5.: Sheet carrier density vs. AlGaN barrier thickness for different Al contents. a) n_s vs. t_{AlGaN} for 25% Al content. Thinner barriers show an increased sensitivity to thickness variations. b) Different n_s vs. t_{AlGaN} for Al contents in the range of 5% to 35 % in 5% steps and for 100% Al. Parameters for calculating P_{sp} are shown in Tab. A.1 and calculation of P_{pz} is performed after [38]. $\phi_B - \Delta E_C/q$ is assumed to be constant as an increase of ΔE_C is commonly compensated by an increase in ϕ_B for increasing Al content in the barrier [39].

After a thickness t_{relax}, barrier relaxation starts which degrades the material quality [26]. As the difference between the lattice constants *a* of barrier and buffer increases with higher Al content (see section 2.2), t_{relax} decreases leading to an upper limit for n_s. The maximum reported 2DEG sheet carrier density is $n_s = 5.5 \cdot 10^{13}\,\mathrm{cm}^{-2}$ for an AlN/GaN heterostructure with a 7 nm barrier [40].

2.4. Electron Mobility in the 2DEG

Another distinctive feature of the 2DEG apart from the large sheet carrier density n_s is its high electron mobility μ. Due to the quantization inside the 2DEG potential well and the polarization-induced carriers (without extrinsic doping), the electron mobility can be theoretically increased from 1520 cm^{-2}/Vs in bulk GaN up to 2700 cm^{-2}/Vs in the 2DEG at room temperature [41].

The electron mobility is limited by three dominant scattering mechanisms: Coulomb, interface roughness and optical phonon scattering [37, 42, 43]. In Fig. 2.6, μ in dependence of temperature T and n_s is shown [37]. In Fig. 2.6(a) for T below 77 K, a constant μ of about 5200 cm^2/Vs is observed. Here, μ is limited by Coulomb scattering at low n_s and interface roughness scattering at high n_s [see Fig. 2.6(b)]. Optical phonon scattering

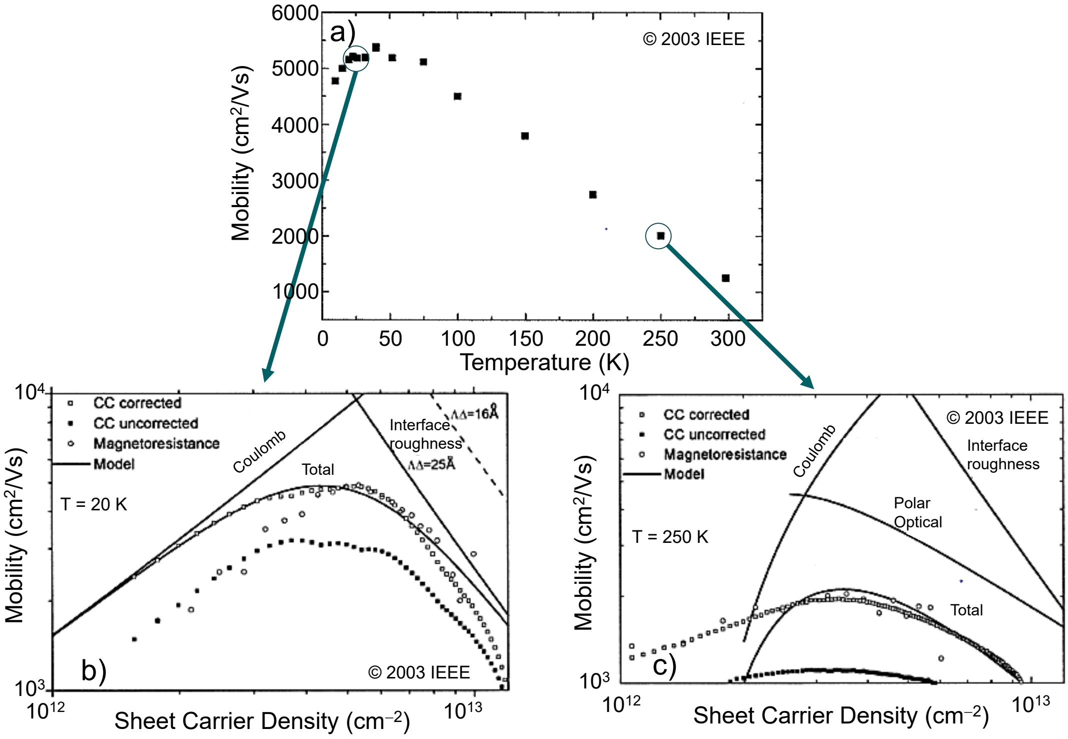


Figure 2.6.: Electron mobility in the 2DEG of an AlGaN/GaN heterostructure. a) Temperature dependence of the electron mobility. b) Sheet carrier density dependence at 20 K. b) Sheet carrier density dependence at 250 K. Images are taken from [37] and slightly modified.

can be neglected here due to low T of 77 K.

Coulomb scattering is caused by ionized impurities and the fixed interface charge densities, which are caused by the polarization. For increasing sheet carrier densities, a part of the free electrons screen the Coulomb field and the impact on μ of all free electrons is reduced ($\mu_{\mathrm{Coul}} \propto n_s^2$).

The interface roughness scattering ($\mu_{\mathrm{IR}} \propto n_s^{-2}$) in the group III nitrides is based on two different physical properties of the AlGaN/GaN interface: the actual roughness and random fluctuations due to the statistical Al distribution in the AlGaN barrier, the so-called alloy disorder scattering [44]. To understand the dependence of the interface roughness scattering on n_s, Fig 2.7(a) shows bulk electron density depth profiles for different n_s simulated by an 1D Poisson solver [45]. Additionally, the conduction band edge of the simulated AlGaN/GaN structure with the highest n_s is shown as an orientation. For increasing n_s, the quantum well of the 2DEG becomes energetically deeper (not shown here), which moves the centroid of the bulk electron density closer to the interface. Therefore, more electrons are scattered by the interface roughness and by alloy disorder, leading to a reduced μ in the 2DEG [42].

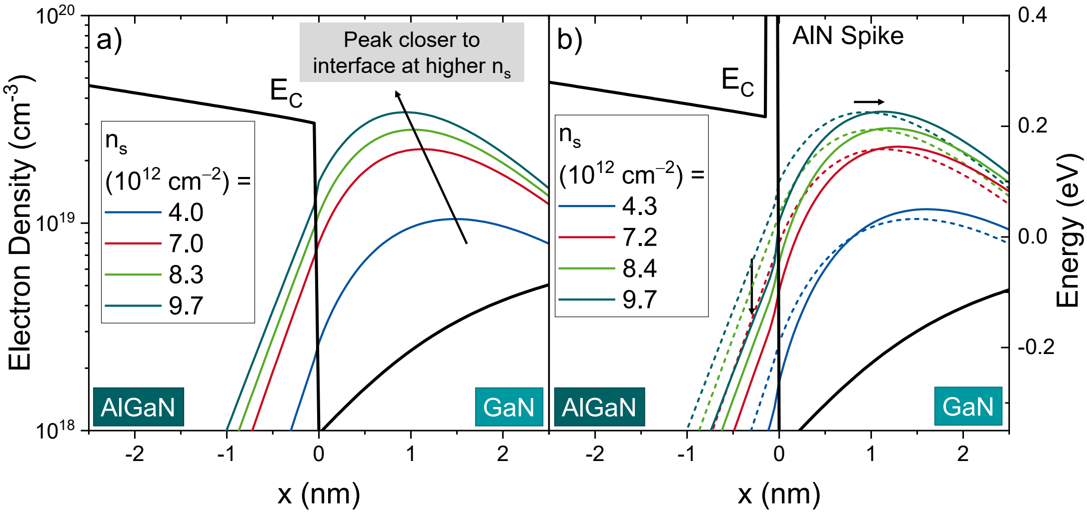


Figure 2.7.: Electron density profiles for different n_s. The conduction band edge is shown as orientation. a) AlGaN/GaN heterostructure. For higher values of n_s, the peak of the profile is shifted towards the interface. b) AlGaN/AlN/GaN heterostructure. Due to the AlN spike, the peak is shifted away from the interface and the electron density inside the barrier is reduced.

A method to mitigate this effect is the introduction of a very thin AlN spike between AlGaN barrier and GaN channel [46]. Fig. 2.7(b) shows the difference between the electron density profiles from Fig. 2.7(a) (dashed lines) and a simulated AlGaN/AlN/GaN structure (solid lines) for similar n_s. The AlN spike increases the AlGaN/GaN conduction band offset leading to a higher potential barrier for the electrons in the 2DEG. Therefore, the confinement of the electrons to the quantum well increases, which shifts the centroid away from the interface. Additionally, the electron density located inside the AlGaN is reduced. Furthermore, AlN as binary compound does not show random fluctuations in the composition, which reduces alloy disorder scattering. These two effects lead to an overall increase of μ at high n_s.

The main limiting factor for temperatures above 77 K is optical phonon scattering, which has an exponential temperature dependence [see Fig. 2.6(a)] [37]. This scattering mechanism is caused by the interaction of the electrons with the Coulomb field of the lattice polarization waves of polar semiconductors. However, the mobility is still affected by Coulomb and interface roughness scattering for low and high n_s, respectively [Fig. 2.6(c)]. Therefore, the reduction of interface roughness scattering is mandatory to achieve high mobilities at high carrier densities.

2.5. Heterostructure Field-Effect Transistor

The heterostructures with its key features, high sheet carrier density and electron mobility, from the previous section will now be employed in a heterostructure field-effect transistor (HFET). This device is depicted in Fig. 2.8 with ohmic source and drain contacts as well as Schottky gate contact.

The HFET can be divided into two regions: The intrinsic HFET under the gate electrode, which is responsible for the control of the conductive channel, and the access regions, which separate the source and drain from the gate.

The intrinsic HFET is shown in the center. It consists of the heterostructure with a gate metal on top of the AlGaN barrier. This system represents a plate capacitor with gate metal and 2DEG as plates and the AlGaN barrier as dielectric. By applying a gate voltage, the sheet carrier density n_s in the 2DEG can be modified [47]. The gate voltage V_{GS} in the electrostatic model is accounted for by an additional term in Eq. (2.9). It modifies the surface potential ϕ_B and leads to the following expression:

$$q \cdot n_s = \frac{\sigma_{AlGaN} - \sigma_{GaN} - \frac{\varepsilon_{AlGaN}}{t_{AlGaN}}((\phi_B - \mathbf{V_{GS}}) - \Delta E_C/q) - \frac{\varepsilon_{GaN}}{t_{GaN}}\Psi_{BB}}{1 + \frac{\varepsilon_{AlGaN}}{t_{AlGaN}} \cdot \frac{\pi\hbar^2}{q^2 m^*}} \tag{2.10}$$

Since the surface potential is now defined by the gate metal, ϕ_B is referred to as Schottky barrier height between metal and semiconductor. Positive V_{GS} increases n_s, while

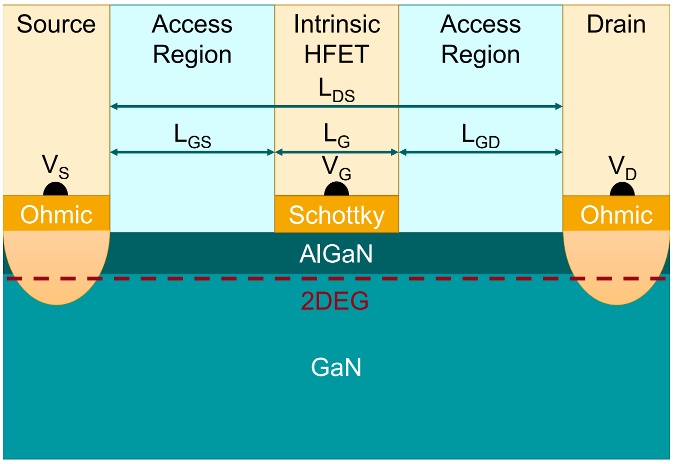


Figure 2.8.: Schematic of an AlGaN/GaN heterostructure field-effect transistor (HFET). The intrinsic HFET consists of the gate area which is responsible for the control of the device. The drain and source contacts are typically separated from the intrinsic HFET by the access regions. The relevant geometries are the drain-source distance L_{DS}, the gate length L_G, the gate-source distance L_{GS} and gate-drain distance L_{GD}.

negative V_{GS} decreases n_s.

The threshold voltage V_{th} for full depletion of n_s and therefore switching off the transistor can be extracted from Eq. (2.10) by setting $n_s = 0$ and solving for V_{GS}:

$$V_{th} = V_{GS} = \phi_B - \Delta E_C/q - \frac{t_{AlGaN}}{\varepsilon_{AlGaN}}(\sigma_{AlGaN} - \sigma_{GaN}) + \frac{t_{AlGaN}}{t_{GaN}} \cdot \frac{\varepsilon_{GaN}}{\varepsilon_{AlGaN}} \cdot \Psi_{BB} \tag{2.11}$$

With the thick-buffer approximation ($t_{GaN} \gg 1\,\mu m \gg t_{AlGaN}$), the expression above simplifies to:

$$V_{th} = \phi_B - \Delta E_C/q - \frac{t_{AlGaN}}{\varepsilon_{AlGaN}}(\sigma_{AlGaN} - \sigma_{GaN}) \tag{2.12}$$

Thicker AlGaN barriers and higher polarization differences between AlGaN and GaN lead to more negative V_{th} as they increase n_s at zero bias (cf. section 2.3).

Typical HFET with 25% Al content, 20 nm barrier thickness and a Ni gate [48, 49] have a calculated V_{th} of –2.7 V. This HFET will be taken as a reference to illustrate the influence of the parameters above on V_{th}. Due to the negative V_{th}, these HFET are classified as normally-on devices, i.e. they are in ON-state at zero gate bias.

For circuit design, not only normally-on but also normally-off transistors, i.e. transistors with a positive V_{th}, are needed. The advantages of normally-off HFET are the elimination of a negative-voltage supply requirement and OFF-state of the device in case of gate driver malfunctioning, which is necessary for power applications. Additionally, access to both, normally-on and normally-off devices, enables complementary designs, e.g. more efficient push-pull inverters [50] or cascodes [51].

This work focuses on the major normally-off concepts of group III nitride HFET. The impact of device design on V_{th} is presented, the individual V_{th} limitations are given and how certain aspects of such devices can be improved. The general approach for all of these concepts is the depletion of the 2DEG in the intrinsic HFET at zero gate bias, while maintaining the key features of the heterostructure: high electron mobilities throughout the whole device and high 2DEG sheet carrier densities in the access regions.

From Eq. (2.11), it is evident that three degrees of freedom exist to tune V_{th}: the Schottky barrier height ϕ_B which is dependent on the gate metal, and the AlGaN barrier with its polarization, which is dependent on the Al content, and its thickness.

To achieve a large ϕ_B, which increases V_{th}, a gate metal with a high work function is chosen. The gate contact metal for the AlGaN/GaN HFET in this work is Ni with a work function of 5.1 eV, which is capped by an Au layer. This represents a common gate metalization for GaN HFET [9, 17, 39, 52, 53]. The metal with the highest work function available is Pt with 5.65 eV [54], thus only a minor V_{th} shift to more positive voltages is possible [55]. By exchanging the Ni gate with a Pt gate in the example above, V_{th} would be shifted from –2.70 V to –2.15 V in an ideal case. Consequently, the AlGaN barrier is the most important design element for achieving normally-off operation.

Fig. 2.9 shows the dependence of V_{th} on the AlGaN barrier thickness and composition, under the assumption that ϕ_B-$\Delta E_C = 1$ eV = const. for varying Al contents [26, 36, 39]. The green area in Fig. 2.9(a) shows the normally-off regime, in which $V_{th} > 0$ V is achieved. Increasing the Al content in the barrier decreases the thickness t_{crit}, which is the maximum thickness that allows for normally-off operation. In the case of the example HFET with 25% Al content, a reduction of the barrier thickness below $t_{crit} = 5.4$ nm would be necessary. For an AlN barrier (100% Al), t_{crit} is approximately 1 nm.

In conclusion, normally-off HFET can be achieved by a low Al content and/or a thin AlGaN barrier. Reduction of the AlGaN barrier thickness is the better solution for two reasons: Reducing th Al content would also lower the conduction band offset at the AlGaN/GaN interface, which decreases the electron mobility due to inferior confinement in the 2DEG (see section 2.4). Secondly, the high carrier density and mobility need to be retained in the access regions. Thus, the normally-off modification has to be limited to the intrinsic HFET, i.e. the gate area. As the heterostructure is grown in a conventional epitaxial process [56], intentional lateral variations of the Al content cannot be achieved during a single growth process. On the other hand, the barrier can be locally thinned by

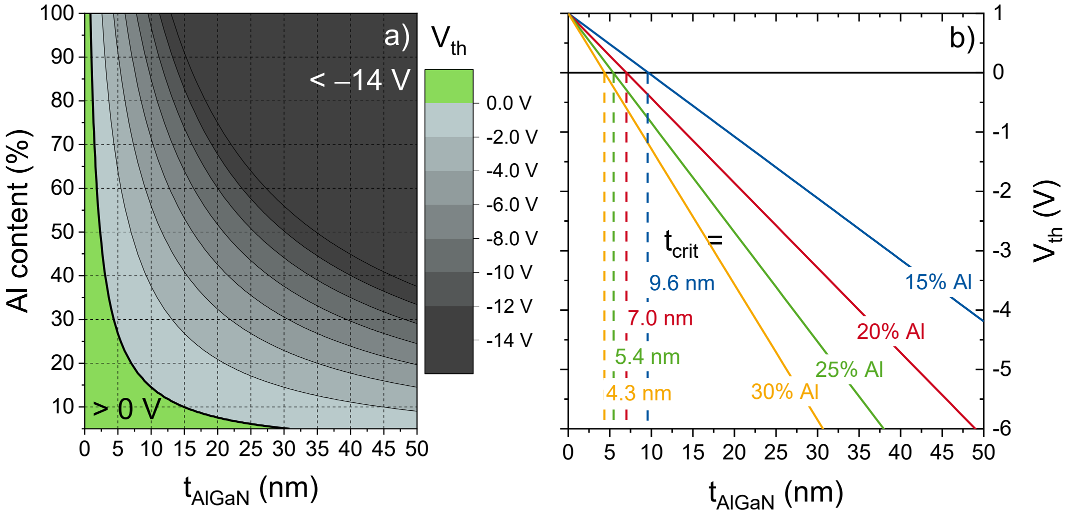


Figure 2.9.: Threshold voltage as a function of AlGaN barrier thickness and Al content. a) Contour plot of V_{th} vs. Al content and t_{AlGaN}. b) V_{th} vs. t_{AlGaN} for four different Al contents. t_{crit} denotes the barrier thickness for which normally-off operation is achieved.

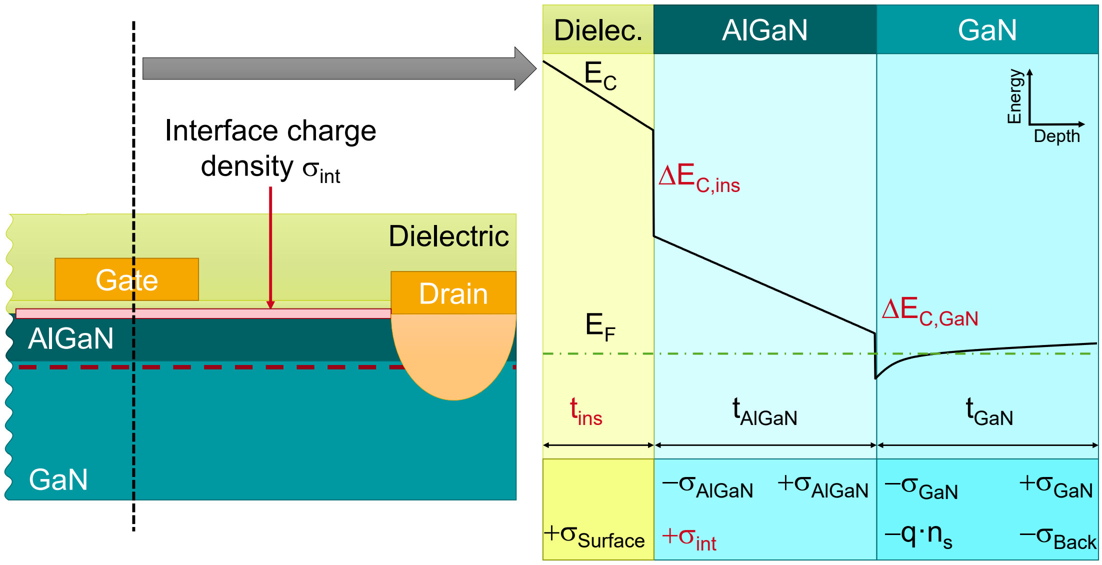

Interface charge density σ_{int}
Dielectric
Gate
Drain
AlGaN
GaN
Dielec.
AlGaN
GaN
E_C
Energy
Depth
$\Delta E_{C,ins}$
$\Delta E_{C,GaN}$
E_F
t_{ins}
t_{AlGaN}
t_{GaN}
$-\sigma_{AlGaN}$
$+\sigma_{AlGaN}$
$-\sigma_{GaN}$
$+\sigma_{GaN}$
$+\sigma_{Surface}$
$+\sigma_{int}$
$-q \cdot n_s$
$-\sigma_{Back}$

Figure 2.10.: Schematic of a passivated MISHFET and the corresponding conduction band diagram. New parameters in regard to Fig. 2.4 are the conduction band offset between dielectric and AlGaN $\Delta E_{C,ins}$, the dielectric thickness t_{ins} and the interface charge density σ_{int}.

patterned dry-etching during device processing [17], the so-called gate-recess etching. This leads to a high electron mobility and a vanishing/high sheet carrier density in the intrinsic HFET and access regions, respectively.

2.6. Dielectrics in an HFET

In contrast to a MOSFET, the basic functionality of the HFET requires no dielectric as the AlGaN barrier serves as an insulator between gate metal and 2DEG. Nonetheless, dielectrics are mandatory for real devices to mitigate parasitic effects.

2.6.1. Electrostatics of a MISHFET

Due to the introduction of a dielectric, the electrostatics described in the previous sections change. The new structure and extended band diagram are shown in Fig. 2.10. Additional parameters are the conduction band offset between dielectric and AlGaN $\Delta E_{C,ins}$, the dielectric thickness t_{ins} and an interface charge density σ_{int}. A derivation similar to Eq. (2.9) can be performed leading to the following expression [36]:

$$\begin{aligned} q \cdot n_s = \Bigg[& \sigma_{AlGaN} - \sigma_{GaN} - \frac{1}{\frac{t_{AlGaN}}{\varepsilon_{AlGaN}} + \frac{t_{ins}}{\varepsilon_{ins}}} (\phi_B - \Delta E_{C,ins}/q - \Delta E_{C,GaN}/q) \\ & - \frac{\frac{t_{ins}}{\varepsilon_{ins}}}{\frac{t_{AlGaN}}{\varepsilon_{AlGaN}} + \frac{t_{ins}}{\varepsilon_{ins}}} (\sigma_{AlGaN} - \sigma_{int}) \\ & - \frac{\varepsilon_{GaN}}{t_{GaN}} \Psi_{BB} \Bigg] \\ & / \Big[1 + \frac{1}{\frac{t_{AlGaN}}{\varepsilon_{AlGaN}} + \frac{t_{ins}}{\varepsilon_{ins}}} \cdot \frac{\pi \hbar^2}{q^2 m^*} \Big] \end{aligned} \tag{2.13}$$

Here, the barrier capacitance ($\varepsilon_{AlGaN}/t_{AlGaN}$) is substituted by the series capacitance of the barrier capacitance and the dielectric capacitance $(t_{AlGaN}/\varepsilon_{AlGaN}+t_{ins}/\varepsilon_{ins})^{-1}$. Furthermore, a term accounting for the dielectric is introduced (second row in Eq. (2.13)).

The interface charge density σ_{int} is the most important new variable, as it defines the dependence of n_s on the properties of the dielectric. In the case of $\sigma_{AlGaN} - \sigma_{int} = 0$, i.e. a charge-neutral interface between AlGaN and passivation, the corresponding dielectric term drops out of the equation. The only difference to the dielectric-free equation Eq. (2.9) is now the substitution of the barrier capacitance. In this case, increasing the barrier thickness t_{AlGaN} has a similar effect on n_s as increasing the dielectric thickness t_{ins}. For $\sigma_{AlGaN} - \sigma_{int} < 0$, the dielectric term has a positive sign leading to a higher n_s. For $\sigma_{AlGaN} - \sigma_{int} > 0$, the sign of the dielectric term is negative. Therefore, it represents another depletion term for n_s.

Apart from σ_{int}, the band alignment $\Delta E_{C,ins}$ between dielectric and barrier and the permittivity have to be taken into account. Fig. 2.11 shows different dielectrics, which are currently investigated in nitride technology [57–60], and their parameters in relation to an AlGaN barrier with 25% Al. The focus of this work is on silicon nitride (SiN_x) as surface passivation and aluminum oxide (AlO_x) as gate dielectric. SiN_x has proven to be one of the best surface passivation materials [36, 53, 64, 65] in group III nitride technology. AlO_x has one of the best insulating properties with a conduction band offset of 1.4 eV and a medium relative permittivity of 9.

In this work, only the interface charge density σ_{int} is considered. Commonly, dielectrics also have bulk volume charge densities [66], which are important if dielectrics with different thicknesses are investigated. Here, the dielectric thickness is kept constant during each experiment and the bulk charge densities are integrated into the interface charge density σ_{int}.

A more detailed explanation of the impact of the dielectrics on the device properties

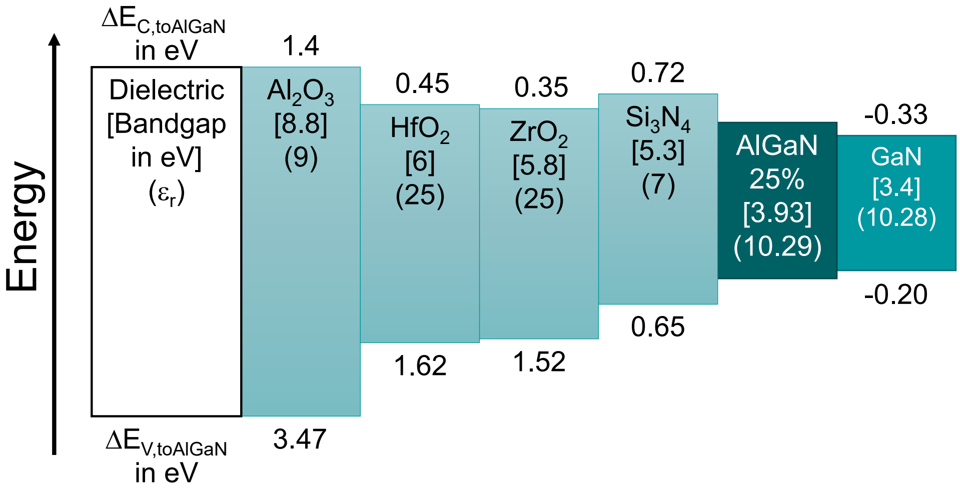


Figure 2.11.: Schematic of calculated band offsets of different dielectrics to AlGaN with 25% Al. Parameters of the dielectrics are taken from [61], whereas the AlGaN and GaN parameters are calculated. Image designed after [62, 63].

is given the following sections, starting with the surface passivation.

2.6.2. Surface Passivation of the Access Regions

In the access regions, the surface is not covered by a metal layer. Therefore, the surface potential is not fixed and can be influenced by absorbed ions or captured charge carriers in surface states. These surface states are originating from the abrupt end of the bulk semiconductor, which leads to unsaturated bonds (dangling bonds) and defects in the crystal structure. In the case of nitride semiconductors, the surface is particularly prone to capture electrons due to polarization [67].

In an HFET during device OFF-state at high drain bias, the gate metal edge emits electrons into these surface states (depicted in Fig. 2.12). The negative surface potential built up by the trapped electrons then leads to a depletion of the 2DEG. When the device is switched to ON-state, these electrons are not immediately discharged and lead to an increases resistance of the access regions. This effect is called virtual gating as the negative surface potential acts like a gate with negative bias [67]. A technique to mitigate virtual gating is surface passivation. By depositing a dielectric on top of the AlGaN barrier, a majority of the surface traps are saturated. Furthermore, the actual device surface is shifted away from the 2DEG, which reduces its influence on n_s [see Eq. (2.9)]. Here, the focus is not on the insulating properties, but on a dielectric/AlGaN interface with low trap densities and fast discharging of trapped electrons during switching.

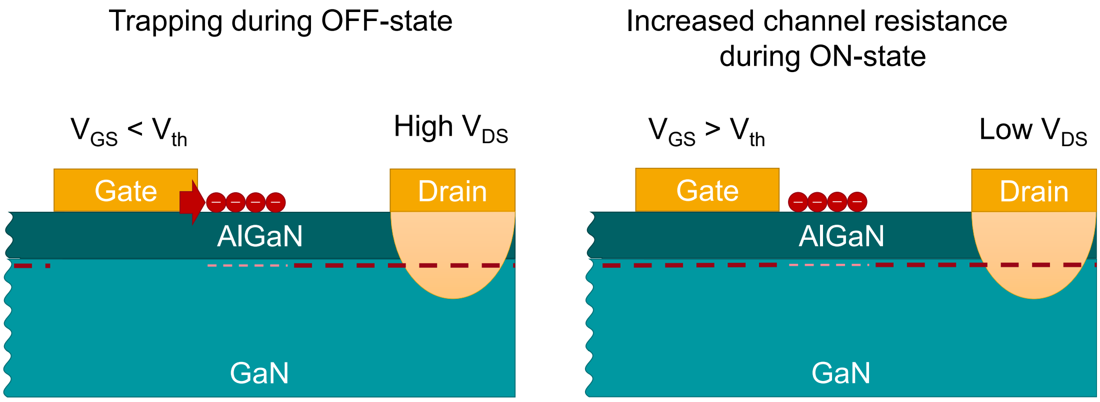


Figure 2.12.: Virtual gating effect during OFF-state. Electrons are emitted from the gate edge and trapped in surface states on top of the AlGaN barrier. The negative surface potential depletes the 2DEG leading to an increased channel resistance during the ON-state.

In addition to the reduced virtual gating, the experimental results using silicon nitride passivation show an increased n_s. This effect is expected from the electrostatic model of Eq. (2.13) for $\sigma_{\mathrm{AlGaN}} - \sigma_{\mathrm{int}} \leq 0$ and is particularly beneficial for HFET with thin AlGaN barriers, since n_s can be increased in the access regions by the passivation leading to an improved R_{ON}.

However even in a passivated device, charge trapping can occur at the SiN/barrier interface. The trapped electrons reduce σ_{int}, which increases the difference $\sigma_{\mathrm{AlGaN}} - \sigma_{\mathrm{int}}$ and decreases n_s. Thus, the passivation should have a positive fixed charge σ_{int} greater than σ_{AlGaN} and ideally, no electron traps at the interface.

2.6.3. Gate Insulation of the intrinsic HFET

In the intrinsic HFET, the gate leakage current can be reduced by switching to a metal-insulator-semiconductor HFET (MISHFET). This is particularly important for normally-off devices, which are realized by gate-recess etching. Due to the thin barrier, the leakage current is increased in comparison to the normally-on HFET. Additionally, the gate diode of the HFET is no longer biased in reverse direction to deplete the 2DEG, but needs to be biased in forward direction for 2DEG accumulation. This leads to high gate leakage currents during the device ON-state [17]. The additional dielectric of the MIS contact is able to suppress these leakage currents.

The requirements for an optimal gate insulator are a large bandgap with a conduction band offset over 1 eV to the barrier for electron blocking capabilities at positive gate bias, low bulk defect densities and a high quality interface between the insulator and semiconductor [68].

The strongest impact of the dielectric on the device characteristics of the intrinsic HFET, is the threshold voltage shift ΔV_{th}. Solving Eq. (2.13) for the threshold voltage in analogy to section 2.5 gives the following equation:

$$V_{th} = \phi_B - \Delta E_{C,ins}/q - \Delta E_{C,GaN}/q - \frac{t_{AlGaN}}{\varepsilon_{AlGaN}}(\sigma_{AlGaN} - \sigma_{GaN}) - \frac{t_{ins}}{\varepsilon_{ins}}(\sigma_{int} - \sigma_{GaN}) \qquad (2.14)$$

The threshold voltage is now not only defined by the AlGaN barrier, but also by the insulator thickness and the interface charge σ_{int}.

For the threshold voltage dependence on the insulator properties, it can be differentiated between three cases in analogy to Eq. (2.13). They are shown in Fig. 2.13: In the first case $\sigma_{int} = \sigma_{GaN}$, the term equals zero and no ΔV_{th} occurs. For $\sigma_{int} > \sigma_{GaN}$, V_{th} is shifted to more negative values with increasing insulator thickness, whereas for $\sigma_{int} < \sigma_{GaN}$, V_{th} is shifted to more positive values.

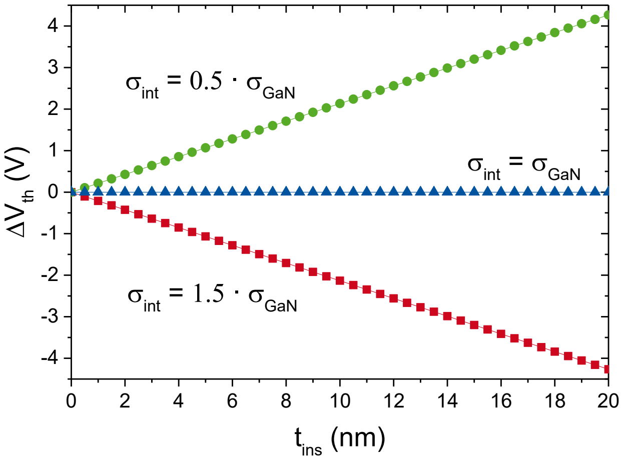


Figure 2.13.: Threshold voltage shift ΔV_{th} in dependence of the insulator thickness t_{ins}. The plot shows three different cases for the interface charge density σ_{int}: $\sigma_{int} < \sigma_{GaN}$, $\sigma_{int} = \sigma_{GaN}$ and $\sigma_{int} > \sigma_{GaN}$.

Therefore, the gate dielectric can have a large impact on the operation mode of the device. In case of a positive V_{th} shift, the dielectric is beneficial for the normally-off HFET as it shifts V_{th} to even more positive voltages or can enable normally-off operation with thicker AlGaN barriers. In case of the negative V_{th} shift however, the dielectric can turn the initially normally-off HFET into a normally-on MISHFET. Thus, the control of σ_{int} is particularly critical for normally-off devices.

In this chapter, an introduction into the group III nitrides was given. The uniquely-high polarization effects can be used in heterostructure to create a conducting channel, the 2DEG, without doping. The electrostatics of the heterostructure were explained and it was shown that the AlGaN barrier composition and thickness have the highest impact on the sheet carrier density inside the 2DEG. In addition, the 2DEG also shows a high electron mobility, for which the main scattering mechanisms and limitations were introduced. Based on this heterostructure with its two key features, high sheet carrier density and electron mobility, the HFET was explained with focus on its threshold voltage. A method to shift the threshold voltage from negative to positive was shown, i.e. turning a normally-on into a normally-off device through thin barriers. In the last part, the requirement for dielectrics in a normally-off HFET and their impact on the device properties, particularly the impact on V_{th}, was explained.

3. Electrical Characterization Methods

In this chapter, the characterization methods for the different device properties are presented and the corresponding measurements plots explained. Capacitance-Voltage (C-V) profiling is a powerful tool to investigate the heterostructures in terms of electron density n_s, interface charge density σ_{int} and threshold voltage V_{th}. Current-voltage (I-V) measurements are used to characterize the manufactured HFET and extract its relevant parameters. Pulsed-I-V gives access to analyzing dispersive behavior which is only visible through switching between stress and measurement bias points.

3.1. Capacitance-Voltage (C-V)

Capacitance-Voltage (C-V) profiling enables a profound investigation of the accumulation and depletion processes in nitride heterostructures. The underlying principle of C-V measurements is a small-signal alternating-current (AC) excitation of charge carriers and the measurement of the total transported charge. From the two parameters, a corresponding capacitance can be extracted. In C-V profiling, this measurement is performed for different direct-current (DC) bias points. This allows for analyzing the depletion or accumulation of charge carriers depending on their polarity as well as their depth profiles.

Fig. 3.1 depicts a schematic of an AlGaN/GaN heterostructure with a simple equivalent circuit. The cross section contains a large-area diode (LAD, see A.5) used for the C-V measurements and the plot shows simulated C-V curves. The simulations are performed for a 20 nm AlGaN barrier with varying Al content in Sentaurus TCAD [69]. The measured capacitance equals a plate capacitor with the Schottky contact as one plate and the 2DEG as the other with AlGaN as dielectric:

$$C = \varepsilon_0 \varepsilon_r \cdot \frac{A}{t_{AlGaN}} \tag{3.1}$$

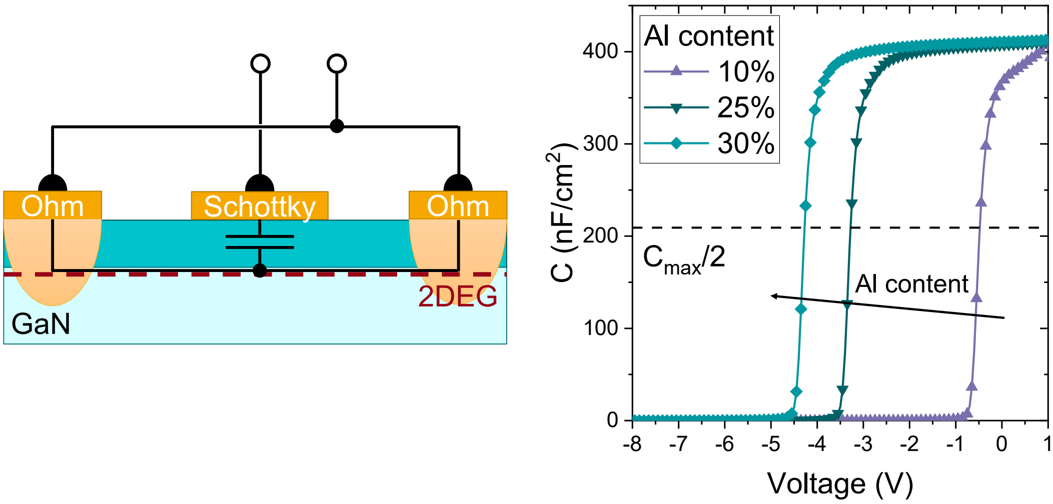


Figure 3.1.: Schematic of an AlGaN/GaN heterostructure with a simple equivalent circuit and simulated C-V plots of the device. The simulations are performed for a 20 nm AlGaN barrier with varying Al content.

where A is the device area (Schottky area for a LAD) and t_{AlGaN} the AlGaN thickness.

On the left side of the C-V plots, towards negative DC bias voltage, the 2DEG is depleted and therefore $C = 0\,nF/cm^2$. At some point, the capacitance rises and saturates when the 2DEG is fully formed. The threshold voltage V_{th} for the LAD is defined at the point on which half of the maximum capacitance $C_{max}\,/\,2$ is reached. As described in the previous section, the varying of the Al content inside the barrier changes the polarization difference and therefore shifts V_{th}. The slight increase in capacitance after V_{th} towards zero is originating from a shift in the electron density maximum towards the AlGaN barrier for higher carrier concentrations (see section 2.4). The 10% Al content curve rises faster in the accumulation regime because of the weak carrier confinement due to only a small conduction band offset between AlGaN and GaN. In the positive bias regime, the Schottky gate contact becomes conductive and the leakage current invalidates the C-V measurement. This limits the measurement to approximately 1 V.

For a MISHFET device, an additional gate insulator is deposited on top of the AlGaN barrier. In the accumulated 2DEG state, a series capacitance of AlGaN and insulator is now measured:

$$C = \frac{C_{ins} \cdot C_{AlGaN}}{C_{ins} + C_{AlGaN}} \tag{3.2}$$

Furthermore, a third state in the C-V curve other than 2DEG accumulation and depletion can be observed, the so-called spill-over regime [70]. The different regimes with the corresponding equivalent circuits are depicted in Fig. 3.2. Under larger forward bias of

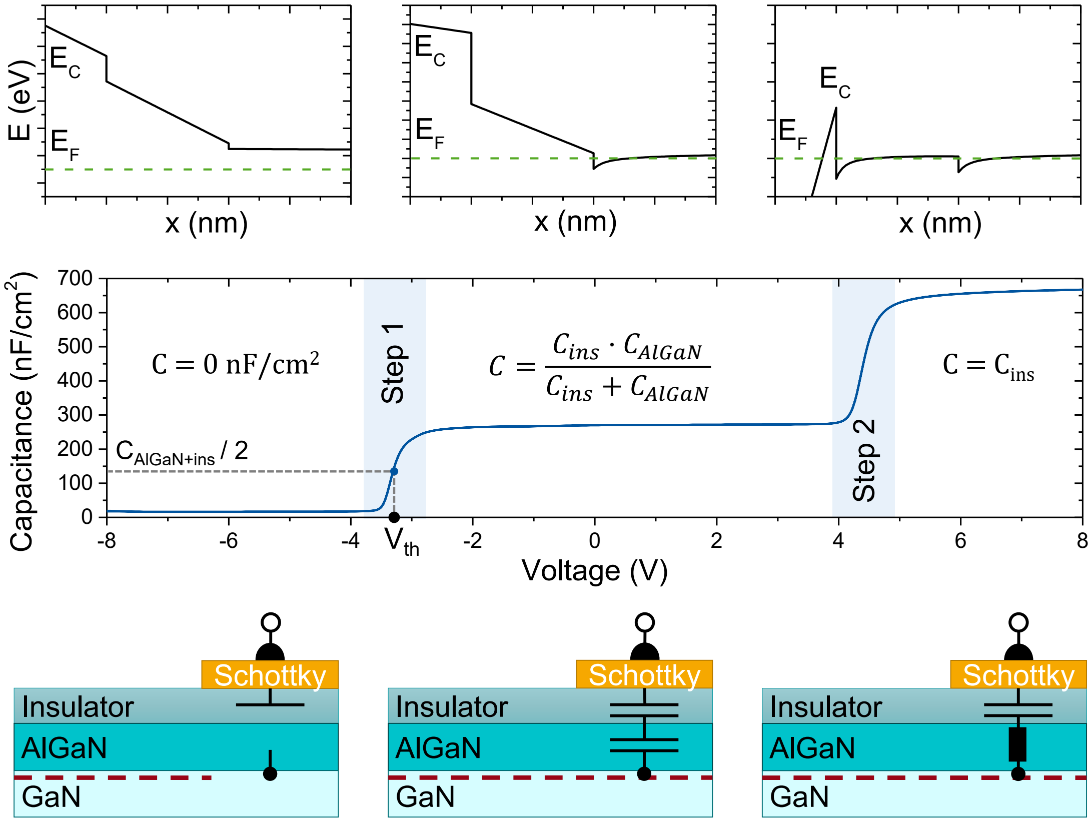


Figure 3.2.: Simulated C-V curve of an insulator/AlGaN/GaN structure. Above, simulated band diagrams for the different states are shown whereas below, the corresponding equivalent circuits are depicted.

the gate diode, the electrons are able to surpass the AlGaN barrier and are transfered from the 2DEG to the insulator/AlGaN interface. The capacitance rises and now only the insulator capacitance is measured, which is connected to the 2DEG over the AlGaN barrier resistance.

The visibility of this second capacitance plateau after step 2 is dependent on the measurement frequency and AlGaN barrier resistance [70]. In a quasi-static C-V measurement, the second plateau is always visible, whereas it can be suppressed at higher frequencies due to the $R_{AlGaN} \cdot C_{ins}$ time constant of barrier and insulator. For large time constants, the electrons at the insulator/AlGaN interface cannot follow the applied AC signal and therefore, only the series capacitance of oxide and barrier is measured in the spill-over regime. Thus, it is beneficial for the C-V characterization to measure at lower frequencies.

Furthermore, the MIS theory of Eq. (2.14) is also valid in this case. By solving this equation for σ_{int}, it can be determined from V_{th} extracted at $C_{\text{AlGaN+ins}}/2$:

$$\sigma_{\text{int}} = \frac{\varepsilon_{\text{ins}}}{t_{\text{ins}}} \cdot [\phi_B - \Delta E_{C,\text{ins}}/q - \Delta E_{C,\text{GaN}}/q - V_{\text{th}} - \frac{t_{\text{AlGaN}}}{\varepsilon_{\text{AlGaN}}}(\sigma_{\text{AlGaN}} - \sigma_{\text{GaN}})] + \sigma_{\text{GaN}} \tag{3.3}$$

3.2. Current-Voltage (I-V)

For the basic characterization of transistors, commonly three different direct current-voltage (I-V) measurements are employed as shown in Fig. 3.3:

- Input characteristics which describe the gate current in dependence of the gate-source voltage I_G vs. V_{GS}.
- Output characteristics which show the drain current in dependence of the drain-source voltage I_D vs. V_{DS} at constant V_{GS}.
- Transfer characteristics which contain the drain current in dependence of the gate-source voltage I_D vs. V_{GS} at constant V_{DS}.

From the transfer characteristic in linear scale in Fig. 3.3(a), V_{th} can be estimated by linear extrapolating the tangent in the point of maximum transconductance $g_{m,\text{max}}$ towards the x-Axis. The value of $g_{m,\text{max}}$ is an important characteristic for the switching behavior of the transistor, since it shows how effectively the output current I_D can be controlled by the input voltage V_{GS}.

Fig. 3.3(b) shows a semilogarithmic plot of the transfer characteristic (blue) as well as the input characteristic (red). From the plot, several electrical properties can be extracted. At negative voltages, the flat line of the current represents the OFF-current of the device and is responsible for the OFF-state power dissipation.

Furthermore, the sub-threshold swing SS can be estimated from the slope of the drain current curve below V_{th} and is given in millivolt V_{GS} per decade I_D (mV/dec). A lower value shows a better current control, and is physically limited to a minimum of 60 mV/dec at room temperature [71] for conventional field-effect transistors.

Two additional threshold voltage criteria are defined at a constant current of 1 mA/mm and 1 µA/mm for a soft- and hard OFF-state, respectively. Since the electrostatic theory for V_{th} assumes a sheet carrier density of zero [see Eq. (2.11)], the hard OFF-state V_{th} is the most suitable criterion for comparison of theoretical and experimental values.

The output characteristics are shown in Fig. 3.3(c). The plot depicts I_D vs. V_{DS} curves for different fixed V_{GS} values. The current rises linearly for low V_{DS} (linear regime) and eventually saturates at higher values (saturation). For high I_D and V_{DS}, the curve is

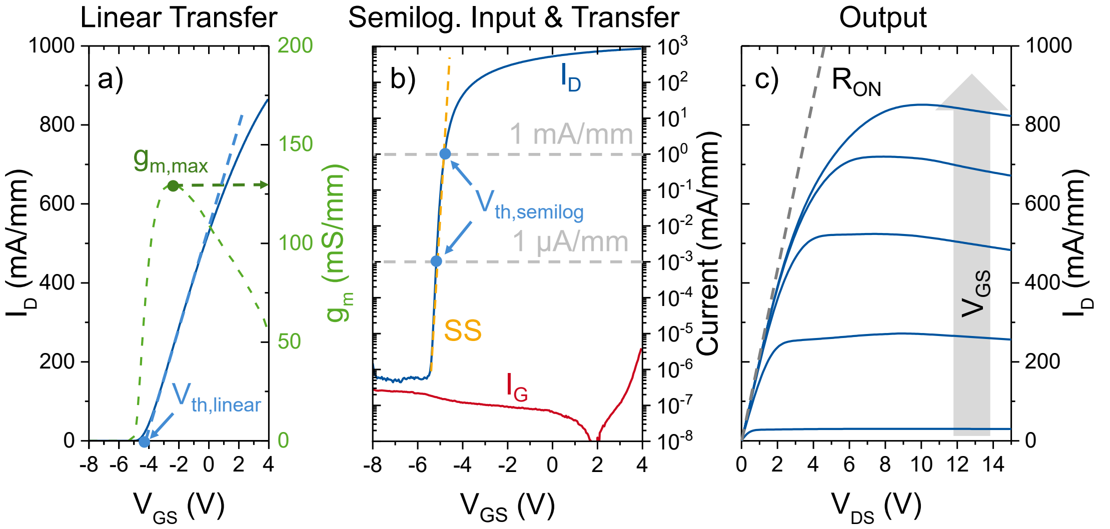


Figure 3.3.: Input, output and transfer characteristics of an example MISHFET. a) Transfer characteristics in linear scale (blue) with the corresponding transconductance (green). V_{th} can be estimated by linear extrapolation of the tangent in the point of maximum transconductance $g_{m,max}$ towards the x-axis. b) Input (red) and transfer characteristics (blue) in semilogarithmic scale. Two threshold voltage criteria are defined at a constant current of 1 mA/mm and 1 µA/mm for a soft- and hard OFF-state, respectively. The sub-threshold swing SS is estimated from the slope of the drain current curve below V_{th} (orange). c) Output characteristic in linear scale. The ON-resistance R_{ON} is calculated from V_{DS} at $I_D = 100$ mA/mm for the curve with the highest V_{GS}.

declining due to self-heating of the device. From the linear regime, the ON-resistance R_{ON} of the device can be extracted. Commonly, V_{DS} at $I_D = 100$ mA/mm is extracted for the curve with the highest V_{GS} and the resistance times gate width is calculated (values in Ωmm). R_{ON} is an important parameter for power electronics since it is a major contributor to losses and should be as low as possible.

Three-Terminal- and Vertical Breakdown

Breakdown measurements are performed to estimate the maximum operation voltage of electrical devices. Fig. 3.4 shows a schematic cross section of an HFET and example measurement curves. The upper limit can be either given by a lateral- or a vertical current flow and is extracted by two different types of measurement. First, a three-terminal breakdown measurement is performed in which the HFET is kept in OFF-state ($V_{GS} < V_{th}$) and V_{DS} is steadily increased until a drain current I_D of 1 mA/mm is reached (soft breakdown criterion). Additionally, the gate current is measured while the substrate is grounded. During the measurement, the probes and DUT (device-under-test) are immersed in Fluorinert^{TM} to avoid breakdown through air.

If the drain and gate current rise at the same time and show similar values, i.e. the drain current is primarily flowing into the gate, the breakdown is limited by the device surface, AlGaN barrier or passivation depicted in Fig. 3.4(1). If the drain current rises independently from the gate current, the breakdown is buffer related and can be lateral between drain and source [see Fig. 3.4(2)] or vertical between drain and substrate [see Fig. 3.4(3)]. To differentiate the two possibilities, an additional vertical breakdown measurement is performed, in which the gate and source terminals are disconnected and the voltage between drain and subtrate V_{vert} is increased until a vertical current I_{vert} of 1 A/cm^2 is measured. If the shapes of I_D and I_{vert} are similar, a vertical leakage path is dominant, otherwise a lateral one. Therefore, the example curve shows a limitation by vertical breakdown.

3.3. Pulsed-I-V

Power transistors are commonly operated in switched mode, which is accompanied by charging and discharging of electron traps within the structure. To emulate "real" device operation and investigate trap dynamics, pulsed current-voltage (pulsed-I-V) output characterization is performed [72, 73]. Here, the device is kept in a quiescent bias point for a longer period of time and then short-pulsed to the individual measurement points.

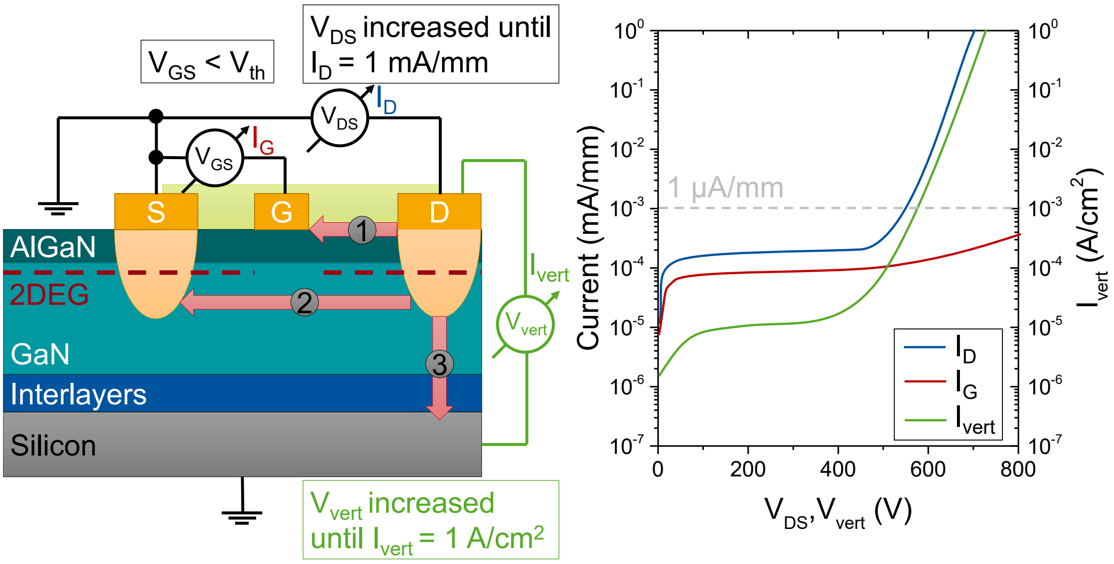

V_GS < V_th
V_DS increased until I_D = 1 mA/mm
V_DS
I_D
V_GS
I_G
S
G
D
1
2
3
AlGaN
2DEG
GaN
Interlayers
Silicon
I_vert
V_vert
V_vert increased until I_vert = 1 A/cm²
Current (mA/mm)
I_vert (A/cm²)
1 µA/mm
10^0
10^-1
10^-2
10^-3
10^-4
10^-5
10^-6
10^-7
0
200
400
600
800
V_DS, V_vert (V)
I_D
I_G
I_vert

Figure 3.4.: Schematic cross section of an HFET with a breakdown measurement configuration and a schematic measurement result.

The duty cycle between quiescent and measurement point is usually in the scale of 0.1%. The measurement is then repeated for various quiescent points to investigate different effects. This pulsed measurement scheme is depicted in Fig. 3.5.

In an isothermal measurement, the quiescent bias point is chosen to $V_{DS} / V_{GS} = (0, 0)$ [see Fig. 3.5(1)]. In a DC setup, the constant current flow leads to a self-heating of the device, which increases the resistance of the 2DEG. By pulsing from (0, 0) to the individual measurement points for only short periods of time, an output characteristic without any self-heating can be measured (blue curve in Fig. 3.5).

For a class B-type measurement [74], the quiescent bias point is chosen to a gate-source voltage below V_{th} to switch the device off, and a high drain-source voltage $V_{DS} / V_{GS} = (<V_{th}$, high value) [see Fig. 3.5(2)]. During this OFF-state stress, electrons can be injected from the gate edge into surface traps or the passivation and from the drain edge to buffer traps. These captured electrons deplete the 2DEG, thus a lower current is sensed during the ON-state measurement pulses (virtual gating, see section 2.6.2) and R_{ON} is increased. The difference in saturation current is called current collapse, while the ratio $R_{ON,classB}/R_{ON,(0,0)}$ is called dynamic R_{ON} increase.

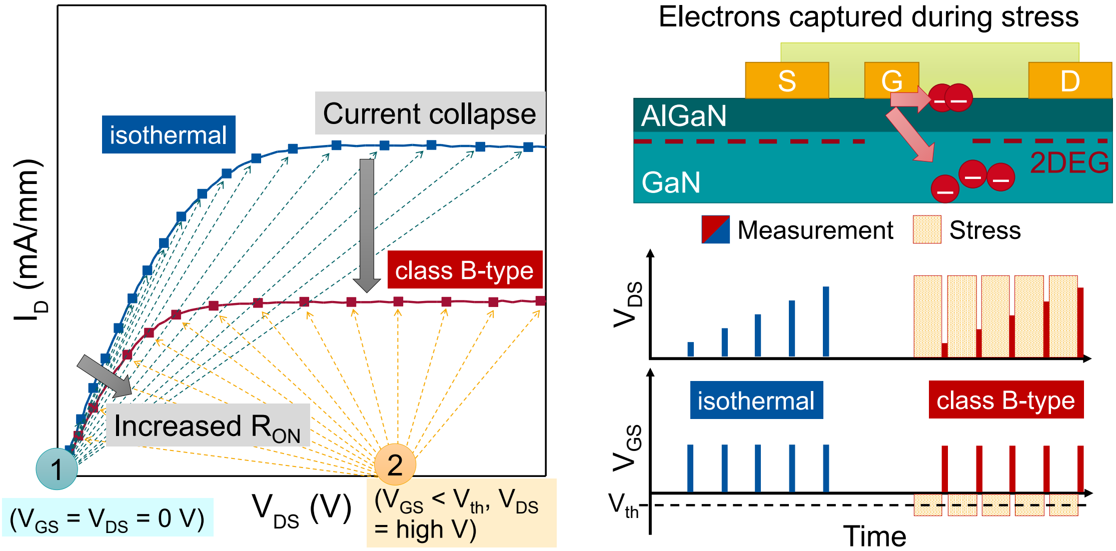

isothermal
Current collapse
class B-type
Increased R_ON
I_D (mA/mm)
V_{DS} (V)
1
($V_{GS} = V_{DS}$ = 0 V)
2
($V_{GS} < V_{th}$, V_{DS} = high V)
Electrons captured during stress
S
G
D
AlGaN
GaN
2DEG
Measurement
Stress
V_{DS}
isothermal
class B-type
V_{GS}
V_{th}
Time

Figure 3.5.: Illustration of the pulse measurement scheme. The left side shows example measurement curves for the isothermal (1) and class B-type measurement (2). The right side shows the electron capture during OFF-state stress and a timing diagram of V_{DS}/V_{GS} vs. time with the alternating stress/measurement scheme.

4. Threshold Voltage Engineering and Stability of MISHFET

In the fundamentals chapter, it was implicitly assumed that the charge condition at the oxide/AlGaN interface is fixed (see Fig.2.10). When analyzing real devices, charging and discharging dynamics of additional interface trap states have to be considered, which change this charge condition. The resulting instabilities can make circuit design challenging or even impossible. Particularly the resulting threshold voltage shift (see Eq. (2.14)) and its transient behavior are important for the operation of normally-off MISHFET.

In the following, the common gate dielectric deposition method atomic layer deposition, is introduced. Next, the different types of interface states, their energetic distribution within the bandgap and their origin are discussed. Consequently, the impact of the gate insulator in MISHFET is shown and two different techniques to manipulate the interface properties, thermal annealing (PDA) and oxygen plasma annealing are investigated. The aim is the reduction of the fixed positive interface charge and interface trap density to achieve a stable, ideally positive, V_{th} shift ΔV_{th} by the gate dielectric. The fundamental threshold voltage shift limitations of MISHFET devices will be discussed and the chapter is concluded by presenting a memory device, which employs the effects shown throughout this chapter.

4.1. Plasma-Enhanced Atomic Layer Deposition

Quality and thickness control of the gate dielectric are vital for achieving the desired device properties. The method of choice for the deposition of thin dielectrics is plasma-enhanced atomic layer deposition (PEALD). The basic working principle is an alternating, self-terminating deposition of an atomic layer of metal and nonmetal. Due to this process scheme, a monolayer-thickness control [75] and very good conformity can be achieved [76].

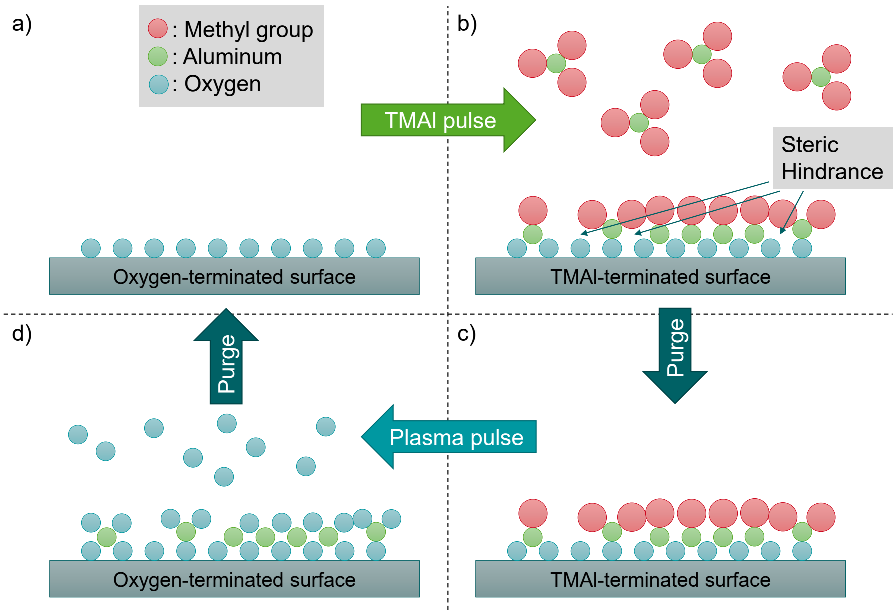

a)
●: Methyl group
●: Aluminum
●: Oxygen
TMAl pulse
b)
Steric Hindrance
Oxygen-terminated surface
TMAl-terminated surface
d)
Purge
c)
Purge
Plasma pulse
Oxygen-terminated surface
TMAl-terminated surface

Figure 4.1.: Schematic overview of a full process cycle of PEALD aluminum oxide. a) Oxygen-terminated surface b) After a TMAl pulse, the TMAl reacts with the oxygen-terminated surface c) TMAl-terminated surface and purge of the remaining molecules d) Plasma-ignition of the oxygen purge gas leads to highly reactive oxygen radicals which react with the TMAl-terminated surface.

The full deposition cycle for PEALD of aluminum oxide (AlO_x) is shown in Fig. 4.1. After cleaning the sample, an oxygen-terminated surface is assumed [Fig. 4.1(a)]. A tri-methyl-aluminum (TMAl) pulse is introduced into the chamber which reacts with the oxygen-terminated surface and splits-off the methyl groups [Fig. 4.1(b)]. After the whole surface is saturated with TMAl, the process automatically terminates and the remaining TMAl is purged from the chamber [Fig. 4.1(c)]. Next, the oxygen purge gas is plasma-ignited in a remote chamber. This creates highly reactive oxygen radicals, which react with the aluminum-terminated surface and form a (new) layer of AlO_x. Ideally, each full cycle deposits a monolayer of AlO_x, but due to incomplete reactions and steric hindrance, the deposition is less than a monolayer [75]. The deposited AlO_x thin films are amorphous, but thin films of other materials can also be crystalline [77].

In this work, the following pulse scheme was used: 30 ms TMAl, 1970 ms purge, 3000 ms plasma, 1000 ms purge. The chamber pressure was 20 Pa and the deposition temperature was 250 °C. The resulting deposition rate was 0.105 nm per cycle and the relative dielectric constant of the resulting thin film was $\varepsilon_r = 8$, which is comparable to literature values [78].

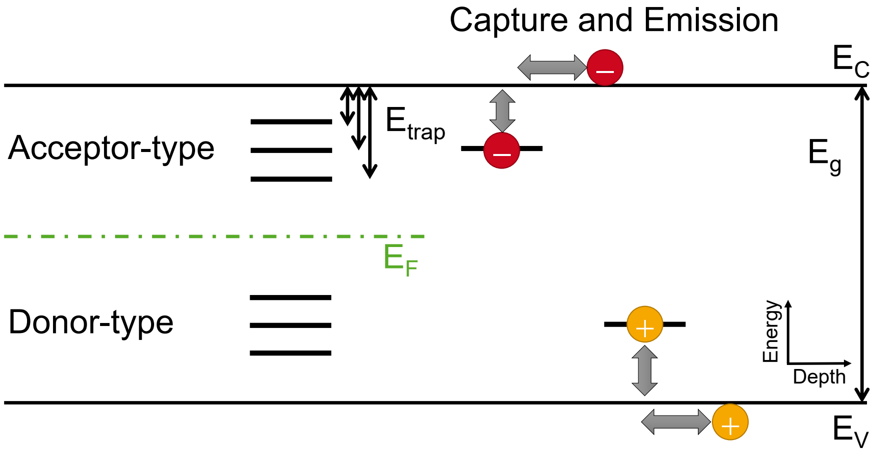


Figure 4.2.: Band diagram of the different types of traps within the bandgap. Furthermore, the capture and emission processes are depicted.

4.2. Interface Trap States

The interface charge density σ_{int} was considered as fixed charge in the previous chapter. But due to impurity incorporation during deposition, dangling bonds and defects, dielectrics and dielectric/semiconductor interfaces commonly show bulk/interface states, respectively. These so-called trap states capture and emit electrons and have a high impact on the device properties, as they change the charge condition within the structure, effectively changing σ_{int}. They are classified into two types, namely acceptor- and donor-type traps in analogy to dopants.

Fig. 4.2 shows a schematic of these two trap types in the semiconductor bandgap. In thermal equilibrium, the trap states are occupied in their relation to the Fermi level. In the presence of free charge carriers, acceptor-type traps are able to capture electrons and become negatively charged, while donor-type traps capture holes becomes positively charged. As no free states in a more energetically-favorable position exist, the charge carriers are now trapped.

The transient behavior of trap states is related to their energetic depth within the bandgap E_{trap}. It can be either related to the distance between the trap state and the conduction band edge or valence band edge for acceptor-type traps and donor-type traps, respectively. While the capture process is commonly considered to be very fast, the mean time until an emission process occurs τ (emission time constant) can be described by Shockley-Read-Hall statistics [79]:

$$\tau = \frac{1}{v_{\mathrm{th}}\sigma_{\mathrm{th}}N_{\mathrm{c}}} \exp\left(\frac{E_{\mathrm{trap}}}{k_{\mathrm{B}}T}\right) \tag{4.1}$$

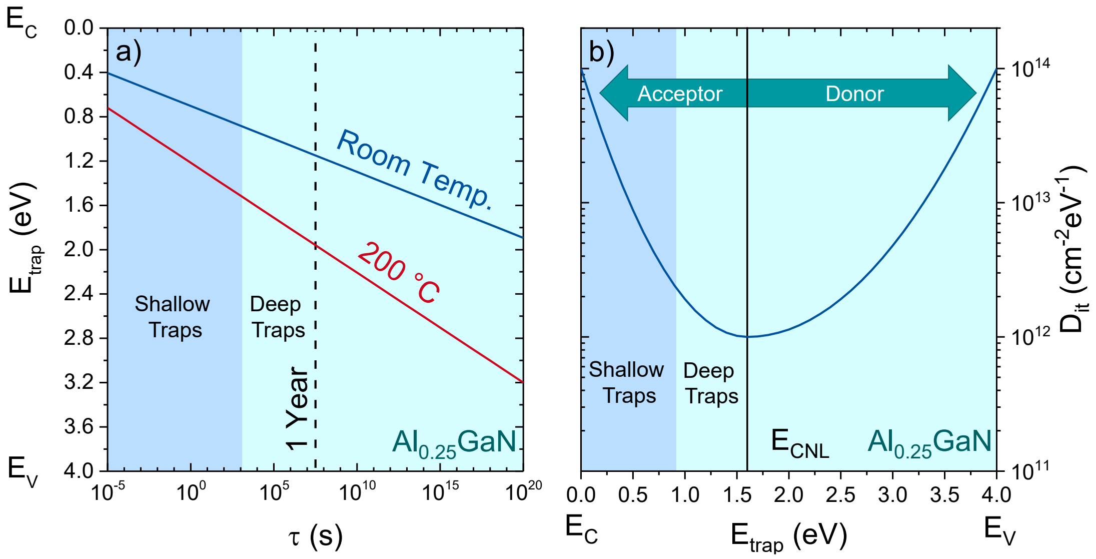


Figure 4.3.: Trap emission time constants and distribution of trap density vs. their distance from the AlGaN conduction band edge E_{trap}. Traps are classified in deep and shallow traps whether they emit captured electrons during the measurement time frame. a) E_{trap} vs. trap emission time constant. b) Trap density D_{it} vs. E_{trap}. Traps from the charge-neutrality level E_{CNL} towards conduction band edge are acceptor-type, while they are donor-type towards the valence band edge. Images after [79].

where v_{th} is the thermal velocity of the electrons, σ_{th} the trap cross section, N_c the free state density in the conduction/valence band, k_B the Boltzmann constant and T the absolute temperature in Kelvin.

Fig. 4.3(a) shows E_{trap} related to the conduction band edge of AlGaN with 25% Al vs. τ. Traps that are located deeper in the bandgap have a significantly longer τ than traps near the band edge [see Eq. (4.1)]. At room temperature, traps with $E_{trap} = 1.15\,\text{eV}$ already have τ of approx. one year. Increasing the temperature reduces τ strongly, which is the foundation of various trap characterization techniques [80].

Based on their emission time constant τ, traps are additionally classified into shallow and deep traps. Shallow traps have τ in the range of the measurement duration used to characterize the traps, therefore the impact of a change of the charge state can be observed. Deep traps have τ longer than the measurement time and thus act as fixed charge. The focus in this work is on traps that are located at the interface between insulator and semiconductor, and capture/emit electrons.

Fig. 4.3(b) shows the energetic distribution of the interface trap density in the bandgap D_{it} vs. E_{trap}. The U-shape distribution is based on the unified disorder-induced gap state model by Hasegawa and Ohno [81] and was experimentally confirmed for oxide/III-nitride interfaces by Matys et al. [82]. According to this model, the interface states

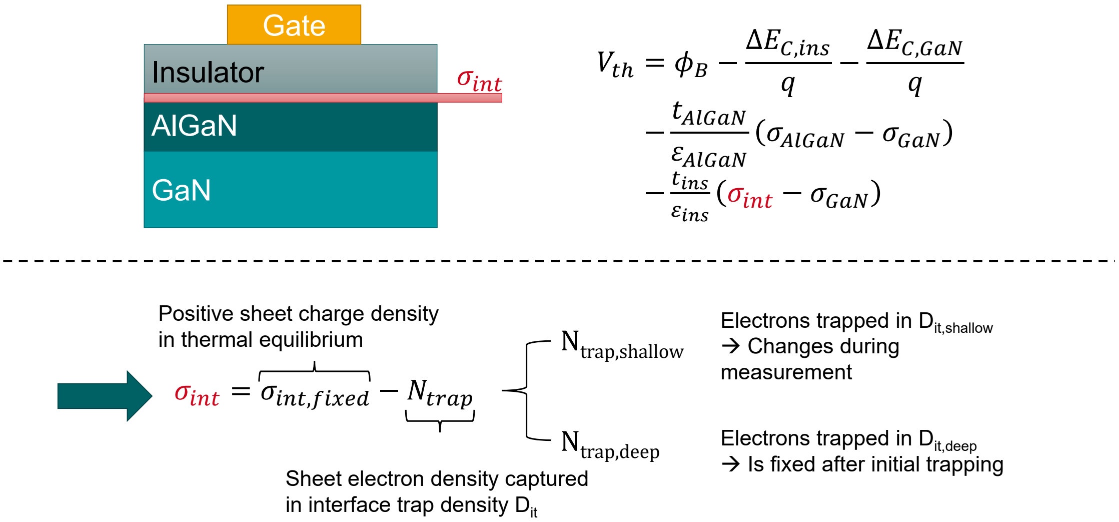

Gate
Insulator
AlGaN
GaN
σ_{int}
$V_{th} = \phi_B - \frac{\Delta E_{C,ins}}{q} - \frac{\Delta E_{C,GaN}}{q} - \frac{t_{AlGaN}}{\varepsilon_{AlGaN}}(\sigma_{AlGaN} - \sigma_{GaN}) - \frac{t_{ins}}{\varepsilon_{ins}}(\sigma_{int} - \sigma_{GaN})$
Positive sheet charge density in thermal equilibrium
$\sigma_{int} = \sigma_{int,fixed} - N_{trap}$
Sheet electron density captured in interface trap density D_{it}
$N_{trap,shallow}$
$N_{trap,deep}$
Electrons trapped in $D_{it,shallow}$ → Changes during measurement
Electrons trapped in $D_{it,deep}$ → Is fixed after initial trapping

Figure 4.4.: Overview of the different parts of the interface charge density σ_{int}, which is influencing V_{th}. The equation in the top right corner is Eq. (2.14).

originate from dangling bonds caused by crystal disorder of the semiconductor surface. The U-shape is caused by the nature of the bonding states to minimize their energy during formation and can be described by an exponential decay of D_{it} towards the charge-neutrality level E_{CNL} [82]. The charge-neutrality level E_{CNL} is defined as the Fermi level position, for which the interface is charge neutral, and is only used in this work for the explanation of this model. The model states further, that trap states from E_{CNL} towards the conduction band are acceptor-type and donor-type towards the valence band. Higher levels of disorder at the insulator/AlGaN interface lead to a higher D_{it}, which decreases the device stability. A more detailed explanation of the capture and emission processes of D_{it} during device operation and the influence on V_{th} is given in the next section. D_{it} will be used for the interface trap density and the interface traps synonymously for the sake of simplicity.

Due to the interface trap states D_{it}, the model for the sheet charge at the insulator/AlGaN interface changes. Fig. 4.4 gives an overview over the different terms used in this chapter. The interface charge density σ_{int} now consists of two terms. The fixed positive interface charge density at thermal equilibrium $\sigma_{int,fixed}$ and the sheet electron density N_{trap}, which is captured inside the interface traps D_{it}. N_{trap} reduces σ_{int}, which shifts V_{th} to more positive voltages. Furthermore, the electrons trapped in the shallow traps $D_{it,shallow}$ are called $N_{trap,shallow}$, while the ones trapped in the deep traps $D_{it,deep}$ are called $N_{trap,deep}$. For pristine devices, it is always assumed that N_{trap} is initially zero and $\sigma_{int} = \sigma_{int,fixed}$.

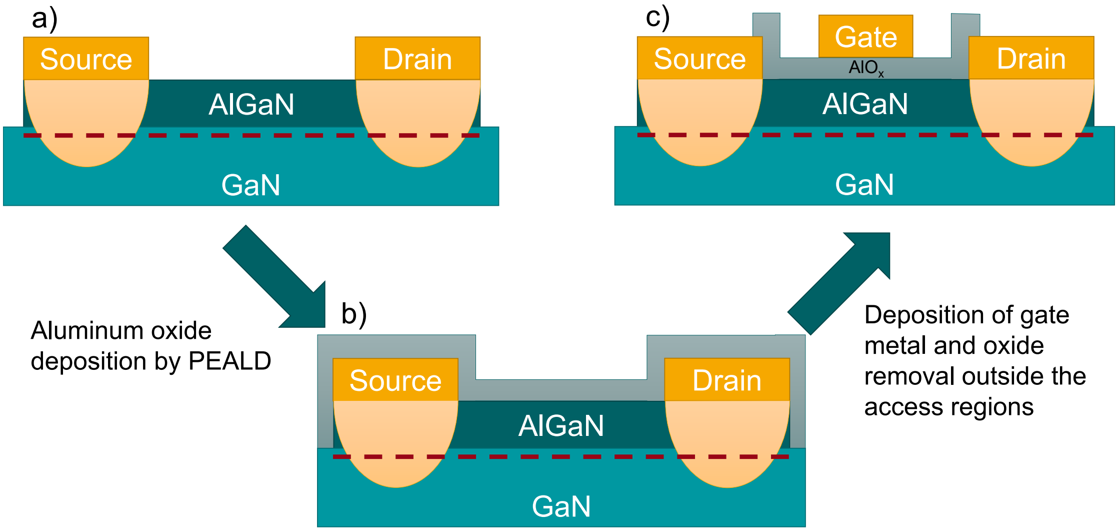

a)
Source
Drain
AlGaN
GaN
Aluminum oxide deposition by PEALD
b)
Source
Drain
AlGaN
GaN
Deposition of gate metal and oxide removal outside the access regions
c)
Gate
AlO$_x$
Source
Drain
AlGaN
GaN

Figure 4.5.: Schematic of MISHFET processing. a) Sample after the formation of the mesa and ohmic contacts. b) Aluminum oxide deposition by PEALD. c) Deposition of gate metal and removal of the oxide outside of the access regions.

4.3. Metal-Insulator-Semiconductor HFET

To investigate the AlO_x/AlGaN interface properties $\sigma_{int,fixed}$ and D_{it} as well as their impact on V_{th}, MISHFET were processed. Fig. 4.5 shows a schematic of the device process which is used in this work. After the formation of mesa and ohmic contacts, 10 nm aluminum oxide is deposited by PEALD (see section 4.1). Subsequently, a post-deposition anneal (PDA) can be performed to improve the interface properties. The device is finished by gate metal deposition and oxide removal outside of the access regions.

In Fig. 4.6, the measurement of an HFET is compared with the one of a MISHFET. The devices of this section are taken as examples to show the differences between HFET and MISHFET and to explain the characteristic hysteresis effects. More detailed wafer information can be found in the appendix A.2 (Wafer I).

The input characteristic in Fig. 4.6(a) shows a reduction of the gate leakage current in forward and reverse direction of about four orders of magnitude. This enables forward bias voltages up to 6 V, after which dielectric breakdown occurs. In general, the dielectric breakdown voltage depends on the insulator thickness for a constant critical electric field of the material. The maximum forward bias in this case is chosen to 4 V.

Due to a better gate insulation, the OFF-current is reduced by two orders of magnitude, improving the ON/OFF-ratio from 10^6 to 10^8 [see Fig. 4.6(b)]. Furthermore, a V_{th} shift of 2.5 V in negative direction can be observed. As described in section 2.6.3, the

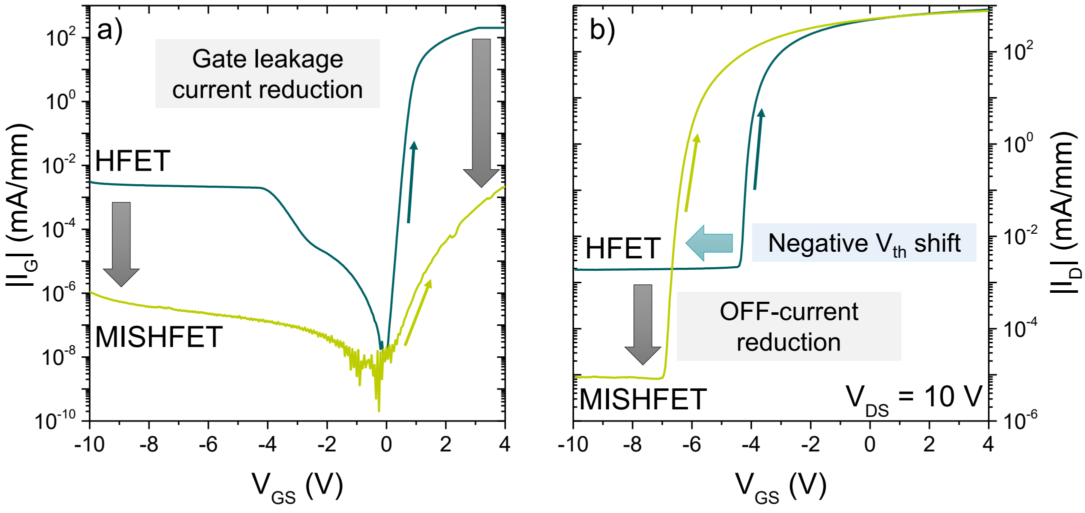


Figure 4.6.: Comparison of electrical characteristics between an HFET and a MISHFET. a) Input characteristic shows a gate leakage current reduction of four orders of magnitude. b) Transfer characteristic, in which a negative V_{th} shift of 2.5 V and an OFF-current reduction of two orders of magnitude is visible. Measurement direction is indicated by the small arrows.

deposited gate insulator will lead to a negative V_{th} shift as long as the positive interface charge density σ_{int} is larger than the GaN polarization. From the position of V_{th} and by using Eq. (3.3), $\sigma_{int,fixed}$ can be estimated to $9 \cdot 10^{12}$ cm^{-2}.

To characterize D_{it}, hysteresis measurements were performed. Fig. 4.7(a) shows the transfer characteristic of a MISHFET swept from $V_{GS} = -10$ V to 4 V and back to –10 V. The V_{th} hysteresis ΔV_{th} between the to- and back-sweep is visible, which is caused by trapped electrons N_{trap}. The different effects during the measurement can be explained better by the C-V measurement of the same sample, which is shown in Fig. 4.7(b) [79].

First, the to-sweep from $V_{GS} = -10$ V to 4 V is discussed. At $V_{GS} = -10$ V, the 2DEG is depleted, thus no capacitance is measured. After step 1, the 2DEG is accumulated and the capacitance rises to 300 nF/cm^2. At this point, no charge transfer from the 2DEG to the oxide/AlGaN interface has taken place, therefore $N_{trap} = 0$/cm^{-2} [see Fig. 4.7(c)]. During step 2, the conduction band is pulled down low enough to allow electrons to surpass the AlGaN barrier and accumulate at the oxide/AlGaN interface [see Fig. 4.7(d)]. Here, the electrons are transferred from the conduction band and to the interface traps, which changes the electrostatics and thus, the electric fields. The increasing amount of trapped electrons change the electric field in such a way, that it works against the increasing forward bias leading to slowly rising capacitance in step 2 [79] compared to step 1. The capacitance would eventually saturate at $C_{ox} = 600$ nF/cm^2 for a sufficiently high forward bias voltage, but the voltage is limited by the dielectric breakdown of the oxide. The slope of the C-V curve during step 2 depends on the magnitude of D_{it}. Very large D_{it} can lead to a complete suppression of step 2. In this example, the capacitance rises up to 450 nF/cm^2 at 4 V forward bias.

During the start of the back-sweep, $D_{it,shallow}$ start to emit their electrons $N_{trap,shallow}$ according to Eq. (4.1), while the electrons in deep traps $N_{trap,deep}$ can be considered as fixed. The change in the electric field caused by $N_{trap,deep}$ [see Fig. 4.7(e)] now works in the same direction as the declining forward bias, which leads to a steeper slope of the capacitance during step 2 of the back-sweep. The capacitance decreases until no more free electrons are located at the interface and the oxide/AlGaN barrier capacitance of 300 nF/cm^2 is reached. As the electrons in deep traps are not emitted during the back-sweep, they reduce the total net interface charge density σ_{int}. This ultimately shifts V_{th}

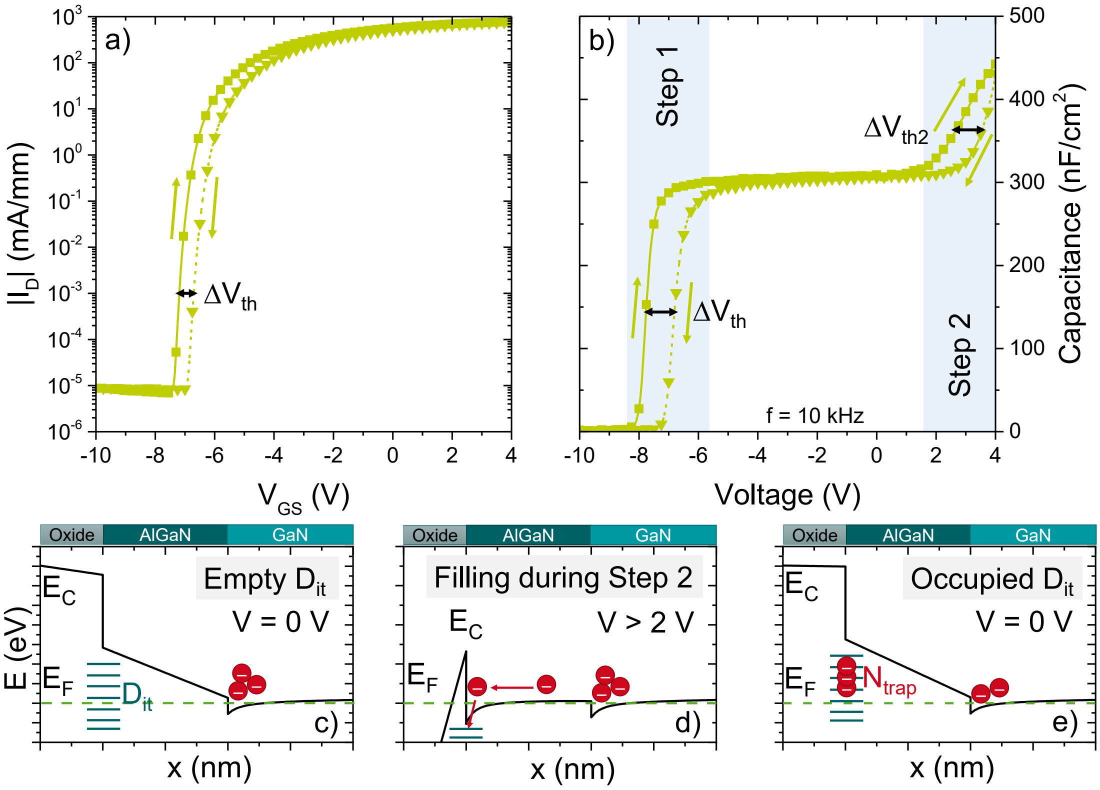


Figure 4.7.: Transfer characteristic and capacitance-voltage measurement of a MISHFET swept from -10 V to 4 V and back. a) Transfer curve with small ΔV_{th} between to and back sweep. b) The C-V measurement shows two capacitance steps, step 1 and step 2, associated with charge accumulation in the 2DEG and the oxide/AlGaN interface, respectively. During the to-sweep D_{it} is empty (c) until step 2, in which electrons move from the 2DEG to the oxide/interface (d). The now trapped electrons (e) shift V_{th} of the back-sweep. Figure after [79].

to more positive values, which can be seen from the difference of the position of step 1 ΔV_{th} between the to and back-sweep [see Fig. 4.7(b)].

In general, the characterization of the oxide/AlGaN interface is challenging due to the separation of interface traps and the 2DEG by the AlGaN barrier. Therefore, this combination of trap-filling at forward bias and characterization of the impact on the 2DEG is used [79]. From ΔV_{th}, the trapped electron density N_{trap} can be estimated using Eq. (3.3) (see Fig 4.4):

$$N_{trap} = \sigma_{int,1} - \sigma_{int,2} = \sigma_{int,fixed} - (\sigma_{int,fixed} - N_{trap}) = \frac{C_{ins} \cdot \Delta V_{th}}{q} \tag{4.2}$$

For the C-V curve of Fig. 4.7(b), a ΔV_{th} of 0.97 V leads to N_{trap} of $8.9 \cdot 10^{12}\,\mathrm{cm}^{-2}$. This represents a medium high value for D_{it}. D_{it} as low as $1.6 \cdot 10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ is reported in literature for dielectric/AlGaN interfaces [83], while very high D_{it} can be caused by insufficient surface cleaning or the lack of a thermal treatment (shown in the next section).

N_{trap} can also be determined from the hysteresis ΔV_{th2} of step 2 by using the same equation Eq. (4.2). The advantage of using ΔV_{th2} is a smaller delay between trap-filling and characterization. Thus, more of the fast shallow D_{it} can be measured. However during the measurement, high levels of D_{it} [79] or a large AlGaN barrier resistance [70] suppress step 2, which can make the evaluation of N_{trap} from ΔV_{th2} challenging.

4.4. Post-Depositon Anneal

A technique to improve the bulk- and interface properties of deposited dielectrics is the post-deposition anneal (PDA) [84]. While the bulk properties are important for the electrical insulation of the dielectric, the interface charge influences the threshold voltage of devices as described in the previous section. Through the supply of thermal energy, several processes in the dielectric can be activated such as healing of defects and reordering of the dielectric/semiconductor interface. The upper temperature limit is given by the onset of crystallization of the amorphous aluminum oxide layer, which starts at 800 °C [85]. The resulting grain boundaries in the polycrystalline thin films commonly lead to an increased leakage current and premature dielectric breakdown.

To investigate impact of the PDA temperature on device properties, large-area diodes (LAD) were fabricated with a PDA ranging from 450 °C to 800 °C in nitrogen atmosphere. Details of the wafer used in this experiments can be found in the appendix

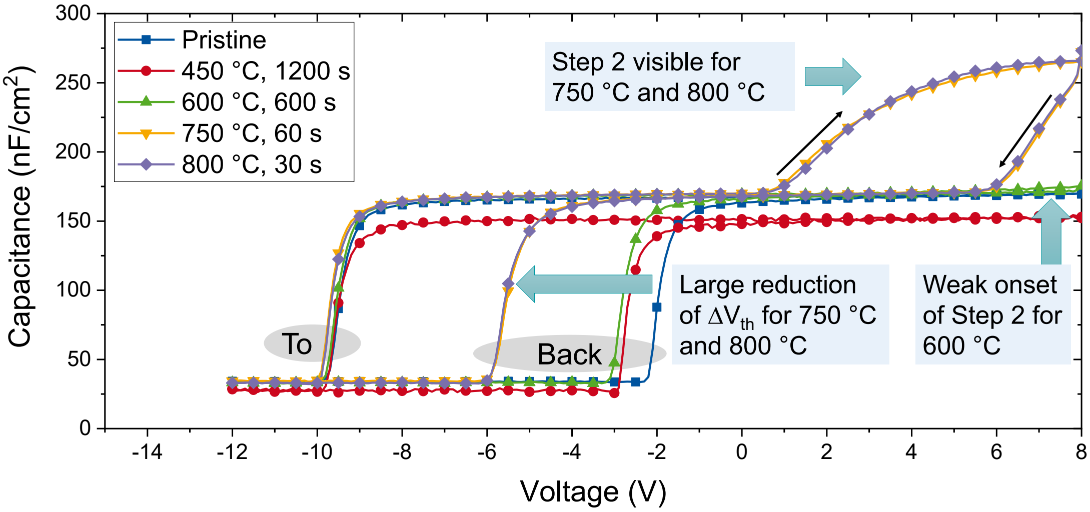


Figure 4.8.: Capacitance-voltage measurement of LAD with different PDA. The threshold voltage hysteresis ΔV_{th} is reduced for higher PDA temperatures. Step 2 is weakly pronounced for 600 °C. For 750 °C and 800 °C, step 2 is fully developed and a saturation at the oxide capacitance is visible. The measurement frequency was f = 10 kHz.

A.2 (Wafer II). The PDA duration started at 1200 s for 450 °C and was lowered for higher temperatures to reduce the total thermal budget. Fig. 4.8 shows the results of C-V measurements. For these samples, 20 nm AlO_x were deposited after the formation of ohmic contacts. An additional pristine sample without annealing is included for comparison. The detailed description of the experiment can be found in [86].

The samples were measured from –12 V to 8 V and back. The hysteresis for the pristine sample is large with $\Delta V_{th} = 7.49$ V. A PDA at 450 °C and 600 °C slightly decreases ΔV_{th} to 6.82 V and 6.73 V, respectively. After high-temperature PDA at 750 °C and 800 °C, ΔV_{th} is further reduced to 4.16 V and 4.1 V, respectively. N_{trap} at the interface is calculated by Eq. (4.2) and the results are summarized in Tab. 4.1. $N_{trap} = 1.65 \cdot 10^{13}$ cm^{-2} of the pristine sample was reduced by 45% to $0.91 \cdot 10^{13}$ cm^{-2} through PDA at 800 °C.

Table 4.1.: ΔV_{th} and N_{trap} of C-V measurements performed on LAD with different PDA temperatures and durations.

Annealing Temp. (°C)	Pristine	450	600	750	800
Time (s)	-	1200	600	60	30
ΔV_{th} (V)	7.49	6.82	6.73	4.16	4.1
N_{trap} (10^{13} cm^{-2})	1.65	1.51	1.49	0.92	0.91

Furthermore, the C-V curves of this experiment show the influence of D_{it} on step 2 at forward bias of the LAD. For the pristine sample and PDA at 450 °C, only step 1 is visible in the C-V curve. The high D_{it} at the interface, which is indicated by the high value of N_{trap}, completely suppresses step 2 (see Fig. 4.7). At 600 °C, D_{it} is reduced strongly enough to allow for a weak onset of step 2. Finally for 750 °C and 800 °C, step 2 is fully developed and a saturation at the oxide capacitance is visible.

The optimized PDA was then used in a MISHFET fabrication process. Details for the employed material can be found in the appendix A.2 (Wafer III). For the sake of a lower thermal budget and to avoid dielectric crystallization, 750 °C is chosen as optimum for this experiment. The aluminum oxide for the MISHFET has thickness of 10 nm and was deposited by PEALD. The input characteristic in Fig. 4.9(a) shows a further improved reverse leakage current through the PDA, while the forward leakage current is increased. In Fig. 4.10, the current-voltage characteristic of a LAD with identical processing is shown for comparison. Here, only a very low leakage current in forward direction is visible. Therefore, the forward leakage current of the gate diode [Fig. 4.9(a)] is most likely caused by additional leakage current paths along mesa sidewalls [87] or between contact pads (see appendix A.4). A defect-rich AlO_x could be formed on the mesa sidewall with only weak insulating properties, which could further degrade at higher temperatures [88].

Fig. 4.9(b) depicts the corresponding changes of the transfer characteristics through the PDA. The OFF-current of the device is suppressed by additional two orders of magnitude (in comparison to the HFET) leading to an ON/OFF-ratio of 10^{10}. ΔV_{th} is reduced from 0.52 V to 0.27 V. This corresponds to N_{trap} of $2.30 \cdot 10^{12}\,cm^{-2}$ and $1.19 \cdot 10^{12}\,cm^{-2}$, respectively (see Fig. 4.4). In contrast to the C-V measurements shown in Fig. 4.8, a positive shift of V_{th} of 3.21 V can be observed. Since V_{th} depends on σ_{int}, the PDA has effectively decreased $\sigma_{int,fixed}$ to $2.25 \cdot 10^{12}\,cm^{-2}$ in addition to the reduction of D_{it}, which is evident from the lower ΔV_{th}.

In this section, it was shown that a high-temperature PDA can improve the bulk- and interface properties of deposited AlO_x. According to the unified disorder-induced gap state model, this improvement is achieved by a higher degree of order at the interface. Due to the high temperature during PDA, the bonds can arrange in an energetically more favorable state. The reduction of σ_{int} to $2.25 \cdot 10^{13}\,cm^{-2}$ has led to a V_{th} shift in positive direction in relation to the not annealed MISHFET, which is already close to the GaN polarization σ_{GaN} of $2.12 \cdot 10^{13}\,cm^{-2}$. As already described in section 2.6.3, as soon as $\sigma_{int} < \sigma_{GaN}$, the sign of the V_{th} oxide thickness dependence flips. This consequently enables a positive shift in V_{th} with increasing oxide thickness, which ultimately could

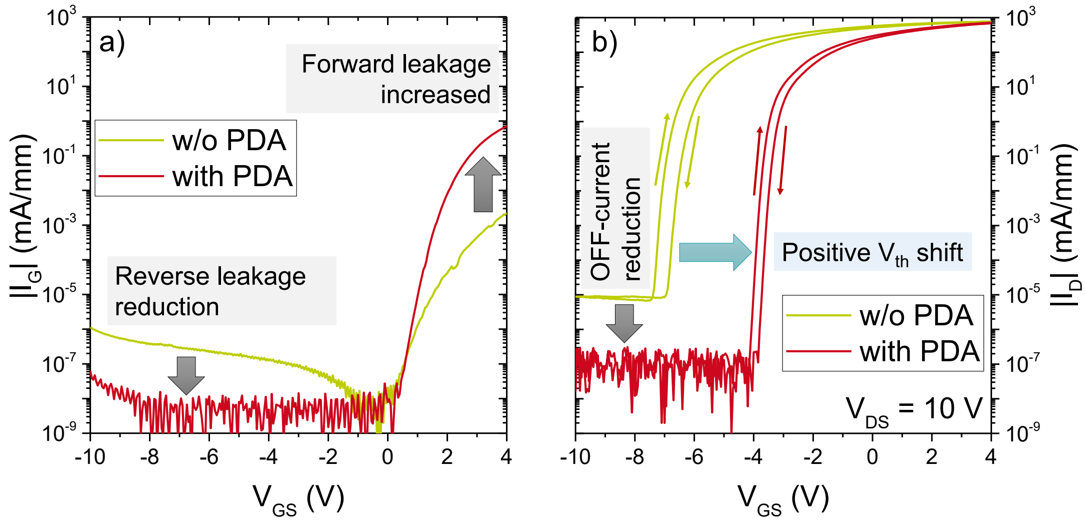


Figure 4.9.: Comparison of a MISHFET with and without PDA of the AlO_x. a) Input characteristic of the two devices. The reverse leakage is reduced through the PDA, while an increased current in forward direction of the gate diode can be noticed. b) Transfer characteristic of the devices. The OFF-current is reduced by approximately two orders of magnitude. Furthermore, the threshold voltage is shifted in positive direction from –6.66 V to –3.45 V. The hysteresis ΔV_{th} is reduced from 0.52 V to 0.27 V for the PDA sample. This corresponds to N_{trap} of $2.30 \cdot 10^{12}\,\text{cm}^{-2}$ and $1.19 \cdot 10^{12}\,\text{cm}^{-2}$, respectively.

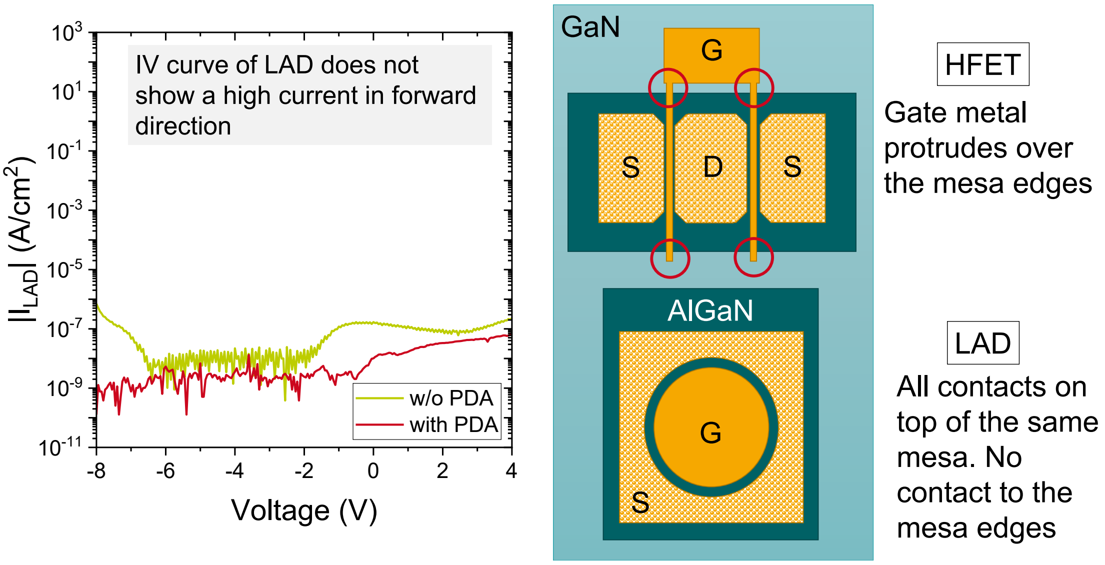


Figure 4.10.: I-V characteristic of an LAD with oxide. The LAD shows no signs of a high forward current density caused by the PDA. Additionally, schematics of an HFET and an LAD are depicted on the right side.

transform a normally-on to a normally-off device. To access this additional degree of freedom in device design, a different approach to reduce σ_{int} below σ_{GaN} is discussed in the following section.

4.5. Pre-deposition Plasma Oxidation

The surface preparation before dielectric deposition plays a major role for the resulting interface between the two materials. First, an extensive chemical cleaning with e.g. hydrofluoric acid (BOE), hydrochloric acid (HCl) or piranha solution is commonly employed to achieve a clean surface prior to deposition [89, 90]. The sample is then transferred to the PEALD reactor. During the PEALD process, the sample is not immediately covered with a closed $\mathrm{AlO_x}$ thin film leading to a partial oxidation of the sample surface. The resulting $\mathrm{(Al)GaO_x}$ has a strong influence on the interface properties of the finished device [84]. Thus, an active control of the unavoidable surface oxidation is crucial for the device performance.

A way to achieve an intentional surface oxide is oxygen plasma annealing. In a theoretical study from Miao et al., it was shown by density functional theory (DFT) that there is the possibility of a stable oxide consisting of two monolayers [91]. This theory is supported by an experimental work from Qin et al., in which the formation of a crystalline oxide passivation on an AlGaN surface by plasma oxidation has been proven [92]. The two-monolayer oxide is expected to possess a low $\sigma_{\mathrm{int,fixed}}$ as well as a low D_{it}. The low $\sigma_{\mathrm{int,fixed}}$ is particularly important for gate-recessed normally-off HFET [17] since a gate dielectric with a high σ_{int} could change the device back to normally-on (see Fig 2.13).

In the following, the investigation of oxygen plasma annealing on dry-etched (i.e. "gate-recessed") AlGaN surfaces is presented. Parts of the results are already published in [57]. The AlGaN barrier has a thickness of 23 nm with an Al content of 26% and a 1 nm AlN spike. More detailed wafer information can be found in the appendix A.2 (Wafer III). After ohmic contact and mesa formation, the samples were etched in an inductive coupled plasma reactive ion etching (ICP-RIE) tool by a cyclic $\mathrm{BCl_3/O_2}$ etch [17] to a final barrier thickness of approximately 13 nm. Subsequently, the samples are oxygen plasma annealed either directly inside the ICP-RIE or inside the PEALD tool prior to the deposition process. Four different samples are investigated: a reference sample, which is recessed but not plasma annealed (sample REC), a sample annealed in the ICP-RIE at 40 °C directly after the recess (sample ICP40) and two samples, which

REC	ICP40	ALD250	ALD350
Reference sample with recess only	Direct plasma in ICP-RIE at 40 °C	Remote plasma in PEALD at 250 °C	Remote plasma in PEALD at 350 °C

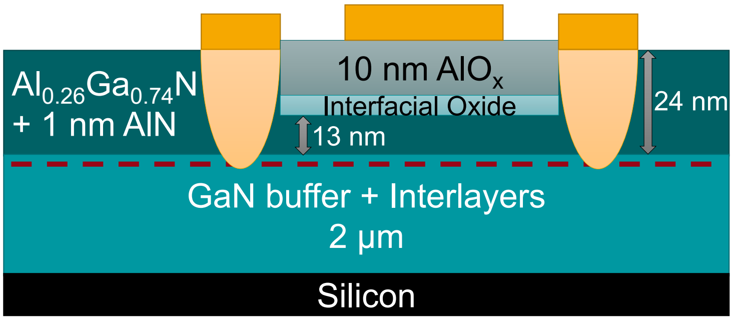


Figure 4.11.: Sample overview and a schematic of the LAD used for the plasma annealing experiments.

are plasma annealed in the PEALD system either at 250 °C (sample ALD250) or 350 °C (sample ALD350). The plasma type inside the ICP-RIE is a direct plasma, whereas the plasma inside the PEALD is a remote plasma. After plasma annealing, 10 nm AlO_x are deposited by PEALD at 250 °C, and the samples are finished by top metal contact deposition. No PDA was performed to solely show the influence of the plasma annealing. The process details can be found in [57]. A schematic overview and a table of the different samples are depicted in Fig. 4.11. For characterization, C-V measurements were performed, which are extended by stress-time dependent and transient C-V measurements where applicable.

Fig. 4.12 shows C-V measurement results of sample REC. The voltage is swept from –12 V to 4 V after different stress times at –12 V. A pristine device is chosen for each measurement to avoid prior electron transport from the 2DEG to the oxide/AlGaN interface. Therefore, the trap occupancy is only related to thermally generated carriers. Additionally to the C-V measurement results, a TCAD-simulated C-V curve is shown in which the interface charge density σ_{int} is set to the GaN polarization σ_{GaN} $\sigma_{\text{int}} = \sigma_{\text{GaN}} = 2.12 \cdot 10^{13}\,\text{cm}^{-2}$. Thus, V_{th} is independent of the oxide (see Fig. 2.13). The experimental results reveal a larger negative V_{th} of –7.4 V in relation to the simulated curve. This indicates a highly positive σ_{int} of $4.86 \cdot 10^{13}\,\text{cm}^{-2}$.

Furthermore, a stress-time-dependent shift of V_{th} to more negative voltages can be observed when the device is kept at –12 V prior to the measurement. Since the threshold

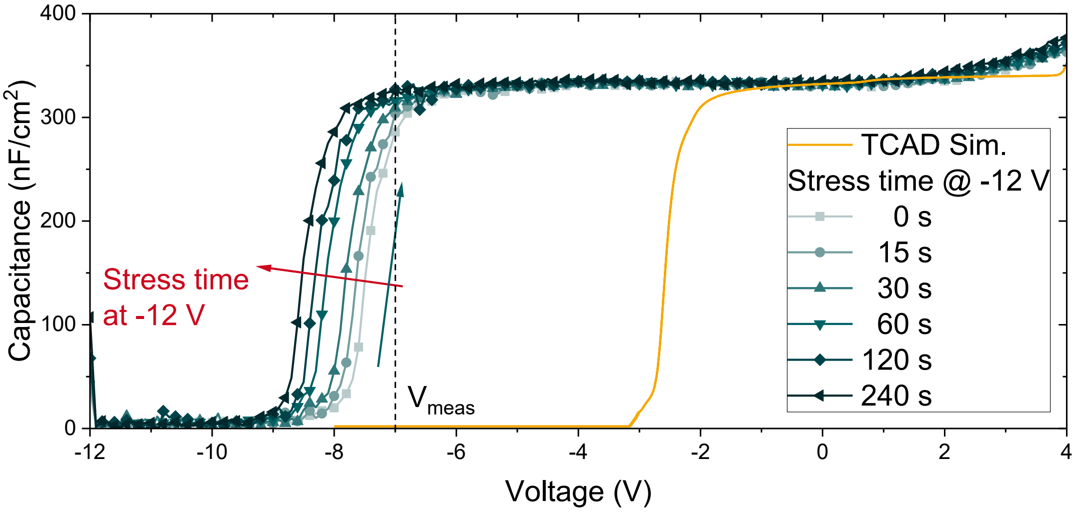


Figure 4.12.: C-V curves of sample REC (recess-only) with different stress times at –12 V prior to the measurement. For comparison, a simulated C-V curve with $\sigma_{int} = \sigma_{GaN}$ is shown. The measurement frequency was f = 1 kHz.

voltage depends on σ_{int}, this indicates electron emission from D_{it} at the oxide/AlGaN interface. This behavior is not expected for a pristine device, since the device was not operated in the spill-over regime (see Fig. 4.7) and thus, D_{it} should not be occupied with electrons.

For a more detailed insight into the dynamic processes, transient C-V measurements were performed. First, the sample is stressed at a positive forward bias V_{stress} to occupy the trap states with electrons (see Fig. 4.7). Afterwards, the capacitance is monitored at a voltage V_{meas} for a set period of time. V_{meas} is chosen just below the threshold voltage, when the device is switched from $V_{stress} = 1$ V to V_{meas}. Therefore at t = 0 s, the capacitance is depleted for all stress voltages. When the trap states start to emit electrons over time, V_{th} is shifted towards more negative voltages and at some time the capacitance at V_{meas} rises. Through this technique, the time it takes for V_{th} to reach V_{meas} can be evaluated, which is an indicator for the trap depth (see Eq. (4.1)).

The sample was subjected to V_{stress} for 10 s and then continuously measured at –7 V for 590 s. All measurement sweeps were performed on the same LAD and are shown in Fig. 4.13(a).

For higher forward stress voltages, the capacitance needs a longer recovery time period to return to its original value. However for all stress biases up to 8 V (dielectric breakdown of the oxide occurs at 9 V), the capacitance saturates in the measurement time frame and its value shows only a minor dependence on the stress bias. Thus, there

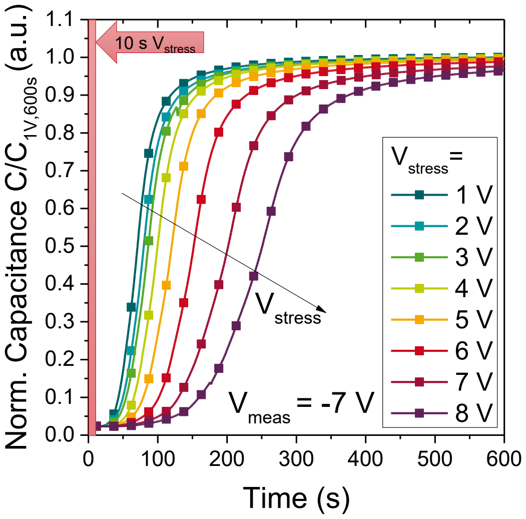


Figure 4.13.: Transient C-V measurement of sample REC. The sample is stressed at $V_{stress} = 1$ V to 8 V for 10 s and subsequently measured for 590 s at $V_{meas} = -7$ V. C-V curves are normalized to the capacitance value for $V_{stress} = 1$ V stress after 600 s. The measurement frequency was f = 1 MHz.

is no "permanent" V_{th} shift, which would be related to $N_{trap,deep}$. From fitting a TCAD-simulation of the transient C-V curve for $V_{stress} = 1$ V with only a single trap energy level at the insulator/AlGaN interface, a corresponding energy level of approximately 0.9 eV below the conduction band edge can be estimated (assuming a capture cross section of $\sigma = 10^{-16}$ cm^2 [93]).

Commonly, a V_{stress} lower than the voltage required for spill-over would not result in any V_{th} shift (see Fig. 4.7). Furthermore, $N_{trap,deep}$ is occupied first at low V_{stress}, so a near "permanent" shift is expected. Thus, the capacitance should not return to its original value for a long period of time (see Fig. 4.3). But here, only faster dynamics are observed in the timescale of minutes, which is only expected for higher V_{stress} and occupation of $N_{trap,shallow}$.

For the presented transient C-V measurements, the observed behavior cannot be explained by the expected U-shaped trap distribution (see section 4.2). For the considerations above, only the trap emission time constant is taken into account and the transport of the emitted electron is assumed to be instantaneous. But since the oxide/AlGaN interface is separated from the 2DEG, not only the emission time of N_{trap} is relevant but also the transport of the emitted electrons from the interface, over the AlGaN barrier and AlN spike, to the 2DEG. Therefore, the observed time constant needs to reflect a two-step process of emission and transport $\tau = \tau_{emit} + \tau_{trans}$. This process is depicted in

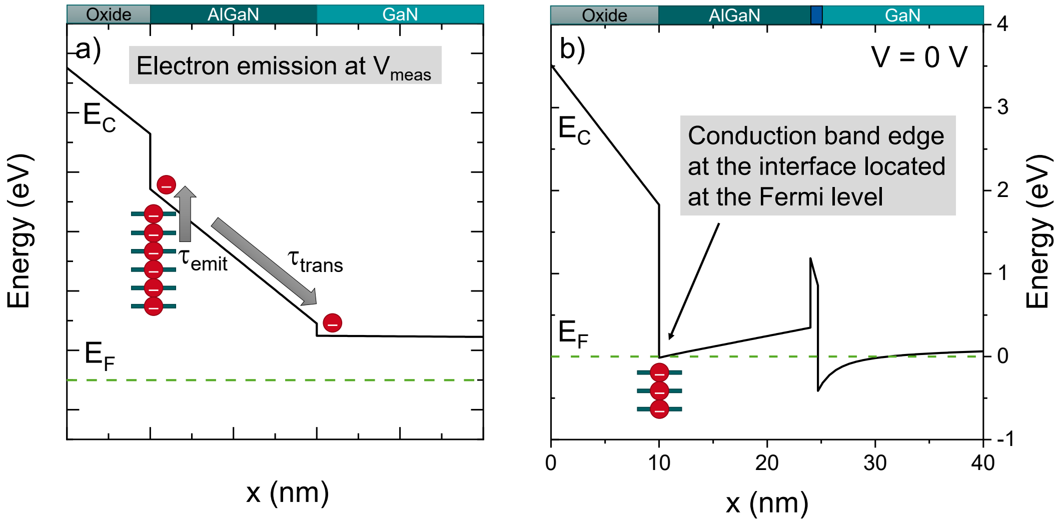


Figure 4.14.: Conduction band diagrams of an oxide/AlGaN/(AlN)/GaN heterostructure. a) Schematic band diagram at the reverse bias V_{meas}. The total electron time constant is a combination of the trap emission time constant τ_{emit} and the transport time constant τ_{trans}. b) Simulated band diagram of sample REC at thermal equilibrium. The conduction band edge reaches the Fermi level even at zero bias, therefore D_{it} is already fully occupied.

Fig. 4.14(a). Such a limitation due to defect assisted transport was proposed by Mehari et al. [94] with an activation energy of 0.9 eV, which is in good agreement with the simulation results.

In the transport-limited case, the observed time constant is dominated by the transport time constant τ_{trans}. So even for very fast traps ($\tau_{emit} \ll \tau_{trans}$), discharging is limited by τ_{trans} which leads to a projection of all fast traps to the 0.9 eV activation energy.

Furthermore, the simulated conduction band diagram of sample REC in Fig. 4.14(b) shows, that the high $\sigma_{int,fixed}$ leads to electron accumulation at the oxide/AlGaN interface at zero bias. Consequently, all electron traps are already occupied at thermal equilibrium and excess electrons are accumulated at the interface. If the sample is now measured at negative bias, the electron emission and transport away from the interface to the 2DEG shift V_{th} to more negative values over time. The longer recovery time observed in the measurements originates from the higher density of electrons for increased V_{stress} at the oxide/AlGaN interface. This assumption is supported by the high barrier resistance reflected in the weak onset of the second capacitance step, which is barely observable in Fig. 4.12 [70].

In the following, a comparison of all four samples is performed. Fig. 4.15 shows the C-V curves of pristine LAD on samples REC, ICP40, ALD250 and ALD350 with the different oxygen plasma treatments prior to oxide deposition as well as the TCAD-

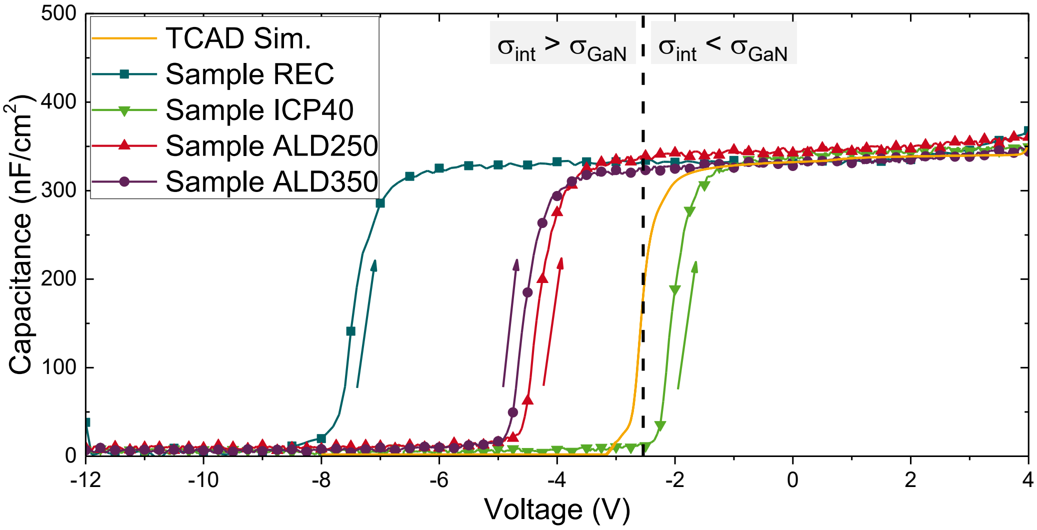


Figure 4.15.: Initial C-V curves of the recessed and plasma-treated samples as well as the TCAD-simulated curve. The measurement frequency was f = 1 kHz.

simulated CV curve from Fig. 4.12. All C-V curves of the pristine oxygen-plasma annealed samples (initial C-V curves) show a V_{th} shift to more positive values in relation to sample REC. The oxygen plasma annealing apparently reduces σ_{int}. Unlike sample REC in 4.12, the samples do not reveal a reverse stress time dependent C-V curve (not shown here), which is consistent with the positive V_{th} shift. While the samples annealed in the PEALD (ALD250+ALD350) still exhibit a negative V_{th} shift in respect to the TCAD-simulated curve ($\sigma_{int} > \sigma_{GaN}$), devices of sample ICP40 have a positive V_{th} shift ($\sigma_{int} < \sigma_{GaN}$). Therefore, it represents the most suitable oxygen plasma annealing process for gate-recessed normally-off HFET.

To further investigate the charging and discharging properties of the oxide/AlGaN interface and the related stability of V_{th}, repeated C-V measurements were performed. During the initial sweep at forward bias, electrons from the 2DEG are transfered to the oxide/AlGaN interface and occupy D_{it} as shown in Fig. 4.7. The electrons in the deep traps $D_{it,deep}$ will remain occupied in the observed time frame and therefore lead to a "permanent" positive V_{th} shift, whereas the shallow traps $D_{it,shallow}$ will change their occupancy. Thus, the samples were measured again with a full sweep from –12 V to 4 V and back until a stable state is reached.

The results for the oxygen plasma annealed samples are shown in Fig. 4.16. The first sweep is the initial to-sweep of the devices, while the second sweep consists of the second to-sweep and the back-sweep and represents the stable state for each subsequent measurement. All of the oxygen plasma annealed samples show a positive V_{th} shift and a

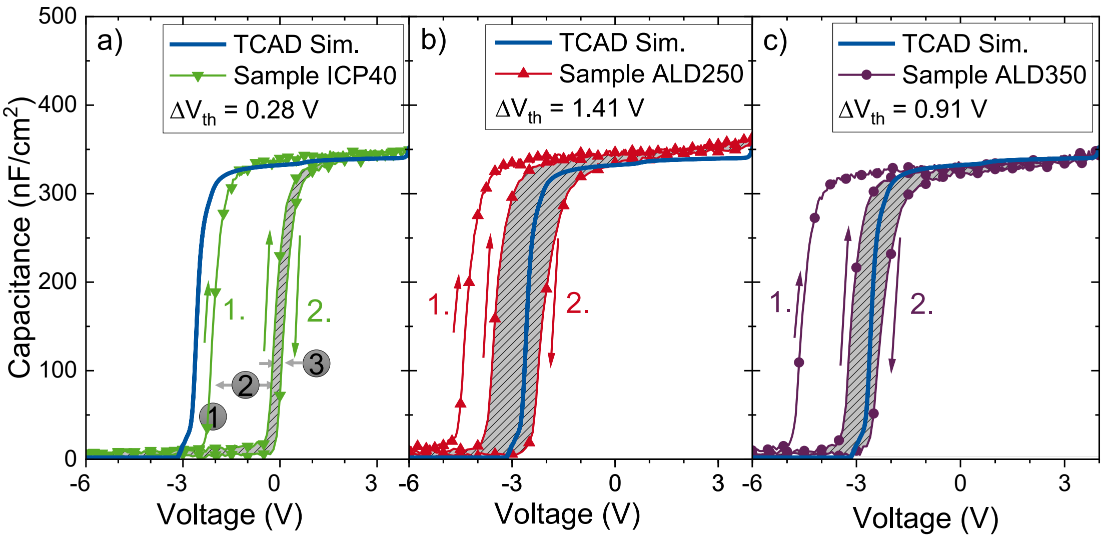


Figure 4.16.: C-V curves with initial sweep (1), shift to higher V_{th} for subsequent sweeps (2) and TCAD-simulated curve. Voltage sweep –12 V to 4 V and back. ΔV_{th} is depicted by the shaded area (3). The measurement frequency was f = 1 kHz.

V_{th} hysteresis ΔV_{th}, while the furthest shift is seen for sample ICP40. V_{th} of the different sweeps is influenced by $\sigma_{int,fixed}$ and N_{trap}, which changes during the measurements:

- First to-sweep: $V_{th,first} \sim \sigma_{int,fixed}$
- Second to-sweep: $V_{th,second} \sim \sigma_{int,fixed} - N_{trap,deep}$
- Back-sweep: $V_{th,back} \sim \sigma_{int,fixed} - N_{trap,deep} - N_{trap,shallow}$

Consequently, from V_{th} of the first to-sweep [Fig. 4.16(1)], the difference between first and second to-sweep [Fig. 4.16(2)], and ΔV_{th} [Fig. 4.16(3)], it is possible to estimate σ_{int}, $N_{trap,deep}$ and $N_{trap,shallow}$, respectively:

- $\sigma_{int,fixed}$ extracted from $V_{th,first}$
- $N_{trap,deep}$ extracted from $V_{th,first} - V_{th,second}$
- $N_{trap,shallow}$ extracted from $\Delta V_{th} = V_{th,second} - V_{th,back}$

Tab. 4.2 shows the results of these calculations. For sample REC, σ_{int} represents the total interface charge σ_{int}–$N_{trap,deep}$–$N_{trap,shallow}$, since D_{it} is fully occupied for zero bias. The results for samples ALD250 and ALD350 are similar, with slightly higher $N_{trap,deep}$ and a lower $N_{trap,shallow}$ leading to a more positive V_{th} and smaller ΔV_{th} for sample ALD350. Sample ICP40 shows the highest $N_{trap,deep}$, shifting V_{th} to –0.34 V, while it also has the lowest $N_{trap,shallow}$ leading to ΔV_{th} = 0.28 V.

Table 4.2.: Evaluated values for V_{th} of the first and second (subsequent) sweeps, σ_{int} from the position of $V_{th,first}$, $N_{trap,deep}$ from the difference of $V_{th,first}$ and $V_{th,second}$ and $N_{trap,shallow}$ from ΔV_{th}. V_{th} of sample REC is extracted from the stress curve for 0 s. Permittivity values taken from [26].

Sample	TCAD	REC	ICP40	ALD250	ALD350
$V_{th,first}$ (V)	–2.56	–7.42	–2.04	–4.31	–4.55
$V_{th,second}$ (V)	–2.56	–7.42	–0.34	–3.53	–3.21
ΔV_{th} (V)	-	-	0.28	1.41	0.91
$\sigma_{int,fixed}$ (10^{13} cm^{-2})	2.12 (σ_{GaN})	4.27	1.89	2.90	3.00
$N_{trap,deep}$ (10^{13} cm^{-2})	-	-	0.75	0.35	0.59
$N_{trap,shallow}$ (10^{13} cm^{-2})	-	-	**0.15**	0.73	0.47

As explained by Miao et al. [91], a high oxygen chemical potential is needed to form a stable oxide with low D_{it}. This can be achieved by annealing in either high-temperature oxygen atmosphere (>600 °C) or plasma-activated oxygen. Apparently, the time it takes to transfer the sample from the ICP-RIE tool to the PEALD reactor is already sufficient to oxidize the surface leading to a less favorable oxide termination (samples REC, ALD250 and ALD350). In contrast, the in-situ plasma annealing in the ICP-RIE tool leads to a stable surface oxide (sample ICP40), which results in a more positive V_{th} and low ΔV_{th} after aluminum oxide overgrowth. Consequently, an in-situ cleaning process could be necessary for a reproducible dielectric interface.

4.6. Limitations of positive V_{th} shift through dielectrics

In the previous section, an approach to reduce σ_{int} below σ_{GaN} was presented. With this process, it is possible to shift V_{th} in the positive direction by increasing the dielectric thickness t_{ins}. From the simple electrostatics in Eq. (2.14), it is implied that every MISHFET can be turned normally-off by increasing t_{ins} as long as $\sigma_{int} < \sigma_{GaN}$. However, this trend has a fundamental limit [57]. In the derivation of Eq. (2.14), the valence band edge and the hole density at the dielectric/barrier interface has not been taken into account. To a first approximation, the hole accumulation effect becomes relevant as soon as the valence band edge at the interface touches the Fermi level.

In Fig. 4.17, a simulated band diagram with conduction and valence band edge for two

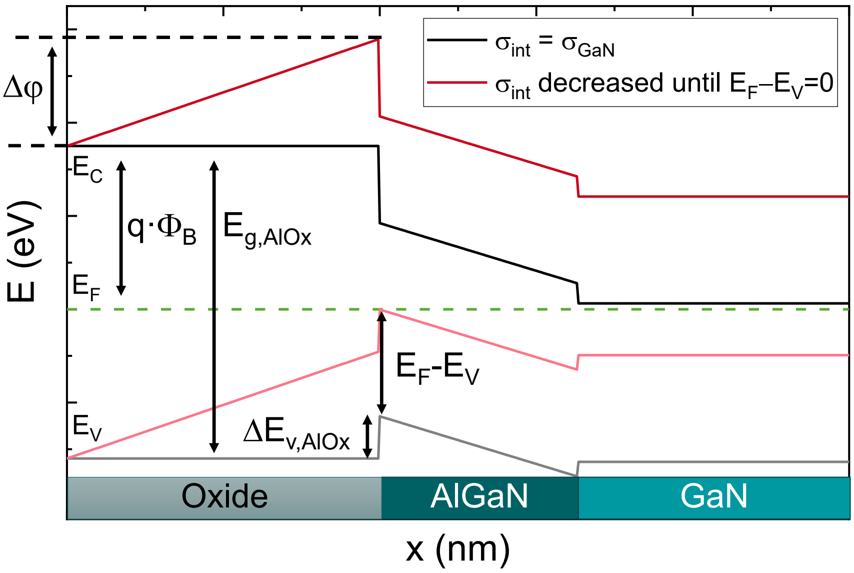


Figure 4.17.: Schematic band diagram for zero potential drop over the oxide (solid black curve) and for the case that the condition is given by Eq. (4.3) (dashed red curve).

different cases of σ_{int} is depicted. For the sake of simplicity, the structure is designed for $V_{th} = 0$ V without a dielectric. For $\sigma_{int} = \sigma_{GaN}$, the dielectric-independent case, the electric field in the oxide is vanishing. When σ_{int} is now reduced, an increasing negative electric field inside the dielectric is induced, which shifts V_{th} to more positive values. At some point the electric field is high enough, that the valence band edge at the interface touches the Fermi level (indicated by the red band diagram in Fig. 4.17). By summing up the potentials and taking into account σ_{int}, an equation for this case can be derived:

$$\frac{1}{q}(E_{g,ins} - q \cdot \phi_B - \Delta E_{v,ins/AlGaN}) + \frac{t_{ins}}{\varepsilon_{ins}}(\sigma_{int} - \sigma_{GaN}) = 0 \tag{4.3}$$

The left part of the equation is only dependent on material parameters and can be defined as a single constant:

$$\Delta\varphi = \frac{1}{q}(E_{g,AlO_x} - q \cdot \phi_B - \Delta E_{v,AlO_x/AlGaN}) \tag{4.4}$$

$\Delta\varphi$ describes the maximum potential difference across the oxide before the valence band edge reaches the Fermi level and represents the maximum possible V_{th} shift for this dielectric/AlGaN layer stack. In the case of aluminum oxide with the parameters shown in Tab. 4.3, this leads to $\Delta\varphi = 2.3$ V.

If we assume $\sigma_{int} = 0$, a critical dielectric thickness of $t_{AlO_x,crit} = \varepsilon_{AlO_x} / \sigma_{GaN} \cdot 2.3$ eV

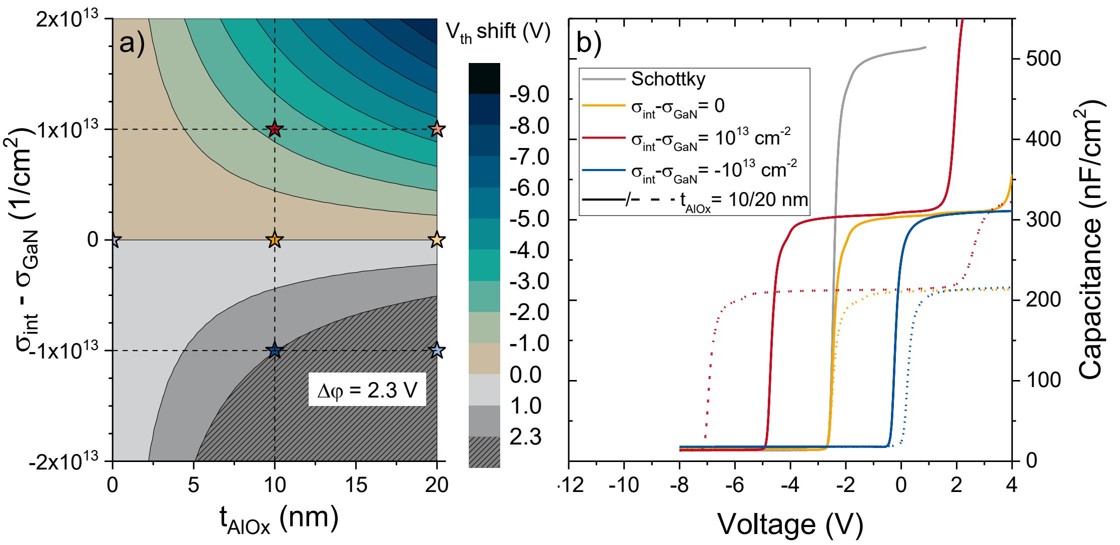


Figure 4.18.: Contour plot of t_{AlO_x} and σ_{int} impact on V_{th} and simulated C-V curves of specific value pairs (depicted by star symbols in the left figure). Shown are a Schottky reference and three different σ_{int} cases for 10 nm and 20 nm oxide thickness. The shaded area in the bottom right corner of the contour plot marks the regime, in which hole accumulation occurs and the border depicts $t_{ins,crit}$ of Eq. (4.5). The blue dashed curve of the C-V plot is represented by the light blue star and lies in the limited regime.

= 4.8 nm can be defined. Any additional t_{AlO_x} will be compensated by accumulation of holes, leaving the 2DEG unaffected. The accumulated holes may be used for advanced passivation methods, e.g. "charge-balancing" as described in [96]; however, for the present discussion, hole accumulation must be seen as a fundamental limit for threshold voltage engineering. For any other value of $0 < \sigma_{int} < \sigma_{GaN}$, the critical thickness will change according to:

$$t_{ins,crit} = \frac{\varepsilon_{ins}}{\sigma_{GaN} - \sigma_{int}} \cdot \Delta\varphi \tag{4.5}$$

To illustrate the influence of the different parameters on V_{th}, Fig. 4.18(a) shows the V_{th} shift in dependence of t_{ins} and σ_{int}. The shaded area in the bottom right corner marks the regime, in which hole accumulation at the oxide/AlGaN interface occurs. Therefore, its border marks $t_{ins,crit}$. In Fig. 4.18(b), simulated C-V curves by Sentaurus TCAD for three different σ_{int} and different t_{ins} values are shown. These different cases are depicted

Table 4.3.: Parameters of AlO_x for the calculation of the maximum potential drop Δφ.

$\mathbf{q \cdot \phi_B}$ (eV)	$\mathbf{E_g}$ (eV)	$\mathbf{\Delta E_v}$ (eV)	ε_{r,AlO_x}
3.5 [63]	6.7 [95]	0.9 [79]	8 [78]

Table 4.4.: Maximum potential drop $\Delta\varphi$ calculated for different dielectrics on an AlGaN barrier with 25% Al content.

Dielectric	ΔE_v	E_g	$q \cdot \phi_B$	$\Delta\varphi$
Units	(eV)	(eV)	(eV)	(V)
Al_2O_3	3.47	8.8	3.5	1.83
HfO_2	1.62	6.0	2.5	1.78
ZrO_2	1.52	5.8	2.5	1.78
Si_3N_4	0.65	5.3	2.1	1.75

as stars in Fig. 4.18(a). The simulation takes into account the pinning of the bands once the accumulation of holes at the insulator/barrier interface occurs. Consequently, the simulated values of V_{th} behave according to Eq. (2.14) except the curve with positive V_{th} shift and $t_{ins} = 20$ nm (blue dashed curve). Here, the simulation results in $V_{th} = -0.37$ V, which is significantly less than the value of V_{th} predicted by the simple electrostatics of Eq. (2.14), which supports the $\Delta\varphi$ limit.

The maximum dielectric potential drop $\Delta\varphi$ depends on the choice of the dielectric and the aluminum content of the AlGaN barrier. By taking the theoretical values of the different dielectrics from Fig. 2.11, the respective $\Delta\varphi$ can be calculated. The results are shown in Tab. 4.4 for an underlying AlGaN barrier with an Al content of 25%. The $\Delta\varphi$ values are quite similar with approximately 1.8 V and lower than the value calculated for the aluminum oxide above, for which the parameters were extracted from experiments. In conclusion, choosing a different gate dielectric does not change $\Delta\varphi$ and therefore is not a design parameter for a maximum positive V_{th} in a first-order approximation. However, since the interface between the various dielectrics and AlGaN will behave differently, it might be easier to achieve a sufficiently low σ_{int} with a specific dielectric.

Since $\Delta\varphi$ depends on the valence band offset between the dielectric and AlGaN barrier, it also depends on the aluminum content inside the barrier. A higher aluminum content leads to a larger bandgap and therefore a smaller valence band offset which increases $\Delta\varphi$. On the other hand, a higher aluminum content also increases σ_{AlGaN}, which leads to a negative V_{th} shift. By taking the MIS V_{th} equation Eq. (2.14) and under the assumption that the general band alignment remains constant (ϕ_B - $\Delta E_{C,ins}/q$ - $\Delta E_{C,GaN}/q = \text{const.}$), the V_{th} shift caused by the barrier and $\Delta\varphi$ in dependence on the Al content x can be expressed by:

$$\Delta V_{th}(x) = \Delta\varphi(x) - \frac{t_{AlGaN}}{\varepsilon_{AlGaN}(x)}(\sigma_{AlGaN}(x) - \sigma_{GaN}) = \Delta\varphi(x) - \varphi_{AlGaN}(x, t) \tag{4.6}$$

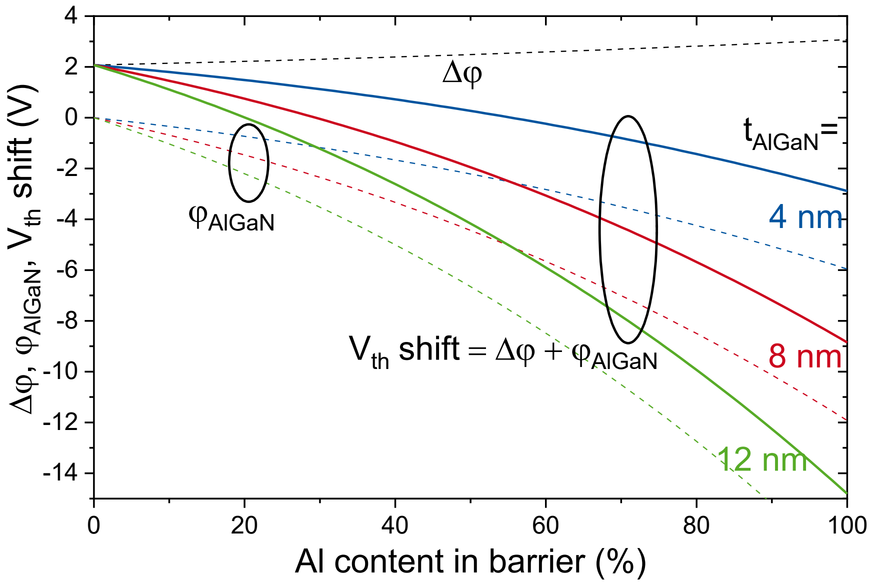


Figure 4.19.: Dependence of $\Delta\varphi$ and the AlGaN barrier term φ_{AlGaN} of Eq. (2.14) on the Al content of the barrier. The value of $\Delta\varphi$ increases with the Al content due to the decreased valence band offset, while the barrier term decreases due to the higher polarization. Even for thin barriers, φ_{AlGaN} is dominant and leads to an overall decreasing V_{th} shift.

The shift of the individual terms (dashed lines) and the sum of both terms (solid lines) for different t_{AlGaN} are depicted in Fig. 4.19. The value of $\Delta\varphi$ increases with the Al content due to the smaller valence band offset, while the barrier term decreases due to the higher polarization. Even for thin barriers, the barrier term is dominant and leads to an overall decreasing V_{th} shift. Therefore, the maximum positive V_{th} shift in Fig. 4.19 is reached at an Al content of 0% in the AlGaN barrier (= GaN), which equals an fully-recessed AlGaN barrier in a real device. These devices are called MIS-hybrid HFET and are discussed in the next chapter.

4.7. Flash-like MISHFET Memory Effect

The previous sections have shown that charge, which is stored in the AlO_x/AlGaN interface, induces a threshold voltage shift. The "permanent" shift due to $N_{trap,deep}$ is beneficial for achieving normally-off operation and is currently actively employed [97–99], while the hysteresis caused by $N_{trap,shallow}$ should be mitigated. However, these charge storage effects can also be useful for other types of devices such as erasable programmable read-only memories (EPROM) [100]. In the following part, the basic working principle of an EPROM is explained and the similarities to a MISHFET are discussed.

A schematic of a silicon EPROM and its band diagram in the neutral and charged state is presented in Fig. 4.20. Additionally, the figure shows exemplary transfer characteristics for both states.

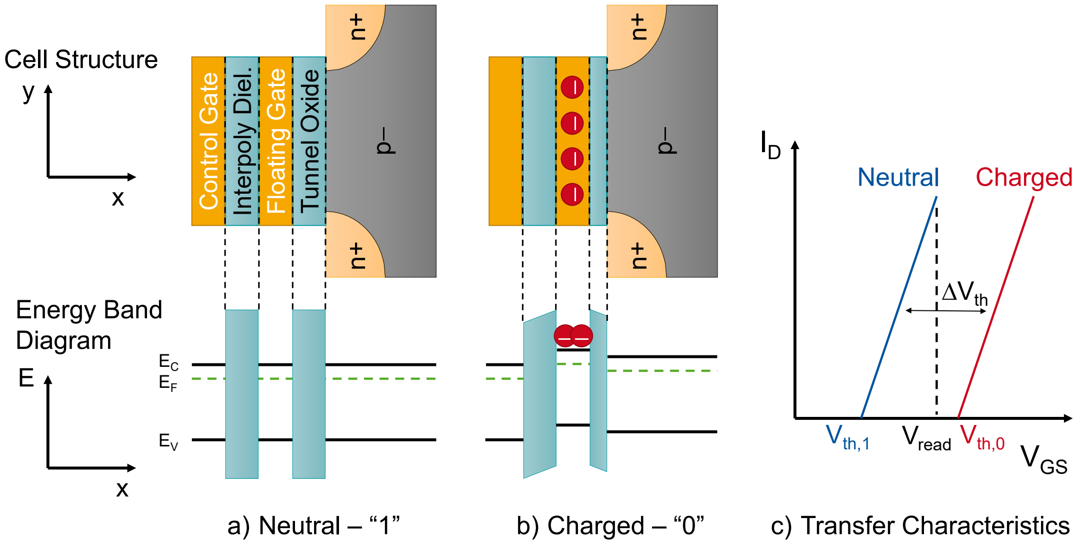

Cell Structure
y
x
Control Gate
Interpoly Diel.
Floating Gate
Tunnel Oxide
n+
p–
n+
Energy Band Diagram
E
x
E_C
E_F
E_V
I_D
Neutral
Charged
ΔV_{th}
$V_{th,1}$
V_{read}
$V_{th,0}$
V_{GS}
a) Neutral – “1”
b) Charged – “0”
c) Transfer Characteristics

Figure 4.20.: Silicon floating-gate MOSFET structure. The neutral a) and charged b) state as well as the corresponding schematic band diagrams and transfer characteristics c) are shown. Image after [100].

The EPROM consists of a standard normally-off MOSFET structure with the addition of a second gate (floating gate), which is sandwiched between oxide layers. In the neutral state of the device, the floating gate (FG) is not charged and the EPROM has a threshold voltage $V_{th,1}$. When electrons are now injected into the floating gate, it becomes negatively charged, which shifts V_{th} to the higher voltage $V_{th,0}$. Consequently by applying a gate-source voltage V_{read} between $V_{th,1}$ and $V_{th,0}$ to the control gate, a high or low current can be sensed depending on the state of the device. The high current level is commonly defined as a logic "1", while the low current level is defined as logic "0", thus the device can store one bit of information.

In an EPROM, the programming, i.e. charge injection into the floating gate, is either performed by Fowler-Nordheim (FN) tunneling or hot electron injection, both from the electron channel. This requires high gate-source voltages or high drain-source voltages, respectively. To erase the device, i.e. neutralizing the FG, it is irradiated by UV light, thus the electrons are discharged due to the photoelectric effect.

A MISHFET behaves similarly. Here, the FG between two oxide layers is substituted by the interface states D_{it} between oxide and wide-bandgap semiconductor. As discussed in section 4.2, the emission time constant of deep traps can easily exceed one year, thus the charge can be stored for a long period of time. The programming of the MISHFET is performed by driving the device in the spill-over regime, in which electrons are transferred from the 2DEG to the oxide/semiconductor interface (see Fig. 4.7). Erasing the device is also be carried out by light irradiation [99]. This is commonly used as a method to characterize the energetic distribution of the interface states inside the bandgap by using monochromatic light of different wavelengths [79].

In silicon technology, the next step for the EPROM was the electrically erasable programmable read-only memory (EEPROM), also known as flash memory [100]. In these devices, the erasing step is not performed by UV irradiation, but by a highly negative gate bias. This leads to FN tunneling of the stored electrons in the FG towards the electron channel [100]. For nitride MISHFET, in which the charge is stored in the oxide/semiconductor interface, this electrically-erasing technique has not been shown in literature yet.

A new technique proposed here to erase the device is hole injection from a two-dimensional hole gas (2DHG) into the oxide/semiconductor in a similar way to the electron injection from the 2DEG. For this purpose, a double heterostructure consisting of an AlO_x/AlGaN/GaN/AlGaN stack is used for a MISHFET, which is shown in Fig. 4.21(a). The layers are designed in such a way that a 2DEG is present at the top AlGaN/GaN interface and a 2DHG at the bottom GaN/AlGaN interface [see Fig. 4.21(b)].

The programming (SET) by driving the device in the spill-over regime (see above) is shown in Fig. 4.21(c), shifting V_{th} to the charged state. The proposed electrical erasing of the device is depicted in Fig. 4.21(d). By applying a negative potential to the surface of the structure, the bands are pulled up. At a sufficiently negative voltage, the holes from the 2DHG are transported to the oxide/AlGaN interface. The electrons trapped inside D_{it} can now recombine with these supplied holes and thus, the device is erased and V_{th} is shifted back to the neutral state. Additionally, hole trapping in the donor-like traps at the interface could occur (see section 4.2). This would shift V_{th} further to more negative voltages than the neutral state [see Fig. 4.20(c)].

For experimental proof of the proposed technique, a GaN-on-Si wafer with the following layer stack was used: 2 nm GaN cap, 25 nm AlGaN barrier with 25% Al and AlN spike, 180 nm GaN channel, AlGaN backbarrier with 10% Al, strain-relief layers and nucleation (also see appendix A.2 (Wafer II)). From this wafer, a MISHFET was fabricated according to the process depicted in Fig. 4.5. As a reference sample, an additional MISHFET from a wafer without buried 2DHG was processed. The samples are referred to as MEM and REF in the following.

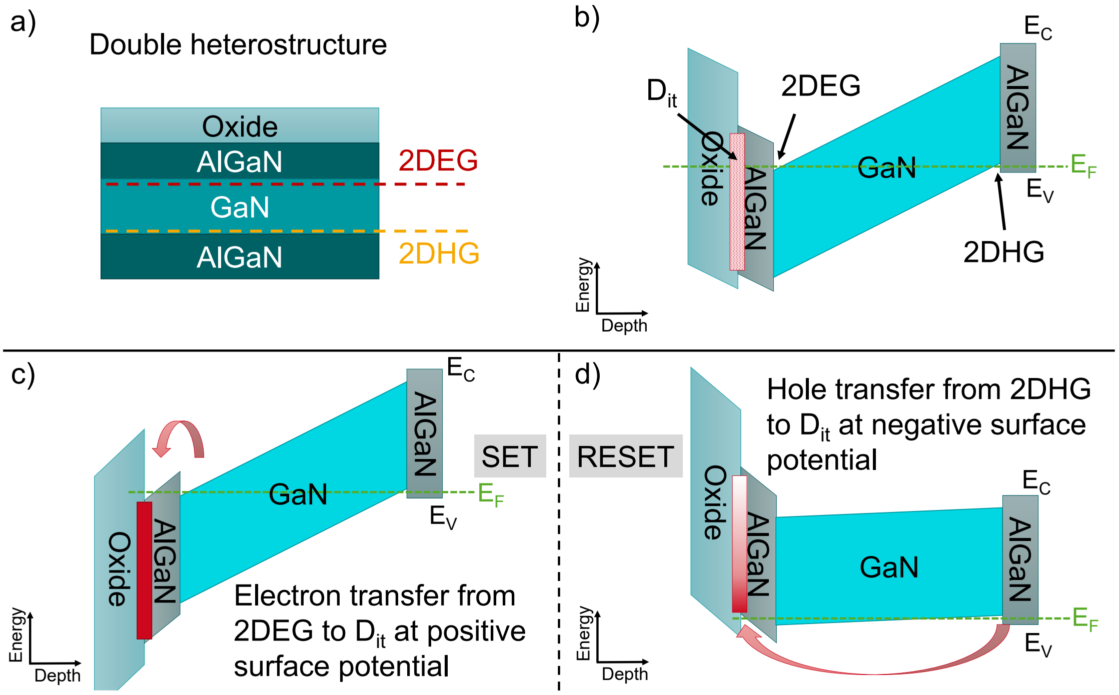

a)
Double heterostructure
Oxide
AlGaN
GaN
AlGaN
2DEG
2DHG
b)
D_{it}
2DEG
Oxide
AlGaN
GaN
AlGaN
E_C
E_F
E_V
2DHG
Energy
Depth
c)
Oxide
AlGaN
GaN
AlGaN
E_C
E_F
E_V
SET
Electron transfer from 2DEG to D_{it} at positive surface potential
Energy
Depth
d)
RESET
Hole transfer from 2DHG to D_{it} at negative surface potential
Oxide
AlGaN
GaN
AlGaN
E_C
E_F
E_V
Energy
Depth

Figure 4.21.: Schematic layer stack a) and band diagram b) of a AlO_x/AlGaN/GaN/AlGaN double heterostructure. c) Band diagram for positive surface potential to achieve spill-over of electrons (SET). d) Band diagram for a negative surface potential at which holes are transported from 2DHG to the oxide/AlGaN interface (RESET).

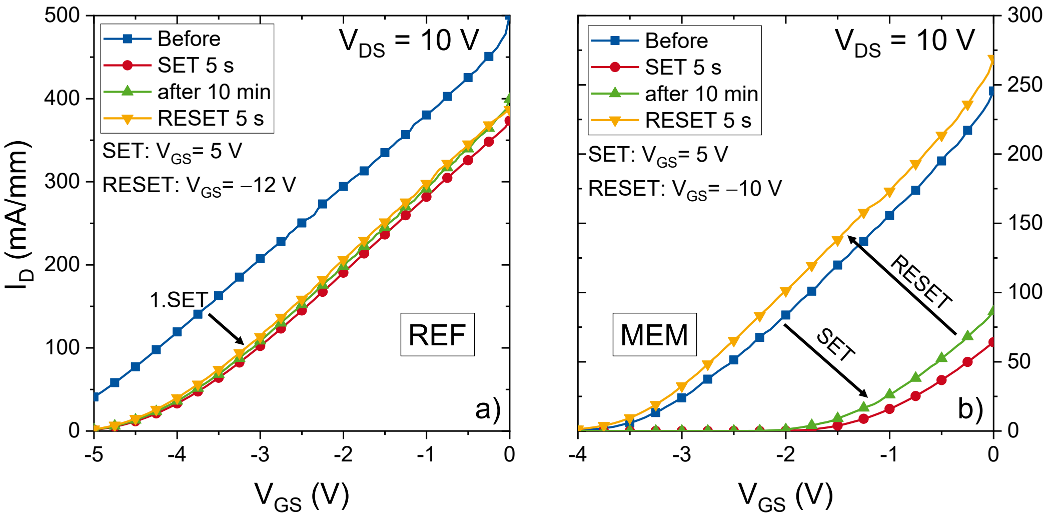


Figure 4.22.: Transfer characteristics of MISHFET with a) a conventional layer stack (REF) and b) the double heterostructure with buried 2DHG (MEM).

To evaluate the memory effect, transfer characteristics with different stress voltages in between were measured. The results are shown in Fig. 4.22. The devices were measured from $V_{GS} = 0\,V$ to $-5\,V$ (REF) or $-4\,V$ (MEM) between the different stress points to determine their V_{th}. This measurement range is chosen to ensure that the devices are neither in the SET nor the RESET regime.

The first measurement was performed for pristine device before any stress voltages were applied (blue curves). Afterwards, the devices were SET at $V_{GS} = 5\,V$ for 5 s and measured again (red curves). Both samples show an initial positive ΔV_{th} after the SET of 1.3 V and 1.9 V for REF and MEM, respectively. For all further measurements, sample REF has a relatively stable V_{th}. This indicates high charge retention and no discharging (RESET) of the interface at negative voltages. After waiting for 10 min to evaluate the short-time charge retention (green curves), V_{th} of sample MEM is shifted slightly towards negative voltages. This indicates electron emission from shallow traps. As the shift is only minor, the majority of the stored charge appears to be retained. Subsequently, the devices were RESET at $V_{GS} = -12\,V$ (REF) and –10 V (MEM) for 5 s and measured (orange curves). This RESET leads to a large negative ΔV_{th} of –2.1 V for sample MEM with a V_{th} more negative than for the initial curve. Most likely, hole trapping at the oxide/AlGaN interface occurs, leading to the observed additional V_{th} shift. These measurements prove the possibility of an electrical RESET enabled by the buried 2DHG of a double heterostructure. If the RESET was originating from FN through the AlGaN barrier, both samples should show a negative V_{th} shift after stress at their respective negative voltages.

In comparison to conventional flash memories, the programming voltage is lower for the presented devices. Silicon-based flash memory commonly has SET/RESET voltages of approximately ±15 V [101], while the presented flash-like MISHFET have a SET/RESET voltage of 5 V and –10 V, respectively. It is expected that these voltages could be even further reduced by optimizing the individual layer thicknesses.

Applications for these memories could be fully-integrated GaN circuits, which can be operated at extreme temperatures. Due to the polarization-induced carriers, no freeze-out occurs at cryogenic temperature and because of the high band gap of the group III nitrides, devices can be operated at elevated temperatures past the silicon limit. Although charge retention will decline at higher temperatures (see Fig. 4.3), it could be still sufficient for short-time data storage.

In conclusion, this chapter has discussed the trap dynamics of oxide/AlGaN interfaces. It was shown that the traps are distributed over the entire AlGaN bandgap and have different time constants. They were categorized as shallow traps, which can emits their electrons during the measurement time frame, and deep traps, which act as negative fixed charge. The deep traps can help in achieving normally-off operation as they "permanently" shift the threshold voltage to more positive values, while the shallow traps cause threshold voltages hysteresis. Additionally, the charge storage effect of the oxide/AlGaN interface was used to fabricate a flash-like memory device, for which a new erasing technique through a buried 2DHG was introduced. PDA and oxygen plasma treatments were investigated to reduce the density of traps and positive fixed charge. These values could be sufficiently reduced to enable positive threshold voltage shift with increasing oxide thickness.

Furthermore, the fundamental limit of shifting the threshold voltage by an oxide layer to more positive voltages was discussed. It was shown that the threshold voltage could be further increased by entirely removing the AlGaN barrier between oxide and GaN. This type of devices is presented in the next chapter.

5. Mobility Enhancement in MIS-hybrid HFET

The metal-insulator-semiconductor-hybrid (MIS-hybrid) HFET combines the low sheet resistance in the access regions of a conventional HFET with the normally-off operation of a MIS structure in the intrinsic FET. This leads to higher threshold voltages compared to the gate-recessed MISHFET discussed in the previous chapter, but has the drawback of a reduced mobility in the gate area.

This chapter firstly presents the structure and working principle of a MIS-hybrid HFET. Afterwards, the deposition of a two-layer gate dielectric stack is discussed and how it can improve the mobility in the gate region. Experimental results are shown, first for devices used for the mobility extraction and subsequently for a standard transistor geometry.

5.1. Metal-insulator-semiconductor-hybrid HFET

The starting point of MIS-hybrid HFET is a conventional AlGaN/GaN heterostructure with an existing 2DEG at the heterointerface. The AlGaN barrier is then fully recessed in the gate area (i.e. the entire AlGaN barrier is removed), which is locally eliminating the 2DEG below the gate. Afterwards, a gate dielectric is deposited and the device is finished by gate metallization. This leads to a metal/insulator/GaN structure in the gate area (MISFET), which is connected to the 2DEG of the an insulator/AlGaN/GaN structure (HFET) in the access regions. Thus, the device is called MIS-hybrid HFET. Fig. 5.1 depicts a schematic of this device.

This concept was first presented by Huang et al. in 2008 [102]. In comparison to the HFET Schottky gate, the MIS gate enables high positive threshold voltages. Experiments have shown V_{th} up to 7.6 V [20], which is one of the highest reported V_{th} over the various normally-off concepts for GaN devices. However, the dielectric/GaN interface in the gate area can have high ionized impurity levels, increased interface roughness

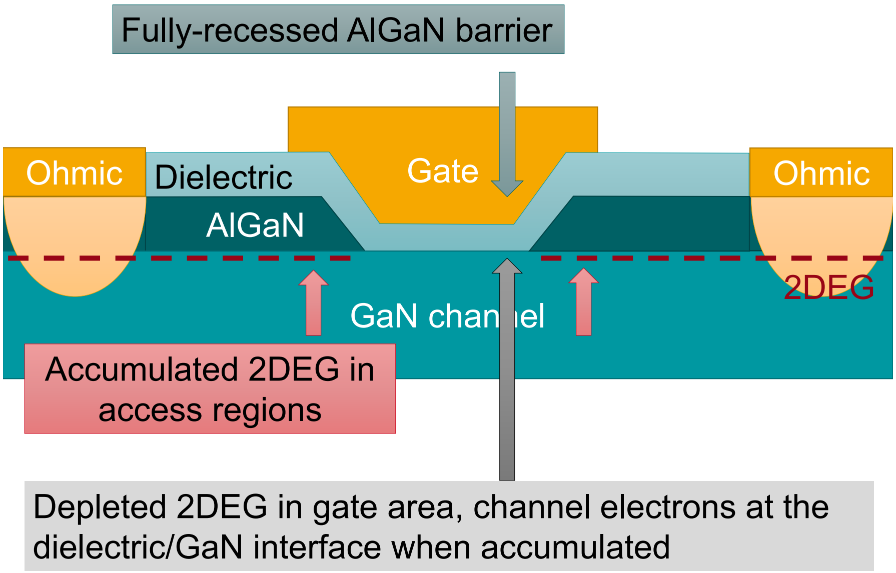

Fully-recessed AlGaN barrier
Ohmic
Dielectric
Gate
Ohmic
AlGaN
2DEG
GaN channel
Accumulated 2DEG in access regions
Depleted 2DEG in gate area, channel electrons at the dielectric/GaN interface when accumulated

Figure 5.1.: Schematic of a MIS-hybrid HFET. In the access regions, the heterostructure leads to an accumulated 2DEG, which connects the MOSFET in the gate area, in which the 2DEG is depleted, to the ohmic contacts.

due to the AlGaN-removal process and trap states. This reduces the electron mobility (see section 2.4) and can lead to V_{th} instabilities as discussed in the previous chapter, which is the main drawback of this normally-off topology. The advantage over standard MOSFET designs is the 2DEG in the access regions, which leads to improved ON-resistances.

In silicon technology, the threshold voltage of a MOSFET is defined at the onset of strong inversion [103]. This means that in an n-channel MOSFET, V_{th} is defined as the voltage, for which the electron bulk density at the oxide/semiconductor interface is equal to the bulk doping density of the p^--substrate. As the GaN channel in the MIS-hybrid HFET is not p-doped, this V_{th} definition cannot be used. Therefore, an identical one to that of the HFET is employed. An electrostatic model is derived in analogy to section 2.3, n_s is set to zero and the resulting equation is solved for V_{th}. This leads to the following equation:

$$V_{th} = \phi_B - \Delta E_C/q - \frac{t_{ins}}{\varepsilon_{ins}}(\sigma_{int} - \sigma_{GaN}) + \frac{t_{ins}}{t_{GaN}} \cdot \frac{\varepsilon_{GaN}}{\varepsilon_{ins}} \cdot \Psi_{BB} \tag{5.1}$$

This equation is similar to Eq. (2.11) for the AlGaN/GaN HFET, the only difference is the substitution of the AlGaN thickness term t_{AlGaN} and polarization term σ_{AlGaN} by the insulator thickness t_{ins} and interface charge density σ_{int}, respectively. The variables with

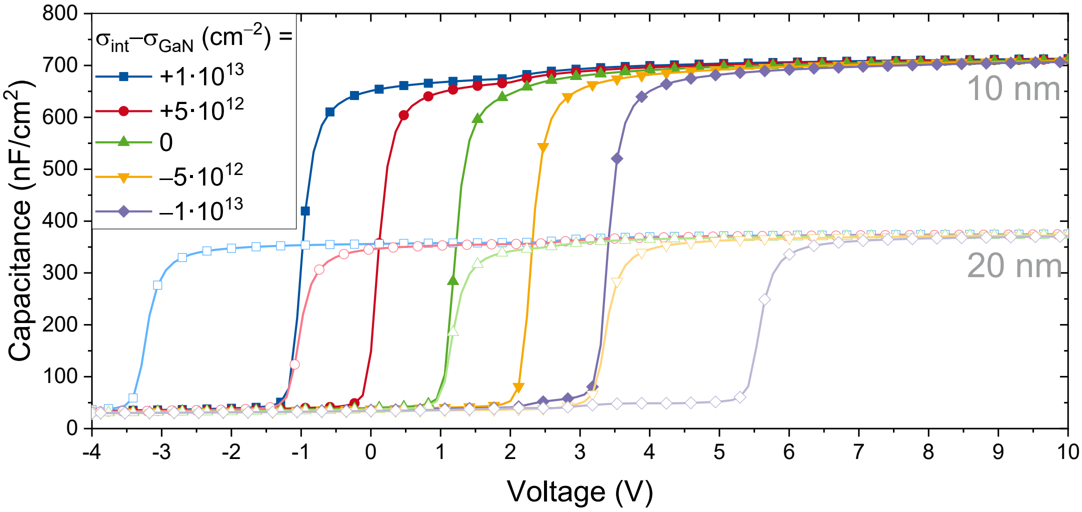


Figure 5.2.: Simulated C-V curves of a MIS diode with AlO_x thicknesses of 10 nm and 20 nm for different values of σ_{int}. The C-V curves behave according to the simple electrostatic model of Eq. (5.1).

the Fig. 5.2 shows simulated C-V curves of MIS diodes to illustrate the influence of the dielectric parameters, t_{ins} and σ_{int}, on V_{th}. The simulations were performed by Sentaurus TCAD [69]. The structure has no back barrier, therefore the backside depletion term in Eq. (5.1) is not taken into account here. The plot shows MIS diodes with five different values of $\sigma_{int} - \sigma_{GaN}$ for two different AlO_x thicknesses of 10 nm and 20 nm. For $\sigma_{int} - \sigma_{GaN} = 0$ (green), V_{th} is independent of the oxide thickness as expected from the analytical model. For $\pm\, 5 \cdot 10^{12}\,\mathrm{cm}^{-2}$, the curves are shifted by 1 V in negative/positive direction, respectively. Doubling the oxide thickness or doubling $\sigma_{int} - \sigma_{GaN}$, doubles the V_{th} shift. The model will be used in this chapter to estimate the interface charge density σ_{int} for the MIS-hybrid devices from its V_{th}.

5.2. Mobility Enhancement by an Amorphous AlN Spike

The mobility and density of the electrons in a device should be maximized to achieve low ON-resistances. While the sheet carrier density in the gate area can be increased by applying a higher gate bias, the electron mobility depends on the semiconductor materials and their interfaces. One method to increase the mobility is the introduction of a thin AlN spike between AlGaN and GaN (see section 2.4).

In a MIS-hybrid HFET, a similar effect is expected from the deposition of a two-layer dielectric consisting of amorphous AlN and AlO_x. By first depositing an amorphous nitride (AlN) on top of the crystalline nitride (GaN) followed by an amorphous oxide (AlO_x), the formation of an interface with a higher degree of order between dielectric and semiconductor is expected. This can lead to a reduction of trap states. Additionally, the AlN spike prevents oxidation of the GaN surface during the oxide deposition (see chapter 4). Thus, the AlN spike could mitigate the V_{th} hysteresis and improve the electron mobility. The advantage of a monocrystalline PEALD AlN interlayer was already proven for MIS-hybrid HFET with a mobility increase of 68% [19], but the devices had only a low V_{th} of 0.3 V. By employing an amorphous AlN spike instead of a monocrystalline one, an increased mobility and a high V_{th} at the same time are expected.

5.2.1. PEALD of Amorphous Aluminum Nitride

To take full advantage of the two layer dielectric, the deposition of AlN and AlO_x should be performed within the same tool. Exposition of the sample surface to atmosphere between two process steps can cause contamination or surface reactions as shown in the previous chapter. Therefore, a process for amorphous PEALD AlN was developed, which enables AlN and AlO_x deposition within the same tool. This process has particular safety constraints since the gas mixture inside the chamber should be non-ignitable at all times and the employed precursors should raise no safety concerns for the tool users.

For the deposition of AlN, aluminum and nitrogen sources are needed. The most common aluminum precursor is TMAl, which is already used in the AlO_x deposition process. In literature, the nitrogen precursor for AlN deposition is either ammonia (NH_3) or a mixture of nitrogen and hydrogen gas (N_2/H_2) [104–106]. Ammonia and hydrogen gas in combination with residual oxygen from AlO_x processes or in case of tool malfunctioning can form an explosive mixture ("Knallgas") and thus do not meet the safety requirements. However, H_2 is necessary for the chemical reactions during PEALD, because nitrogen radicals are not able to remove the methyl ligands of the TMAl-terminated surface (see Fig. 4.1). Tarala et al. have shown that a ratio of at least 20% H_2 to 80% N_2 is needed for AlN growth [107].

To meet the hydrogen and safety requirements at the same time, a new PEALD process with a mixture of N_2 and forming gas (4% H_2 in Ar) is developed. The deposition scheme is illustrated in Fig. 5.3(a). During the whole process, constant gas flows of 10 sccm N_2 and 65 sccm 4% H_2 in Ar are set. The cycle starts with a 50 ms TMAl dose

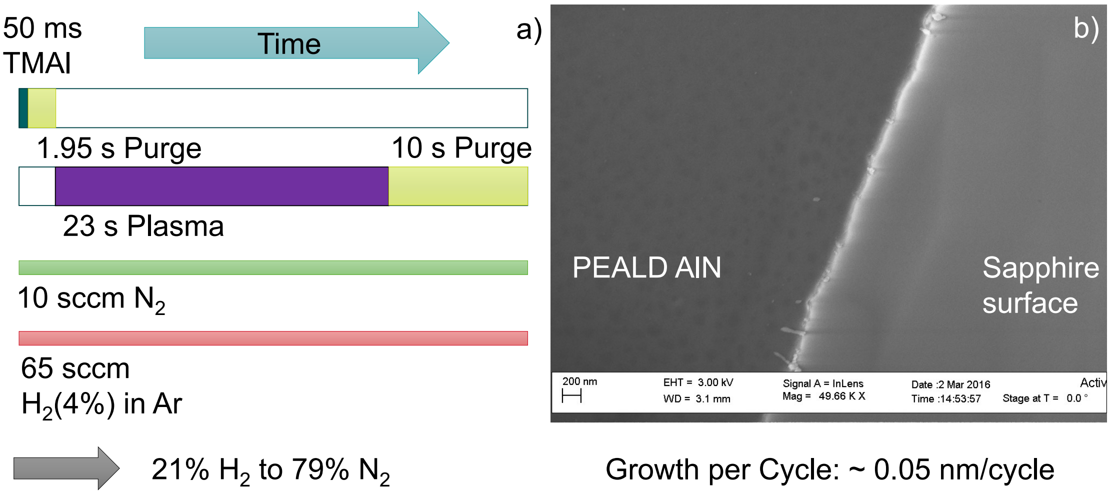

50 ms
TMAl
Time
a)
1.95 s Purge
10 s Purge
23 s Plasma
10 sccm N2
65 sccm
H2(4%) in Ar
21% H2 to 79% N2
b)
PEALD AlN
Sapphire surface
200 nm
EHT = 3.00 kV
WD = 3.1 mm
Signal A = InLens
Mag = 49.66 K X
Date :2 Mar 2016
Time :14:53:57
Stage at T = 0.0 °
Activ
Growth per Cycle: ~ 0.05 nm/cycle

Figure 5.3.: PEALD process for the deposition of amorphous aluminum nitride (AlN). a) Deposition scheme for the PEALD process. b) SEM image of the deposited AlN thin film with a thickness of approximately 50 nm. The growth per cycle is 0.05 nm/cycle.

with a purge period of 1.95 s. Afterwards, a remote-plasma of the N_2/H_2/Ar gas mixture is ignited for 23 s with a purge period of 10 s. Longer plasma durations in comparison to the AlO_x process are needed since the H_2 content is at the lower limit (20.6%). This increases the time needed for the removal of TMAl methyl ligands at the surface compared to a plasma with a higher hydrogen content. The growth per cycle is approx. 0.05 nm/cycle.

The deposited thin film was characterized by scanning electron microscopy (SEM) and X-ray photoelectron spectroscopy (XPS). Fig. 5.3(b) presents an SEM image of an AlN thin film on a sapphire substrate. Part of the AlN was removed to form an edge, enhancing the visibility of the AlN layer. The image shows a closed AlN surface with no visible holes or ridges. An XPS measurement of the deposited film reveals a composition of 49% Al, 19% N, 28% O and 4% C. The high oxygen content originates most likely from oxidation of the AlN layer prior to the measurement. AlN is prone to oxidation in air atmosphere [108] and the measurement was not immediately performed after the deposition. This oxidation is also a reason why using only an amorphous AlN layer as dielectric is not viable, if the sample has to be transported through air between different process steps. A solution would be a cluster tool, in which etching, AlN deposition and metallization can be performed without exposing the samples to atmosphere. However, the XPS results indicate a decent material quality in terms of stoichiometry compared to literature values [106, 109]. The nitrogen content is higher than for samples from [106] grown with N_2-only plasma (7% N), but lower than the samples from [106] grown with ammonia or N_2/H_2 with a 1:1 ration (42% N). This proof-of-concept shows that a nitrogen and forming gas mixture allows for PEALD AlN growth. The PEALD AlN process presented in this section was used in the following experiment.

5.2.2. Comparison of MIS-hybrid HFET with and without amorphous AlN spike

To investigate the effect of the amorphous AlN spike on the dielectric/GaN interface, MIS-hybrid devices depicted in Fig. 5.1 were fabricated. The epitaxial stack of the template consists of a 23 nm AlGaN barrier with 24% Al and AlN interlayer on a GaN buffer with AlGaN staircase and AlN nucleation on silicon (also see appendix A.2 (Wafer IV)). First, ohmic contacts were processed and subsequently mesa areas were patterned by dry-etching. Afterwards, the sample was passivated with SiN_x and the gate area is opened by a fluorine dry-etch. The AlGaN barrier (and epitaxial AlN interlayer) in the opened gate area was entirely removed by a digital BCl_3/O_2 dry etch, which was optimized for minimum material damage and low etch rates [17]. Afterwards, the gate dielectric was deposited by PEALD. On one sample, 20 nm AlO_x was deposited, while another one was fabricated with 4 nm AlN and 16 nm AlO_x. Additionally, a PDA is performed at 500 °C for 10 min. The samples were finished by Ni/Au gate metal deposition including integrated field plates, followed by contact pad deposition. For the access regions, Hall- and van-der-Pauw measurements of the passivated heterostructure show a mobility of 2085 cm^2/Vs and a sheet carrier density of $6.06 \cdot 10^{12}\,cm^{-2}$, resulting in a sheet resistance of 493 Ω/sq.

The transport properties in the MOS gate area are investigated by I-V and C-V measurements of devices with a large gate area of $100\,\mu m \cdot 100\,\mu m$, so-called FATFET (see appendix A.5). The results are presented in Fig. 5.4. All measurements were performed after an initialization sweep from -2 V to 10 V. Fig. 5.4(a) shows transfer curves at a low V_{DS} of 0.1 V, thus the devices operate in their linear regime. The OFF-current of approx. 10^{-4} mA/mm is similar for both samples. The threshold voltage extracted at 1 µA/mm is 4.65 V and 2.45 V for the AlO_x and AlN+AlO_x sample, respectively. These values correspond to an interface charge density σ_{int} of $1.42 \cdot 10^{13}\,cm^{-2}$ and $1.94 \cdot 10^{13}\,cm^{-2}$, respectively. They are in the range of the lowest σ_{int} achieved for the MISHFET structures of section 4.5. The gate leakage current for both samples is below 10^{-6} mA/mm for 10 V forward bias.

In Fig. 5.4(b), C-V measurement results of the two samples are shown. Similar to the

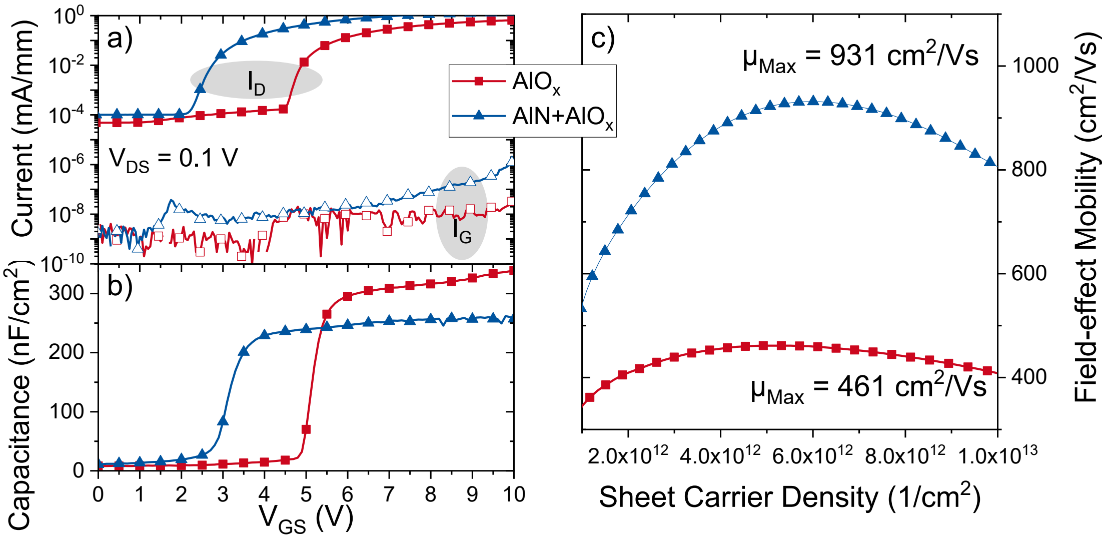


Figure 5.4.: I-V and C-V measurements of FATFET devices with L_G and W_G of 100 µm for the AlO$_x$ (red) and AlN+AlO$_x$ (blue) sample. a) Transfer curves of the devices showing a low gate leakage current and a V_{th} of 4.65 V and 2.45 V for the AlO$_x$ and AlN+AlO$_x$ sample, respectively. b) C-V curve of the two samples. c) Extracted field-effect mobility.

transfer curves, the sample with AlO$_x$ has a higher V_{th} and also a higher capacitance of 338 nF/cm^2 at V_{GS} = 10 V than for the AlN+AlO$_x$ sample. This corresponds to a dielectric thickness of 21 nm (assuming a plate capacitor), which is in good agreement with the deposited AlO$_x$ thickness. For the AlN+AlO$_x$ sample, a capacitance of 257 nF/cm^2 at 10 V is extracted. This corresponds to a thickness of 28 nm by assuming a relative dielectric constant of 8 [110] for the AlN+AlO$_x$ stack. This is higher than the targeted thickness of 4+16 nm for the AlN+AlO$_x$. The AlN growth rate depends on the initial surface conditions and temperature [109, 111]. As the process is calibrated on a bare silicon sample, the growth rate on a GaN sample could be higher than expected, because the surface termination and the surface temperature are different. Assuming twice the growth rate of 0.1 nm for AlN, its layer thickness would increase to 8 nm. Calculating the expected capacitance for a 8+16 nm AlN+AlO$_x$ stack leads to 261 nF/cm^2 by assuming a dielectric constant of 5.76 for AlN [109]. This is in better agreement with the measured capacitance.

The combination of the FATFET I-V and the C-V measurements enables the extraction of the field-effect mobility of the fabricated devices [112]:

$$\mu_{eff} = \frac{g_{DS}}{n_s \cdot q} \cdot \frac{L_G}{W_G} \tag{5.2}$$

the channel conductance g_{DS} can be calculated from the drain current and voltage I_D/V_{DS} in the linear region for different V_{GS}, whereas the sheet carrier density n_s can be extracted from the integration of the C-V measurement. Fig. 5.4(c) presents the results of the field-effect mobility extraction. The AlO_x sample has a maximum μ_{Max} of 461 cm²/Vs, whereas the AlN+AlO_x sample has a maximum μ_{Max} of 931 cm²/Vs showing an increase in μ_{Max} of 102%. As described in section 2.4, the mobility depends on Coulomb and interface roughness scattering as well as the carrier confinement in the 2DEG. Both dielectrics, AlN and AlO_x, have a high ΔE_C to GaN, and the same material and etching process is used. Therefore, the carrier confinement and the interface roughness should be similar for both samples. The main difference between the two samples is their V_{th} caused by different interface charge densities σ_{int}. The AlO_x sample has a net interface charge density of $\sigma_{int} - \sigma_{GaN} = -0.7 \cdot 10^{13}\,\mathrm{cm}^{-2}$, while AlN+$AlO_x$ shows $\sigma_{int} - \sigma_{GaN} = -0.2 \cdot 10^{13}\,\mathrm{cm}^{-2}$ leading to reduced coulomb scattering. Furthermore, the GaN surface is exposed to oxygen radicals during the AlO_x PEALD process, which leads to oxygen incorporation [113] and thus increased coulomb scattering by ionized impurities. In contrast, the nitrogen plasma of the AlN PEALD process fills nitrogen vacancies of the GaN surface [114], which reduces the ionized impurity density. In conclusion, the expected reduction of σ_{int} due to a higher degree of order at dielectric/GaN interface for the AlN+AlO_x sample could not be observed, but a higher mobility due to reduced coulomb scattering could be achieved.

5.2.3. Electrical characteristics of MIS-hybrid HFET with standard geometry

Since the long-gate FATFET devices are hampered by low ON-currents and high ON-resistances only due to their geometries, they are not suited for real applications. Therefore, MIS-hybrid devices with standard device geometry were characterized. First, the results of the AlO_x samples are presented and subsequently the results of the AlN+AlO_x sample. Afterwards, the results of both samples are discussed. The device geometry is $L_{GS}/L_G/L_{GD}/L_{DS}/W_G$ of 2 / 2.5 / 2.5 / 7.0 / 2 · 50 µm unless stated otherwise (see appendix A.5). From the prior results, threshold voltages over 4 V for the AlO_x sample and very low gate leakage currents are expected.

Fig. 5.5 shows the transfer characteristics of samples in semilogarithmic and linear scale. All measurements were taken after an initialization sweep with the same voltage range as the actual measurement. The sweep direction is from negative to positive voltages and back. V_{th} is extracted from the to-sweep at 1 mA/mm in the semilogarithmic scale and additionally from linear extrapolation in the plots with linear scale.

The semilogarithmic transfer curve of the AlO$_x$ sample is shown in Fig. 5.5(a). The OFF-current of $1.2 \cdot 10^{-3}$ mA/mm is by an order of magnitude higher than the gate current of $1.1 \cdot 10^{-4}$ mA/mm, indicating a limitation by the buffer leakage current. Mesa isolation measurements reveal a current of $6.1 \cdot 10^{-4}$ mA/mm at 10 V, supporting this assumption. The ON-current equals 630 mA/mm at $V_{GS} = 8$ V, which leads to an ON/OFF-ratio of 10^6. The gate current of the sample appears high compared to that of the FATFET device. This deviation originates from a different device design. The standard device design has large contact pads on top of the conductive GaN buffer (see appendix A.5), which leads to high currents between the contact pads. Thus, the actual gate current is masked by the high pad currents. In contrast, the FATFET device has no contact pads, therefore the measured current is only determined by gate leakage.

In the following, the threshold voltage is investigated. V_{th} of the to and back sweep of 2.9 V and 3.02 V, respectively, show only a small ΔV_{th} of 0.12 V. This corresponds to $\sigma_{int} = 1.8 \cdot 10^{13}$ cm^{-2} and $N_{trap,shallow} = 2.6 \cdot 10^{11}$ cm^{-2}. The linear extrapolation leads to a V_{th} of 3.54 V and a ΔV_{th} of 0.07 V, which is shown in Fig. 5.5(b). The achieved ON-current in combination with high V_{th} and low ΔV_{th} represent good electrical properties in comparison to literature values [20].

Next, the measurement results from the AlN+AlO$_x$ samples are presented. Fig. 5.5(c) shows the semilogarithmic transfer characteristics. The OFF-current of $4.4 \cdot 10^{-3}$ mA/mm is slightly higher than that of the AlO$_x$ sample and is also limited by buffer leakage. The ON-current of the device equals 688 mA/mm at $V_{GS} = 6$ V, leading to an ON/OFF-ratio of 10^5. In terms of threshold voltage, the devices shows a V_{th} of –3.6 V and –3.0 V for the to and back sweep, respectively, and a ΔV_{th} of 0.6 V. This corresponds to $\sigma_{int} = 2.9 \cdot 10^{13}$ cm^{-2} and $N_{trap,shallow} = 9.6 \cdot 10^{11}$ cm^{-2}. Fig. 5.5(d) displays the linear plot, from which the linear extrapolation leads to a V_{th} of –1.59 V and a medium ΔV_{th} of 0.64 V.

The device threshold voltages of the two samples, summarized in Tab. 5.1, show a large difference between the two samples, and particularly in comparison to their corresponding FATFET devices of the previous section. The AlO$_x$ sample shows $V_{th} = 4.65$ V for the FATFET in contrast to 2.9 V for the standard geometry of the HFET, while the AlN+AlO$_x$ sample has $V_{th} = 2.45$ V for the FATFET in contrast to –3.6 V. The difference in device geometry between the FATFET devices and the transistors presented here is a reduced gate length from 100 µm to 2.5 µm. Therefore, for further investigation of the V_{th} dependence on L_G, devices with different gate lengths were measured. Fig. 5.6 shows the results for the AlO$_x$ a) and AlN+AlO$_x$ b) sample. Both samples show a simi-

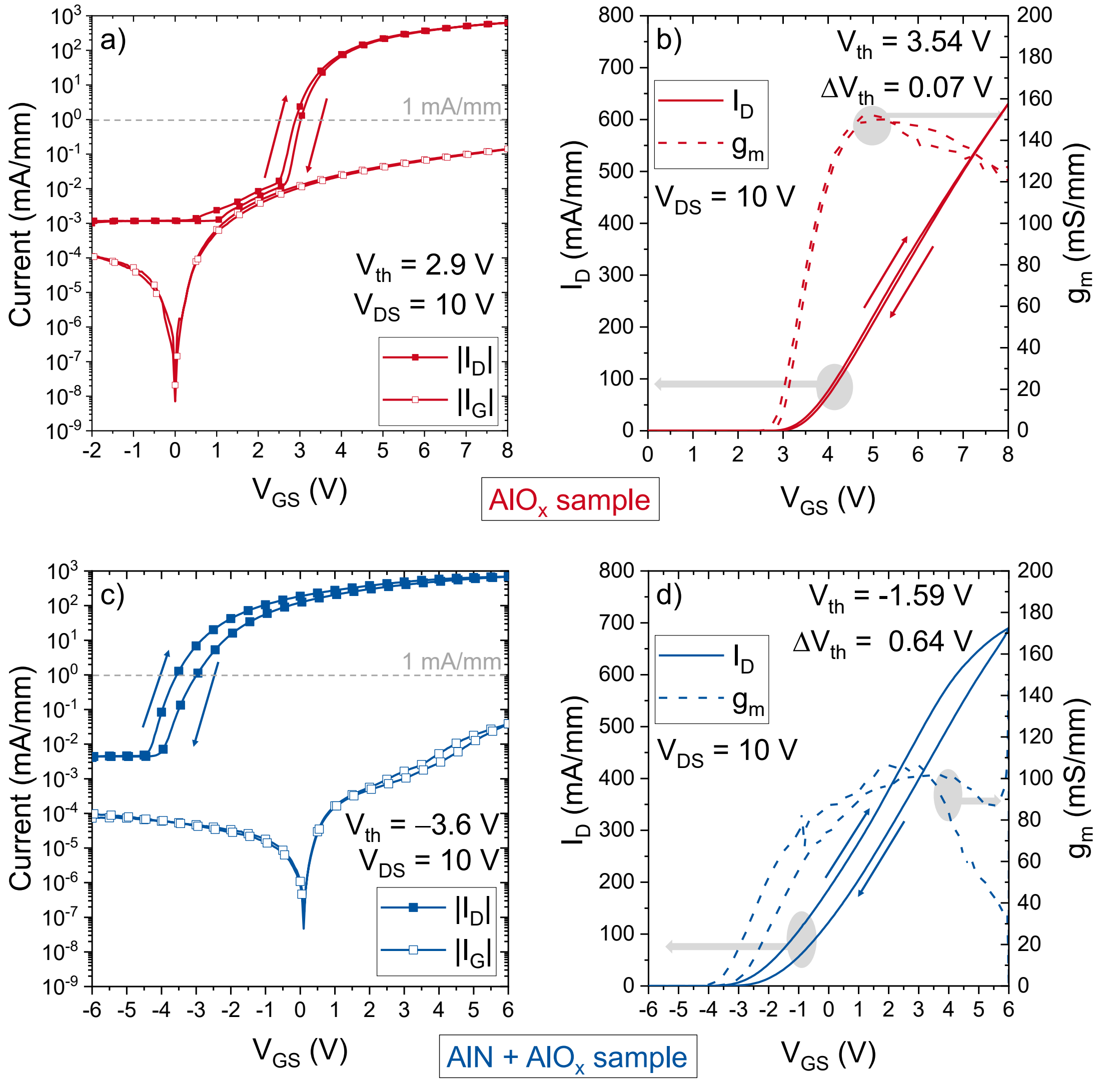


Figure 5.5.: Transfer characteristics of MIS-hybrid with standard geometry. a)+c) Semilogarithmic curves of drain- and gate currents for different drain-source voltages V_{DS} after an initialization sweep. b)+d) Linear curve of the drain current at $V_{DS} = 10\,V$.

Table 5.1.: Threshold voltages extracted from semilogarithmic plots of the FATFET and HFET of both samples.

	V_{th,AlO_x} (V)	$V_{th,AlN+AlO_x}$ (V)
FATFET	4.65	2.45
HFET	2.9	-3.6

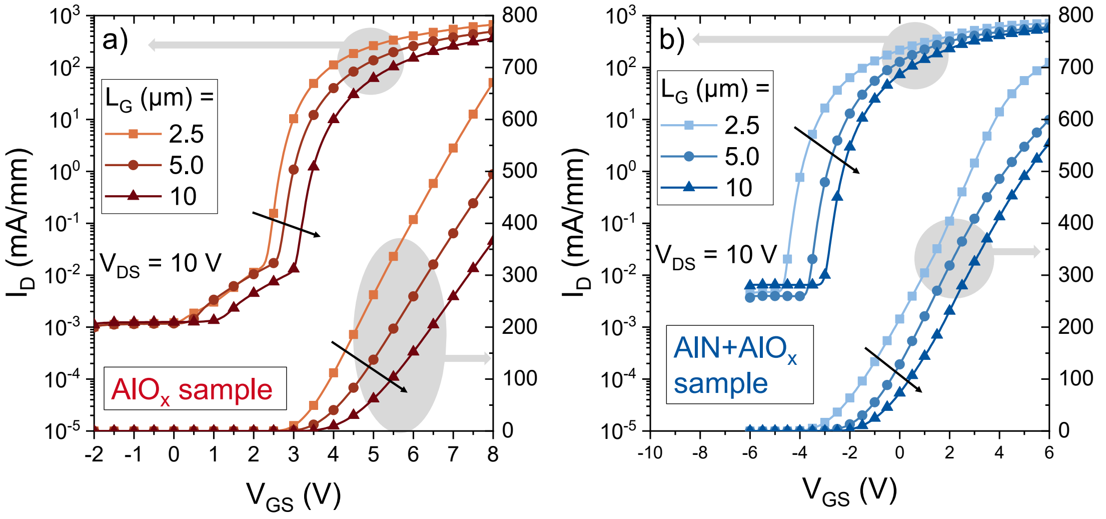


Figure 5.6.: Semilogarithmic and linear transfer curves measured for devices with different gate lengths. Measurements were performed at $V_{DS} = 10$ V. a) AlO$_x$ sample. b) AlN+AlO$_x$ sample.

lar increasing V_{th} with increasing gate length. This is most likely caused by a systematic error in the recess depth and gate oxide thickness due to different gate opening areas, as the threshold voltages for a perfect device should not depend on the gate length (outside of short channel effects). However, the large deviation between the FATFET and standard geometry transistor for the AlN+AlO$_x$ sample of 6 V towards negative voltages is unexpected. An explanation would be an incomplete removal of the AlGaN barrier in the gate openings for geometries smaller than the FATFET. However, a simple increase in positive fixed charge at the AlN/GaN interface cannot be excluded. For a deeper understanding, TEM imaging would be necessary.

The DC characteristics of the AlO$_x$ sample show stable and positive V_{th}. Therefore, pulsed measurements were performed to evaluate the device under switched-mode operation. The resulting output characteristics are shown in Fig. 5.7. The results show standard transistor behavior with an R_{ON} of 3.83 Ωmm without any visible dynamic increase or current collapse. Therefore, the output characteristics indicate a good interface between the gate dielectric and surface passivation without charge trapping effects.

In this chapter, the mobility enhancement by a PEALD AlN interlayer in a MIS-hybrid HFET could be successfully demonstrated. However, further results from DC characterization have shown, that the investigated devices with AlN+AlO$_x$ dielectric cannot benefit from the enhanced mobility. The devices feature a normally-on behavior with a medium V_{th} hysteresis. With an optimization of dry-etching and the AlN deposition, a stable device operation might be achieved. In contrast, the AlO$_x$ sample shows

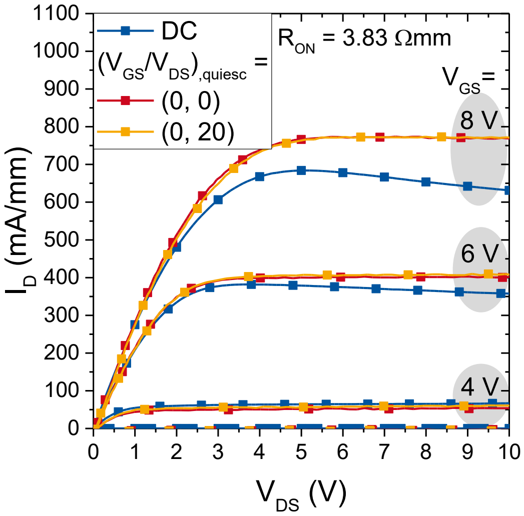


Figure 5.7.: DC- and pulsed output characteristics of the AlO_x sample. R_{ON} is extracted at the highest V_{GS} at 100 mA/mm.

promising electrical properties with a stable V_{th} of 3.54 V, after an initialization sweep, and a high ON-current of 688 mA/mm. Both devices show a rather high OFF-state leakage, which can be attributed to the leaky GaN buffer and the resulting pad leakage current. This effect can be mitigated by employing an insulating carbon-doped [115] or AlGaN back barrier buffer [116] or contact pads on top of a thick insulating dielectric.

Furthermore, the results of the MISHFET and MIS-hybrid HFET have shown, that controlling the charge distribution at the interface between insulator and semiconductor as well as the etch depth can be challenging. Different environmental conditions and manufacturing tool drift influence these parameters. Therefore, achieving reproducible results in a mature process chain can be difficult and the processes have to be well optimized. To avoid this challenges, the threshold voltage can be shifted to positive values without using a gate dielectric by another concept, the p-GaN-gated HFET, which is presented next.

6. Processing of p-GaN-gated AlGaN/GaN HFET

The normally-off HFET employing a p-GaN gate has seen growing attention in industry and research and made significant progress in recent years. It was first introduced by Hu et al. in the year 2000 [21]. Its basic principle relies on the elevation of the conduction band edge in relation to the Fermi level by introducing a p-GaN layer on top of the AlGaN barrier in the gate region. This depletes the underlying 2DEG rendering the device normally-off. An advantage over the MISHFET and the MOS-hybrid devices is the avoidance of an insulator/semiconductor interface in the gate area. Interfaces between the different layers grown by MOCVD are usually sharper and feature lower levels of additional fixed charge σ_{int} besides the polarization. This leads to more stable and reproducible threshold voltages.

This chapter first discusses the structure and working principle of the p-GaN-gated HFET. Challenges for device manufacturing are identified and solutions are presented in a full process chain. Experimental results for a high operation voltage p-GaN-gated HFET are shown and its suitability for high-temperature electronics is analyzed. Additionally, a second series of p-GaN-gated HFET was processed, which was aimed at a more positive threshold voltage. The chapter concludes with advanced device concepts for further improvements. Parts of the following results are already published in [117].

6.1. p-GaN-gated HFET

In a conventional HFET, the sheet carrier density of the 2DEG is primarily determined by the composition and thickness of the barrier [cf. Eq. (2.13)]. For a p-GaN-gated HFET, the 2DEG density in the access region equals that of a conventional HFET, while it is depleted by the p-GaN in the gate area. Thus, the whole device is of normally-off type.

A schematic cross section of the device and the corresponding simulated band dia-

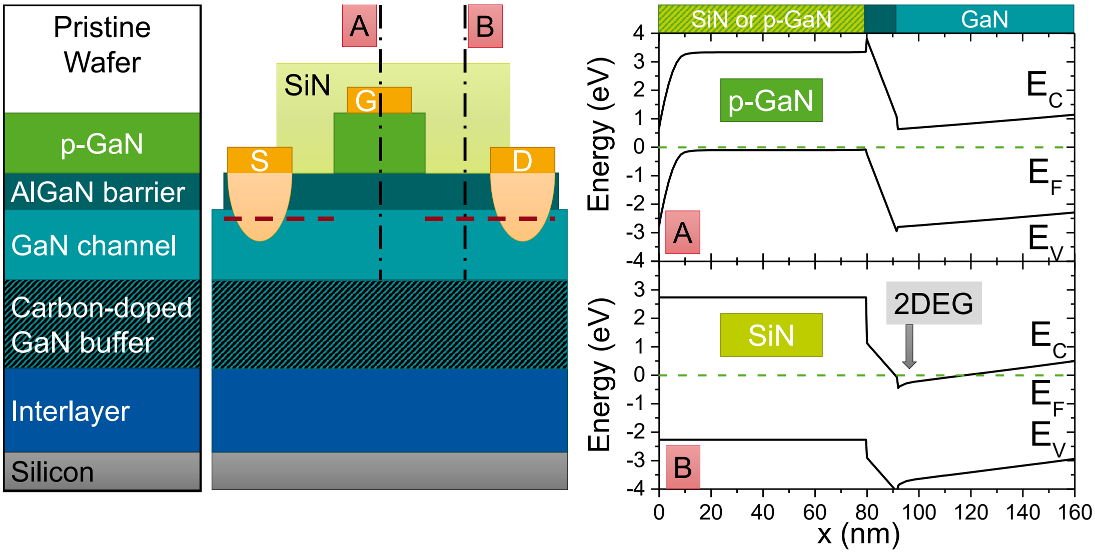


Figure 6.1.: Schematic cross section of a p-GaN-gated HFET with simulated band diagrams of the gate area (A) and the access regions (B).

grams for the gate area and access regions are shown in Fig. 6.1. The left side of the picture depicts a common epitaxial stack starting with a silicon substrate, followed by an interlayer, a carbon-doped insulating GaN buffer, a GaN channel, an AlGaN barrier and a top p-GaN layer. During device processing, the p-GaN outside the gate area is removed to re-accumulate the 2DEG in the access regions [see Fig. 6.1(B)], which here leads to a structure identical to that of an AlGaN/GaN HFET. In the gate area [see Fig. 6.1(A)], the Fermi level of p-GaN is close to the valence band edge. Thus, the energy levels of the AlGaN barrier are pulled up and as long as the potential drop over the barrier is small enough, the conduction band edge at the AlGaN/GaN interface is located above the Fermi level. This condition leads to an upper limit for the AlGaN barrier in terms of thickness t_{AlGaN} and polarization σ_{AlGaN} (i.e. Al content) for normally-off operation $V_{\mathrm{th}} > 0$. In a first-order approximation and by neglecting back-side depletion, the threshold voltage in a p-GaN-gated HFET is determined by the following equation:

$$V_{\mathrm{th}} = \frac{1}{q}(E_{\mathrm{g,GaN}} - E_{\mathrm{F,p\text{-}GaN}}) - \frac{t_{\mathrm{AlGaN}}}{\varepsilon_{\mathrm{AlGaN}}}(\sigma_{\mathrm{AlGaN}} - \sigma_{\mathrm{GaN}}), \tag{6.1}$$

where $E_{\mathrm{g,GaN}}$ is the GaN bandgap, $E_{\mathrm{F,p\text{-}GaN}}$ the distance between Fermi level and valence band edge in p-GaN, and the third term in Eq. (6.1) defines the potential drop over the barrier. A detailed theoretical study of the threshold voltage of p-(Al)GaN-gated HFET can be found in [118]. In the following, the limitations of the simple electrostatic model are shown and the influence of different design parameters is discussed.

Simulations by Sentaurus TCAD [69] were performed for each respective design parameter. An overview of the layer stack and the parameter variations can be found in the appendix A.3.

Influence of p-GaN thickness

Firstly, the V_{th} equation (6.1) does not depend on the p-GaN thickness $t_{p\text{-GaN}}$. This holds true as long as the p-GaN thickness is larger than the space-charge region (SCR) width in the p-GaN below the Schottky gate contact. Fig. 6.2(a) shows calculated values of the SCR width versus Mg-doping density [71, 119]. A metal work function of 4.6 eV (resembling Mo metallization) is assumed. As the SCR width is proportional to $1/\sqrt{N_A}$ [71], the linear curve in the logarithmic plot has a slope of –1/2. A doping density of $3 \cdot 10^{19}\,\text{cm}^{-3}$ leads to an SCR width of approximately 10 nm. The influence of p-GaN thicknesses $t_{p\text{-GaN}}$ below this width is illustrated by simulated conduction band diagrams of p-GaN/AlGaN/GaN heterostructures in Fig. 6.2(b). In the case of $t_{p\text{-GaN}} = 5$ nm (blue), 2DEG is still accumulated. At $t_{p\text{-GaN}} = 10$ nm (red), the conduction band is elevated high enough to deplete the 2DEG, but the SCR still reaches the AlGaN barrier. For $t_{p\text{-GaN}} \geq 20$ nm, the SCR is fully developed and the distance between conduction band edge and Fermi level stays constant. This leads to a constant V_{th}, which is shown by the simulated transfer characteristics in Fig. 6.2(c). The curves for 20 nm to 80 nm are on top of each other.

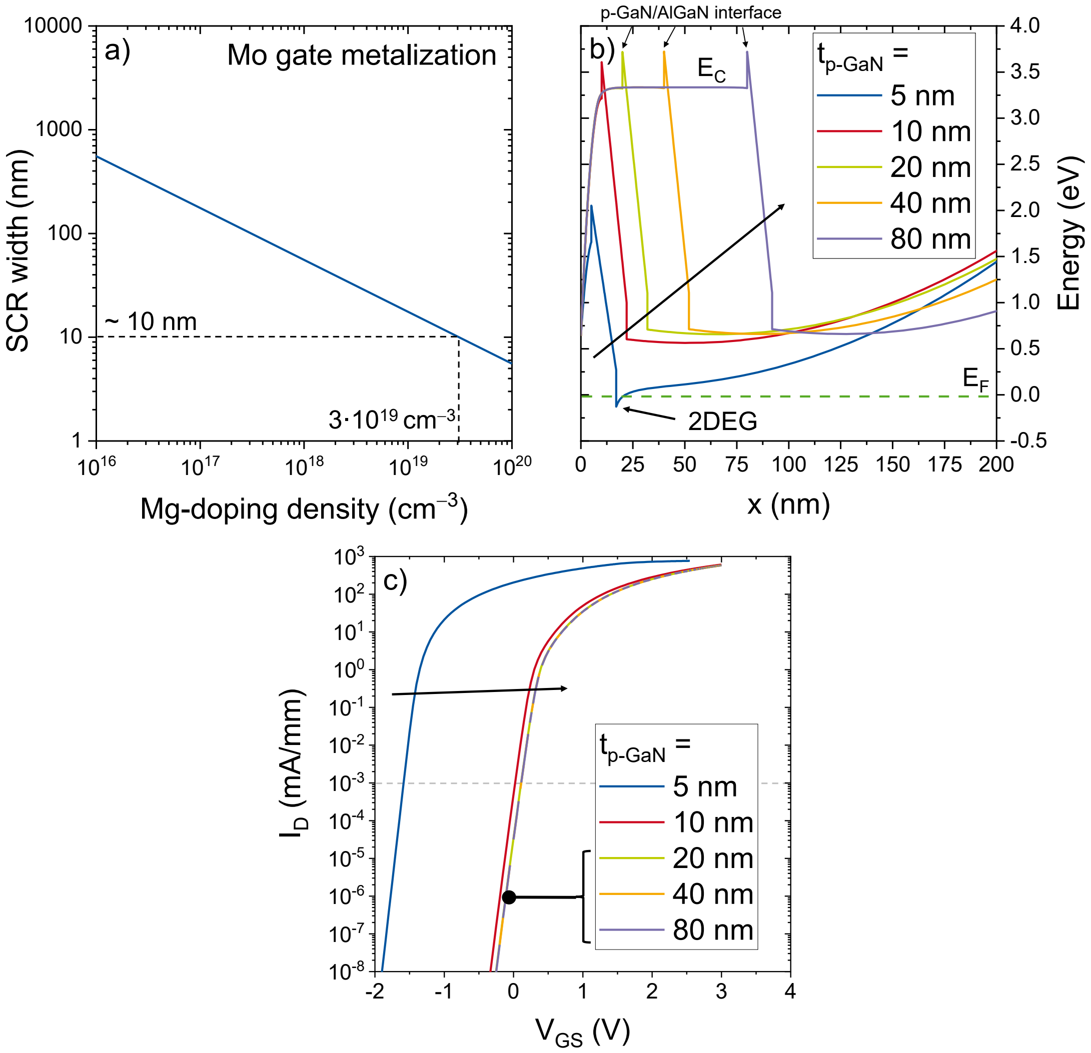


Figure 6.2.: a) Space-charge-region width (SCR) versus Mg-doping density for a Mo gate metallization. b) Simulated conduction band diagrams of p-GaN/AlGaN/GaN heterostructures with different p-GaN thicknesses and a Mg-doping density of $3 \cdot 10^{19}\,\text{cm}^{-3}$. c) Simulated transfer characteristics. Simulations are performed by Sentaurus TCAD [69]. The arrows indicate increasing $t_{\text{p-GaN}}$.

Influence of Mg-doping density

Additionally to defining the minimum p-GaN thickness, the Mg-doping density of the p-GaN layer directly influences V_{th}. Fig 6.3(a) shows calculated $E_{F,p\text{-}GaN}$ values in bulk p-GaN for different doping densities. $E_{F,p\text{-}GaN}$ is slowly decreasing by –0.06 eV per decade Mg-doping density from 0.36 eV at 10^{16} cm^{-3} to 0.11 eV at 10^{20} cm^{-3}. A corresponding conduction band diagram of a p-GaN/AlGaN/GaN heterostructure is depicted in Fig. 6.3(b) with $t_{p\text{-}GaN}$ of 80 nm. For the lowest doping density of 10^{18} cm^{-3}, the SCR reaches the AlGaN barrier and therefore, a negative shift of V_{th} in Fig. 6.3(c) can be observed. For higher doping densities, the SCR is fully developed. The conduction band rises slowly [cf. Fig. 6.3(a)] and V_{th} is shifted from 0.095 V to 0.127 V for 10^{19} cm^{-3} and 10^{20} cm^{-3}, respectively. In conclusion, the lower limit for the p-GaN doping density is given by the SCR width, whereas V_{th} only depends weakly on the doping density above this lower limit.

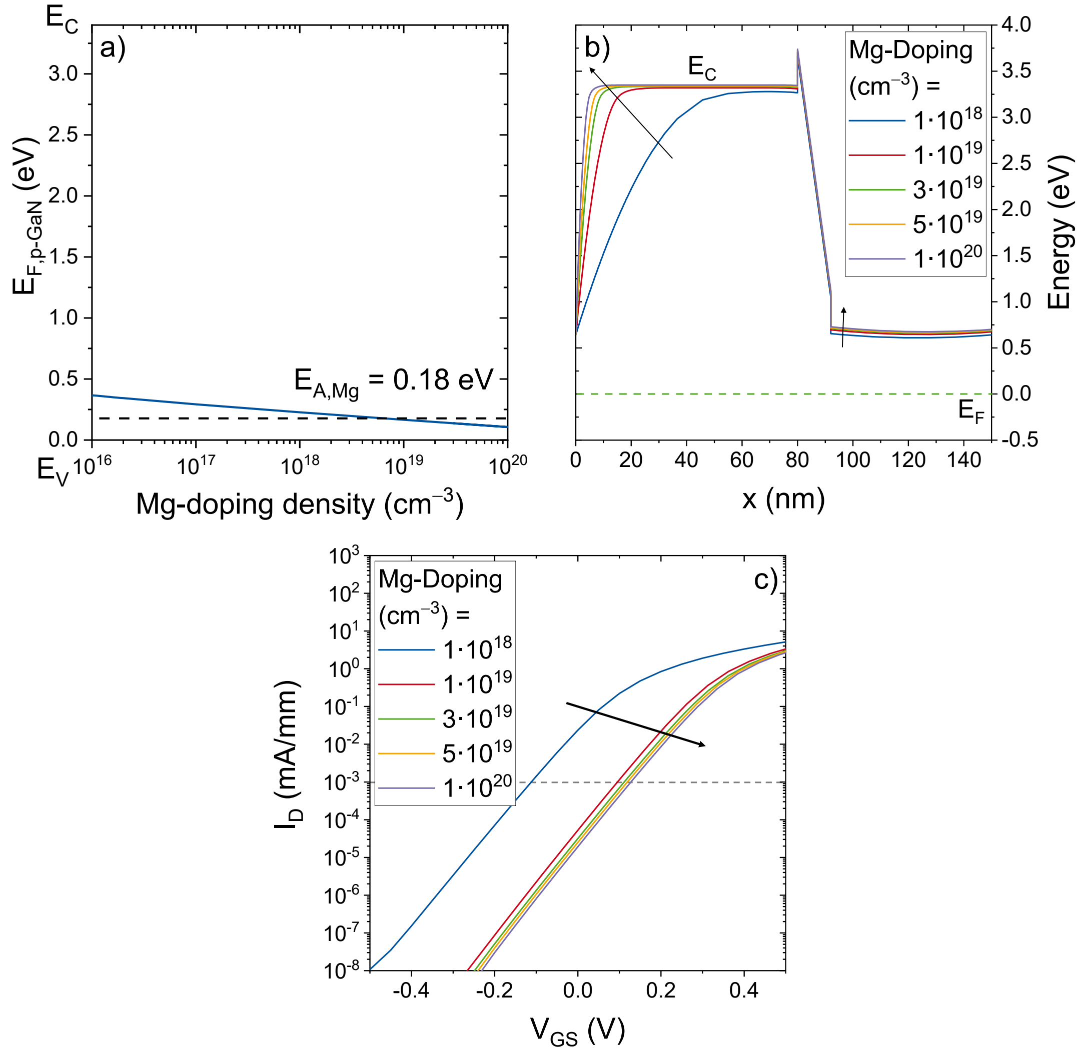


Figure 6.3.: a) Distance from the Fermi level to the valence band edge in Mg-doped bulk p-GaN. b) Conduction band diagram of a p-GaN/AlGaN/GaN heterostructure for different Mg-doping densities and the corresponding simulated transfer characteristics c). Simulations are performed by Sentaurus TCAD [69]. The arrows indicate increasing Mg-doping.

Influence of an undoped GaN layer between p-GaN and AlGaN

During growth of the p-GaN/AlGaN/GaN heterostructure, different growth conditions are employed for each layer. The switch from AlGaN to p-GaN growth conditions is particularly critical. The p-GaN growth should ideally start with a high Mg-doping density at the p-GaN/AlGaN interface, but Mg diffusion into the AlGaN barrier needs to be avoided as it can causes additional leakage at elevated temperatures (shown later) or shift V_{th} [118]. This can be achieved by the growth of a thin undoped GaN layer, which is then doped through Mg diffusion during the subsequent p-GaN growth. But depending on the thickness of this undoped GaN layer, a part of the layer may remain undoped. Therefore, the influence of this thin undoped GaN layer was investigated by simulations with Sentaurus TCAD. A background n-doping of $N_D = 10^{15}\,cm^{-3}$ for this layer was assumed. The results are presented in Fig 6.4. The transfer characteristic in Fig. 6.4(a) shows a negative V_{th} shift with increasing undoped GaN layer thickness $t_{undoped}$. For further evaluation of the V_{th} shift, V_{th} versus $t_{undoped}$ is plotted in Fig. 6.4. The V_{th} of 0.11 V for $t_{undoped} = 0$ nm is shifted to 0.01 V for $t_{undoped} = 20$ nm. This equals an approximated V_{th} shift of –5.5 mV per nm undoped GaN layer.

In conclusion, the p-GaN layer and the undoped GaN layer have only a minor influence on V_{th} as long as the SCR is fully developed. V_{th} is mostly dependent on the design of the AlGaN barrier.

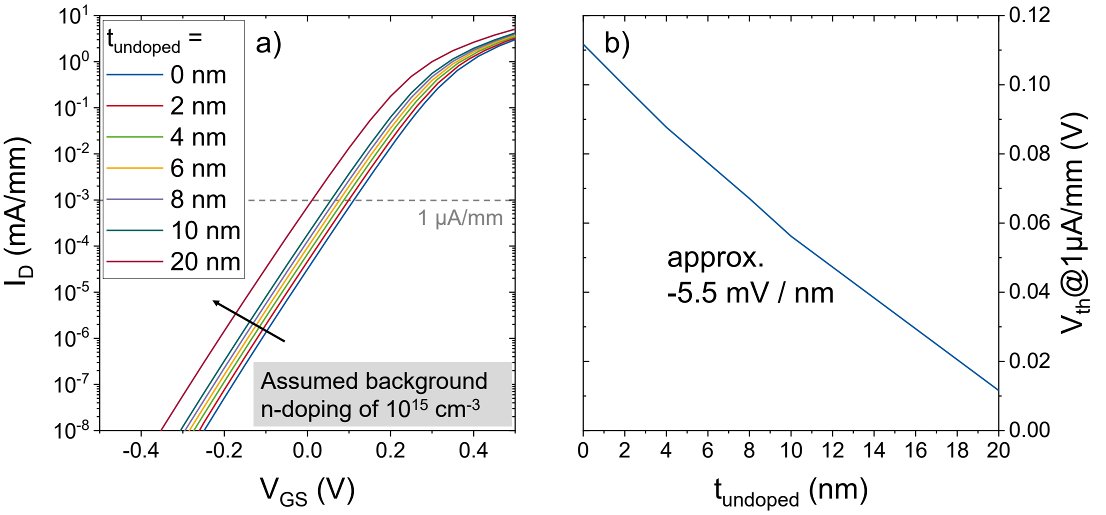


Figure 6.4.: a) Simulated transfer characteristics of a p-GaN-gated HFET with an undoped GaN interlayer between p-GaN and AlGaN. b) V_{th} extracted at 1 µA/mm. Simulations are performed by Sentaurus TCAD [69]. The arrow indicates increasing $t_{undoped}$.

Trade-off between V_{th} and n_s

To achieve high threshold voltages, the polarization (i.e Al content) and thickness of the AlGaN barrier need to be low. In the access regions on the other hand, these parameters should be large to achieve high 2DEG densities and thus, low device ON-resistances. In the p-GaN-gated HFET, the AlGaN barrier has the same thickness and composition throughout the whole wafer. Therefore, the barrier properties of gated areas and access regions are identical and a trade-off between threshold voltage and sheet carrier density in the access regions has to be considered for epitaxy design. The left-side of Fig. 6.5 reflects the gated area of the p-GaN-gated HFET. The minimum p-GaN thickness which is required for the fully developed SCR, i.e. normally-off operation, is visible (indicated by the small arrows for 10 nm and 12,5 nm). For larger AlGaN barrier thicknesses (22.5 nm and 35 nm), a full depletion of the 2DEG is not possible, because the potential drop over the AlGaN barrier is too high. This upper AlGaN thickness limit is significant for the ungated access regions reflected by the right side of Fig. 6.5. From the processing point of view, further thinning of the AlGaN barrier during the p-GaN etching process could lead to a dramatic reduction in the sheet carrier density of the access regions. Due to the thin AlGaN barrier, there is a strong dependence of n_s on the depth of the unintentional AlGaN recess etch [see Fig 2.5(b)]. However, the dependence of n_s on

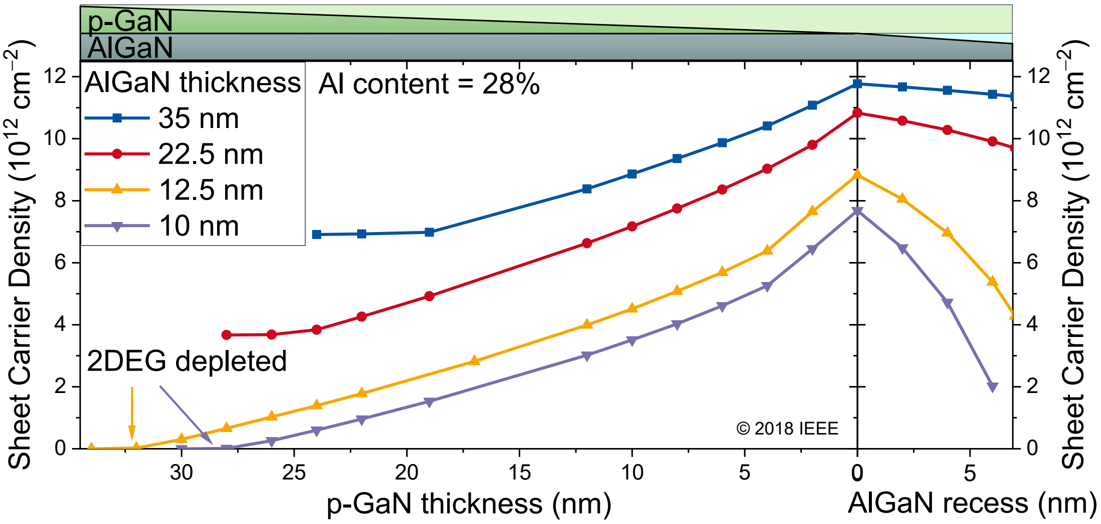


Figure 6.5.: Simulated 2DEG sheet carrier density n_s of a p-GaN/AlGaN/GaN heterostructure with an assumed Al content of 28%. The simulation was performed for different initial AlGaN barrier thicknesses. For 22.5 nm and 35 nm AlGaN thickness, n_s saturates and cannot be depleted by larger p-GaN thicknesses. The right side depicts the impact of an unintentional AlGaN recess during p-GaN removal. Simulations are performed by Sentaurus TCAD [69].

any residual p-GaN is just as strong. Both, 2 nm residual p-GaN or 2 nm recess into the AlGaN barrier already lead to a reduction of the sheet carrier density by approximately 10% (assuming 12.5 nm initial AlGaN thickness). This makes precise etch depth control critical and is achieved by a highly selective dry-etching process as presented next.

6.2. Selective Etching of p-GaN

Completely removing the p-GaN without attacking the underlying AlGaN barrier requires highly selective etch process, i.e. a large etch rate for p-GaN is desired, whereas the etch rate of AlGaN should ideally be zero. Achieving different etch rates for materials is primarily based on chemical reactions in contrast to physical etching by sputtering. Therefore, a dry-etch process in an inductively coupled plasma reactive ion etching (ICP-RIE) tool is preferred, in which the plasma density can be independently controlled through the ICP power. The dry-etching agent of choice for gallium nitride is chlorine, which shows a high etch rate for GaN and, slightly weaker, for AlGaN [120]. Oxygen acts as a retarding agent in the dry-etching process with higher effectiveness for AlGaN compared to GaN [121] and can be used to adjust the selectivity. Another possibility is the use of a fluorine chemistry as retarding agent [122]. For both, a competing process between the passivation of the surface by an oxide/fluoride due to chemical reactions, and etching by sputtering this passivation through ion bombardment and attacking the underlying material is established. These two processes need to be balanced to achieve high selectivity. This type of process was first introduced by Lee et al. in 2000 [123] with a $Cl_2/O_2/Ar$ chemistry leading to a selectivity of 24 and improved by Han et al. [124] with a $Cl_2/O_2/N_2$ chemistry and a selectivity of 60. Particularly the process from Han et al. has seen growing interest recently and shows very good results [117, 125–127].

The chemistry from Han et al. was adopted and RF- and ICP power were tuned down for lower etch rates to gain better control for thin layers. The ICP power was chosen to 600 W and the RF power to 34 W resulting in a DC self-bias of -100 V. The gas flows for $Cl_2/O_2/N_2$ are 30 sccm, 3 sccm, 10 sccm, respectively, at a chamber pressure of 4 Pa. The resulting etch rates were measured to be 19 nm/min for p-GaN and below 1 nm/min for AlGaN leading to a selectivity of at least 19.

This etch process was then evaluated for its suitability in a p-GaN-gated HFET process. Test samples were fabricated from a p-GaN/AlGaN/GaN-on-Si wafer grown by MOCVD with a p-GaN thickness of 80 nm and 12.5 nm AlGaN barrier with 25% Al.

More detailed wafer information can be found in the appendix A.2 (Wafer V). The samples were partially protected by a SiO_x mask, whereas the free surface was etched using the process described above. Four samples were processed with different etch durations of 0 min, 1 min, 3 min and 5 min. After the dry-etching, the SiO_x mask was removed by a wet-chemical treatment with buffered oxide etch (BOE). Characterization was performed by atomic force microscopy (AFM) and SEM. Fig. 6.6 presents the experimental results.

In the first row, AFM images of the sample surface for different etch times are presented. The pristine p-GaN surface has two types of defects. First, small pits, which are homogeneously distributed over the entire surface and second, larger random crack-like defects are visible. The latter becomes smaller as the etch duration is prolonged. The RMS roughness initially increases from 0.55 nm (pristine surface) over 0.85 nm (1 min etched) to 1.3 nm (3 min etched). The second row shows top-view false-colored SEM images (green for p-GaN). Top and bottom half reflect the pristine and etched surface, respectively. In the SEM images, the formation of a well-defined etch edge and the coarse surface for 3 min etch duration is revealed. The third row presents the results for 5 min etch duration (green for p-GaN, dark blue for AlGaN). Upon completely exposing the AlGaN layer, the surface smooths out to 0.65 nm again. Due to the high etch selectivity, the rough morphology of the p-GaN (cf. Fig. 6.6 p-GaN: 3 min) is not transferred to the AlGaN barrier. However, defects in the AlGaN layer are still visible, which are characteristic for the epitaxial material used here. The total height of the etched step was 80 nm visible in the AFM profile of Fig. 6.6. This indicates that despite overetching the barrier by about 1 minute and assuming the nominal thickness of 80 nm to be correct, less than 1 nm was removed from the AlGaN barrier. As a result of this precise etch process, a negligible increase of the access resistance is expected.

6.3. Self-aligned Gate Patterning

In the self-aligned approach, the gate metallization is deposited first in the whole process and is not only used as final metal contact to the p-GaN gate, but also as etch mask during the removal of the p-GaN in the access regions. This avoids the need for an alignment of the gate metallization to the p-GaN ridge. The benefits of self-aligned processes are a reduced number of processing steps and an overall reduction of process complexity. Additionally, an exact alignment between the metallization and the p-GaN ridge area is achieved, ensuring an excellent electrostatic control of the 2DEG channel.

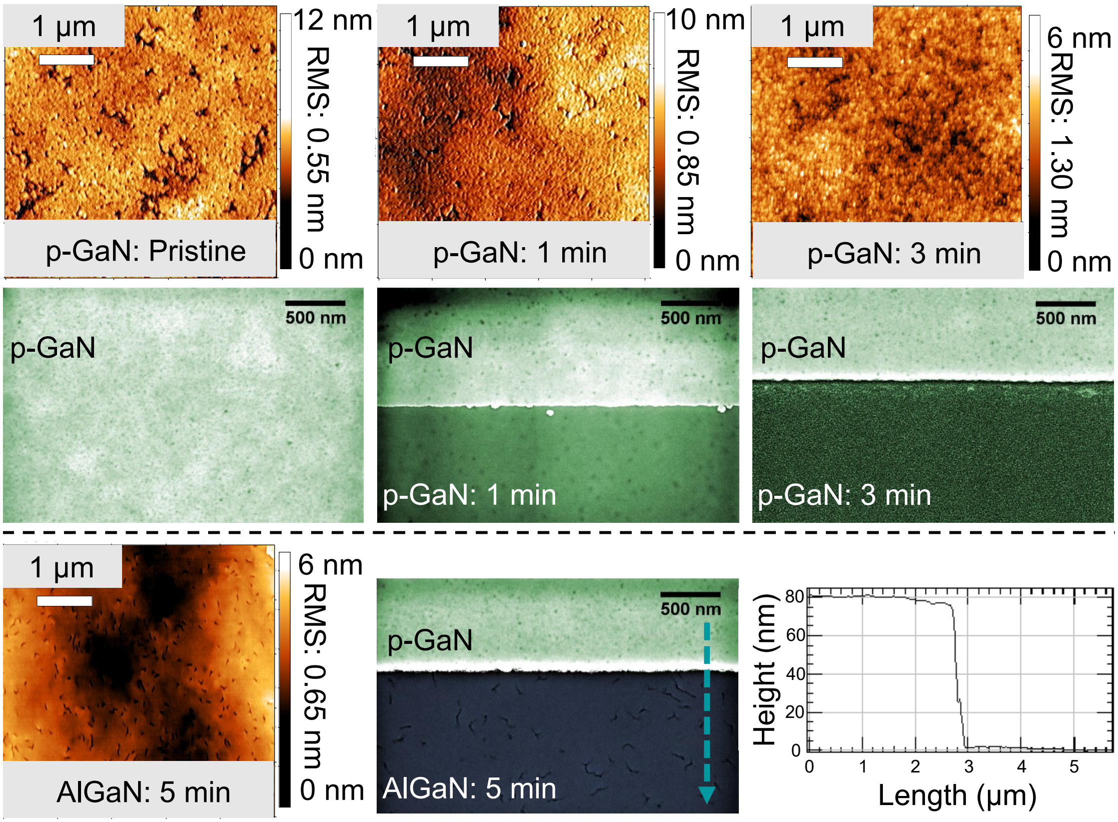

1 µm
12 nm
RMS: 0.55 nm
0 nm
p-GaN: Pristine
1 µm
10 nm
RMS: 0.85 nm
0 nm
p-GaN: 1 min
1 µm
6 nm
RMS: 1.30 nm
0 nm
p-GaN: 3 min
500 nm
p-GaN
500 nm
p-GaN
p-GaN: 1 min
500 nm
p-GaN
p-GaN: 3 min
1 µm
6 nm
RMS: 0.65 nm
0 nm
AlGaN: 5 min
500 nm
p-GaN
AlGaN: 5 min
Height (nm)
80
60
40
20
0
0
1
2
3
4
5
Length (µm)

Figure 6.6.: AFM and SEM images of the pristine and etched p-GaN surfaces for 1 min, 3 min and 5 min etch duration. Additionally, an AFM height profile after 5 min etch duration is shown, for which the measurement direction is indicated by the arrow. Image after [117].

However, the self-aligned gate-first process in combination with selective p-GaN etching introduces particular requirements. Ideally, the gate metal forms a Schottky contact to the p-GaN, thereby reducing gate leakage currents [128]. Schottky contacts to p-type material require low work function metals (e.g Ti, Al, V, ...) which tend to be reactive and easily form nitrides [129]. Particularly, the high-temperature anneal process required for the source and drain contacts might promote reactions between the metallization and p-GaN, degrading the quality of their interface. Consequently, a balance between reactivity and work function has to be considered. Mo has excellent thermal stability [130] and a moderately high work function of 4.6 eV [131]. On the other hand, Mo is highly susceptible to Cl_2/O_2 plasma, which requires a protection of the deposited contact during dry-etching of the p-GaN [132]. Therefore, Ni and SiO_x cap layers as well as AlO_x sidewall spacers are employed as protection during the subsequent dry-etching step. The Ni layer acts as fail-safe for the top encapsulation, since it has a high resistance against chlorine plasma and is often used as hard mask [133]. However, only Ni as top protection is not feasible, since prior experiments have shown that it inhibits the etching of the p-GaN next to the mask.

The encapsulation process is depicted in Fig. 6.7. The SEM images are false-colored for easier identification of the individual layers. Fig. 6.7(a) shows a cross section of the deposited gate stack with the Mo and Ni layers and the SiO_x top encapsulation. All layers were deposited in an electron beam evaporator in one process. The width of the SiO_x cap is gradually decreasing. This is an artifact of the patterning process via evaporation and lift-off, because the size of the resist opening is shrinking due to deposition on the photoresist layer (barely visible in the top right corner). This leads to the two visible edges E1 and E2, which can also be observed in the top view in Fig. 6.7(b). The SiO_x surface shows a homogeneous closed layer with the underlying metal layers visible at the edge. Afterwards, an oxygen plasma cleaning is performed, and 50 nm AlO_x is deposited conformally on the whole sample by PEALD. The AlO_x is then etched anisotropically with a BCl_3/Ar dry-etch process in an ICP-RIE tool. This leads to the formation of the AlO_x sidewall spacers, which are visible in Fig. 6.7(c). The Mo metallization is now encapsulated from all sides against the dry-etching process.

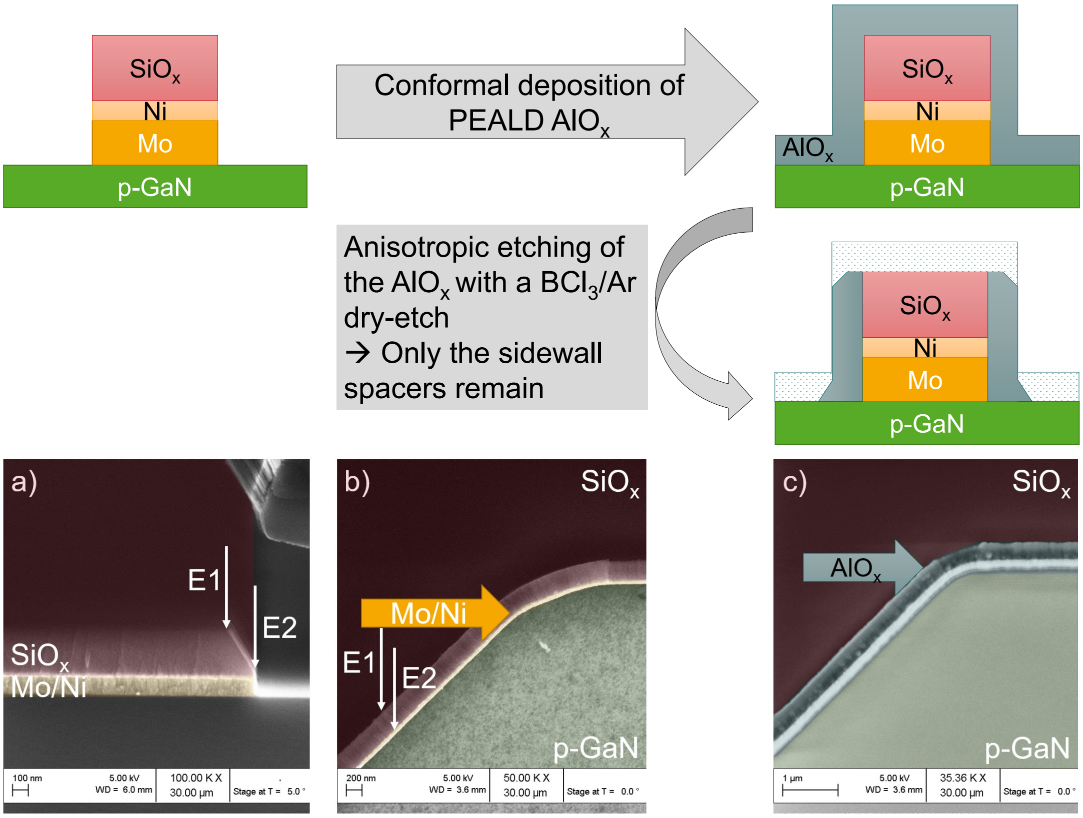

SiOx
Ni
Mo
p-GaN
Conformal deposition of PEALD AlOx
SiOx
Ni
Mo
AlOx
p-GaN
Anisotropic etching of the AlOx with a BCl3/Ar dry-etch
→ Only the sidewall spacers remain
SiOx
Ni
Mo
p-GaN
a)
E1
E2
SiOx
Mo/Ni
100 nm
5.00 kV
WD = 6.0 mm
100.00 K X
30.00 µm
Stage at T = 5.0 °
b)
SiOx
Mo/Ni
E1
E2
p-GaN
200 nm
5.00 kV
WD = 3.6 mm
50.00 K X
30.00 µm
Stage at T = 0.0 °
c)
SiOx
AlOx
p-GaN
1 µm
5.00 kV
WD = 3.6 mm
35.36 K X
30.00 µm
Stage at T = 0.0 °

Figure 6.7.: Schematic overview and false-colored SEM images of the encapsulated gate metallization process. a) Cross section of the deposited gate stack by electron beam evaporation. b) Top view of the metallization edge after lift-off. c) Formation of the AlO_x sidewall spacer.

6.4. Complete Manufacturing Process

The critical steps of selective p-GaN etching and encapsulated self-aligned gate metallization have shown the main processing challenges for p-GaN-gated HFET. In the following, a complete process chain for a p-GaN-gated HFET utilizing these techniques will be presented.

The device is fabricated on a commercial GaN-on-Si wafer grown by MOCVD. The layer stack consists of a carbon-doped GaN buffer with interlayers, a GaN channel, a 12.5 nm AlGaN barrier with an assumed Al content of 28% and a 80 nm Mg-doped GaN layer with a nominal doping density of $3 \cdot 10^{19}\,\text{cm}^{-3}$. The Mg was activated in-situ in N_2 atmosphere. More detailed wafer information can be found in the appendix A.2 (Wafer V).

Different to standard device manufacturing (see appendix A.4), processing is started with the gate stack deposition of 100 nm Mo as gate metallization and 20 nm Ni, 300 nm SiO_x as top encapsulation. The patterning is performed by optical lithography with a

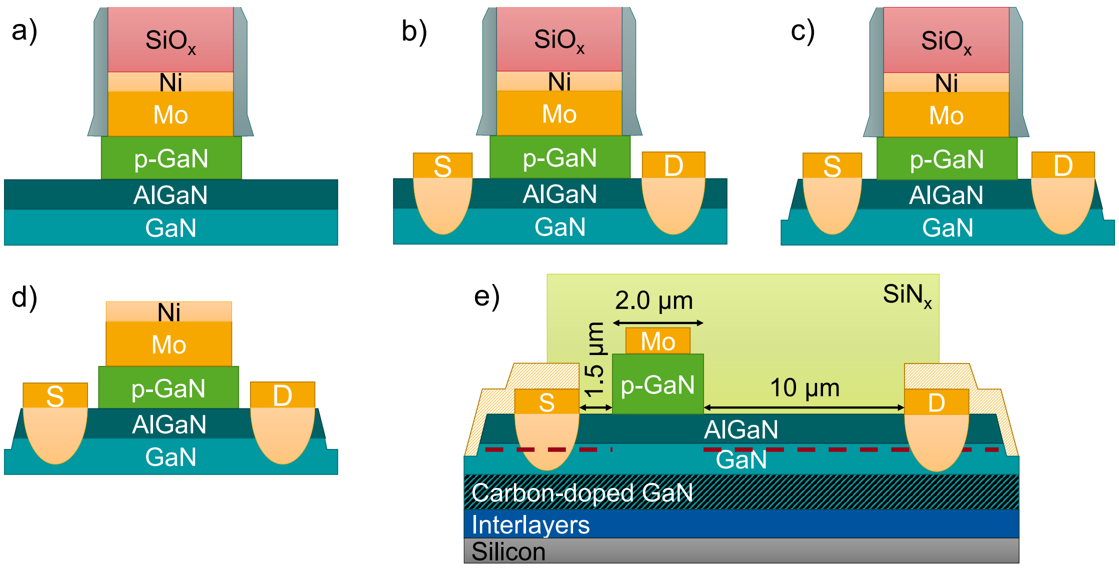


Figure 6.8.: Schematic cross section of the device. Process is shown from left to right starting after the gate module (see Fig 6.7). a) Selective etching of p-GaN. b) Deposition and annealing of source and drain contacts. c) Mesa definition by BCl_3/Ar dry-etching. d) Removal of protective oxides by buffered oxide etch (BOE). e) The device is finished by contact pad deposition and passivation with SiN_x.

thick lift-off resist layer and a positive photoresist. Excess metal and oxide is removed by lift-off afterwards. Next, the AlO_x side wall spacers are formed by deposition and anisotropic dry-etching (see previous section). The gate metallization is completely encapsulated, and the selective removal of the p-GaN outside the gate area is performed by the $Cl_2/O_2/N_2$ dry etch for a duration of 5 min [see section 6.2 and Fig. 6.8(a)]. This leads to the self-aligned gate metallization on top of the p-GaN ridge. Following the gate module, the ohmic contacts and mesa areas are processed [see section A.4 and Fig. 6.8(b)+(c)]. During these steps, the gate metal is still encapsulated, and the protective layers are removed afterwards by buffered oxide etch (BOE) [see Fig. 6.8(d)]. The p-GaN-gated HFET is finished by contact pad deposition and SiN_x passivation [see Fig. 6.8(e)].

In Fig. 6.9(a), a top-view false-colored SEM image of an unpassivated device is shown. The exposed AlGaN surface after the selective dry-etching contains no major defects or roughness. Still, a small residual p-GaN island is visible in the top left corner and some ball-shaped structures on the bottom. Both are most likely originating from minor inhomogeneities of the AlO_x dry etch.

Fig. 6.9(b) shows a cross-sectional false-colored SEM image of the gate (cleaved sample). The interface between the gate metallization and p-GaN appears sharp, showing no signs of metal spiking or surface reactions which may occur due to the high-temperature

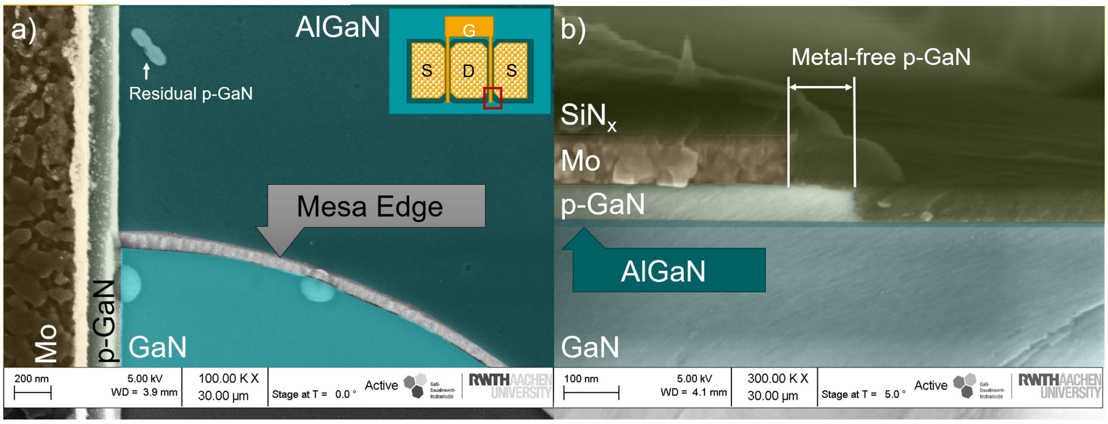

a)
AlGaN
G
S
D
S
Residual p-GaN
Mesa Edge
Mo
p-GaN
GaN
200 nm
5.00 kV
WD = 3.9 mm
100.00 K X
30.00 µm
Stage at T = 0.0 °
Active
RWTH AACHEN UNIVERSITY
b)
Metal-free p-GaN
SiNx
Mo
p-GaN
AlGaN
GaN
100 nm
5.00 kV
WD = 4.1 mm
300.00 K X
30.00 µm
Stage at T = 5.0 °
Active
RWTH AACHEN UNIVERSITY

Figure 6.9.: False-colored top-view SEM images of an unpassivated device next to a gate finger a) and a cross section of gate module of the finished p-GaN-gated HFET b). The inset shows a schematic p-GaN-gated HFET, in which the red square marks the location of the SEM images.

ohmic contact anneal. The AlGaN barrier appears continuous from left to right and is proof of a precise etch depth control of the p-GaN. Due to the thin AlO_x sidewall spacer during etching, the metal-free p-GaN length is minimized to approximately 70 nm. It appears enlarged to 100 nm in the SEM image due to the perspective. The remaining difference of 20 nm to the deposition thickness of 50 nm AlO_x results from the ICP-RIE etch process, which was not optimized for a perfectly anisotropic etch profile. This leads to a thicker base of the sidewall spacers which is removed first and only a fraction of the total etch duration can attack the p-GaN below (supported by the small step in the p-GaN is visible at the outer edge). The electrical results of the finished devices are discussed in the next section.

6.5. High-Voltage Device

The epitaxial material used for the p-GaN-gated HFET here presented was designed for a low ON-resistance and high operation voltages. A second series aimed at higher threshold voltages will be presented afterwards. For the characterization of the device properties, Hall and van-der-Pauw as well as DC- and pulsed I-V measurements were performed.

To investigate the influence of plasma etching on the transport properties of the 2DEG, the etched access regions and the unetched gated areas were analyzed. Additionally, the Hall- and van-der-Pauw measurements were performed before and after device passivation to investigate the influence of the SiN_x on the access regions. The results for the access regions are shown in Fig. 6.10(a). The passivation improves the mobility

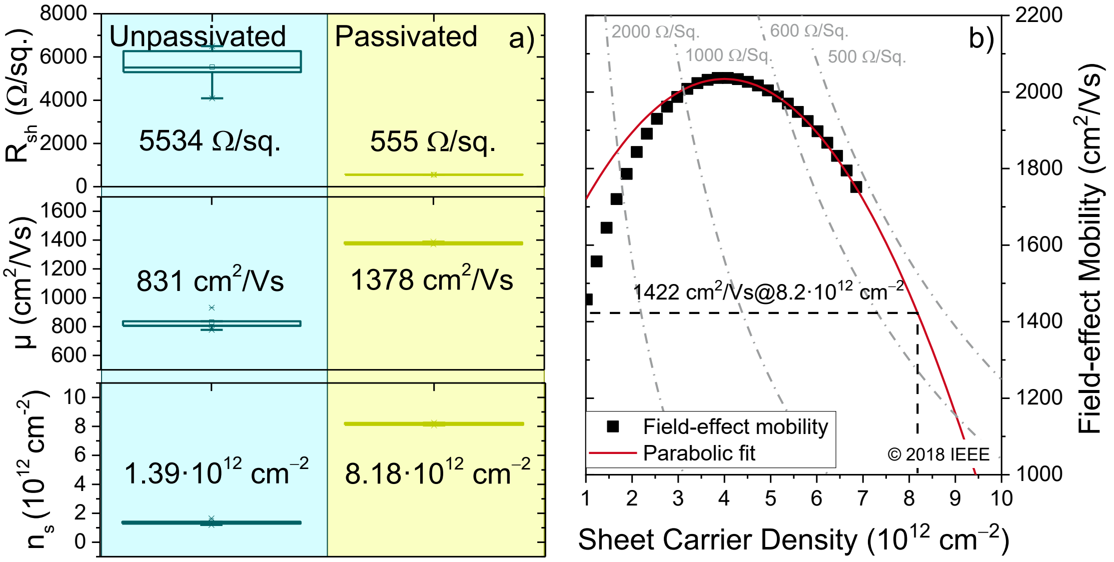


Figure 6.10.: Hall and van-der-Pauw measurements of etched structures (similar to the device access regions) with and without passivation a) as well as extracted field-effect mobilities for the p-GaN-gated areas b) [117].

μ from 831 cm^2/Vs to 1378 cm^2/Vs and the sheet carrier density from $1.39 \cdot 10^{12}$ cm^{-2} to $8.18 \cdot 10^{12}$ cm^{-2} resulting in an improvement of the sheet resistance from 5534 Ω/sq. to 555 Ω/sq. The higher mobility is most likely caused by the larger sheet carrier density which reduces ionized donor scattering through screening effects [42] and the avoidance of surface scattering due to the higher separation between surface and 2DEG. For the evaluation of the measured electron density, the complete epitaxial stack without the p-GaN layer was simulated. The simulation predicts an n_s of $7.13 \cdot 10^{12}$ cm^{-2} in the ideal case, which is much higher than the results in the unpassivated case but slightly lower than the passivated structure. These results show a severe depletion of the 2DEG by the unpassivated surface on the one hand, and the 2DEG enhancement effect of SiN_x described in section 2.6.2 on the other hand. In conclusion, the SiN_x passivation is crucial for proper device performance since it strongly reduces the sheet resistance of the access regions.

A direct comparison of the presented Hall and van-der-Pauw data to the unetched gated areas is not possible due to the normally-off nature of the latter. To experimentally investigate the transport properties of the 2DEG in gated areas, field-effect mobilities were extracted from I-V and C-V characteristics of the FATFET devices [see Eq. (5.2)].

Fig. 6.10(b) shows the extracted values of field-effect mobilities (squares) and a parabolic fit (solid line) used for extrapolation. This fit was chosen, because the mobility for high sheet carrier densities is limited by interface roughness scattering ($\propto n_s^{-2}$, see section 2.4). A maximum mobility of 2034 cm^2/Vs is obtained at $4.1 \cdot 10^{12}\,cm^{-2}$. Due to the lack of an AlN spacer [134], which promotes interface roughness scattering, the mobility peaks at relatively low n_s. For $n_s = 8.2 \cdot 10^{12}\,cm^{-2}$, corresponding to the etched structures, an extrapolated mobility of 1422 cm^2/Vs is estimated, which is in good agreement with the experimental data determined by Hall measurements. The comparable mobility between p-GaN-gated and etched access regions and the high n_s indicate only minor damage to the AlGaN surface during p-GaN removal.

Processed p-GaN-gated HFET were characterized by means of DC and pulsed I-V measurements to show their capabilities as high-voltage devices. The discussed devices have a gate length of $L_G = 2.0\,\mu m$, a gate-source distance of $L_{GS} = 1.5\,\mu m$, a gate-drain distance of $L_{GD} = 10\,\mu m$ and a gate width of $W_G = 2 \cdot 50\,\mu m$. Fig. 6.11 shows the transfer characteristics in semilogarithmic a) and linear scale b). A threshold voltage $V_{th} = 1.08\,V$ is extracted from linear extrapolation which is stable over subsequent measurement cycles and does not suffer from an initial V_{th} shift in contrast to the MISHFET or MIS-hybrid HFET. A saturation current of $I_{D,max} = 554$ mA/mm at $V_{GS} = 6\,V$, $V_{DS} = 10\,V$ is achieved, while $I_G = 9$ mA/mm. The maximum transconductance $g_{m,max} = 150$ mS/mm is reached at $V_{GS} = 2.3\,V$. The semilogarithmic transfer plot in Fig. 6.11(a) confirms sharp pinch-off of the 2DEG channel at 0.1 V ($I_D < 1$ nA/mm) showing an ON/OFF-ratio of 10^8. A threshold voltage of 0.4 V is extracted at $I_D = 1\,\mu A/mm$. The calculated V_{th} by employing Eq. (6.1) equals 0.59 V, which is in the proximity of the extracted value. A nearly-ideal sub-threshold swing of SS = 75 mV/dec is estimated, which is particularly low compared to literature values (200 mV/dec [135], 120 mV/dec [136]). High $I_{D,max}$, $g_{m,max}$ and low SS show the excellent channel control due to the self-aligned gate process.

However, the gate leakage current is rather high in comparison to literature values [135]. This might be caused by current injection from the gate into the SiN_x passivation between gate and source. Another possibility is a leakage current along the mesa edge of the device, which could be avoided by using an implant isolation technique instead of dry-etching. Fig. 6.12 shows a comparison of area-normalized diode characteristics of different devices. The contacts for the large-area diode (LAD) and FATFET are located completely on top of the mesa, therefore they are not connected to the mesa edge. The contact pads of the gate diode, on the other hand, protrude over the mesa (see section A.4) and allow for leakage current over the mesa edge.

For the area normalization of the gate diode, two cases have to be considered. Commonly, the area only consists of the gate fingers on top of the mesa, because the additional metal is located on the insulating buffer. However, in the case of the presented

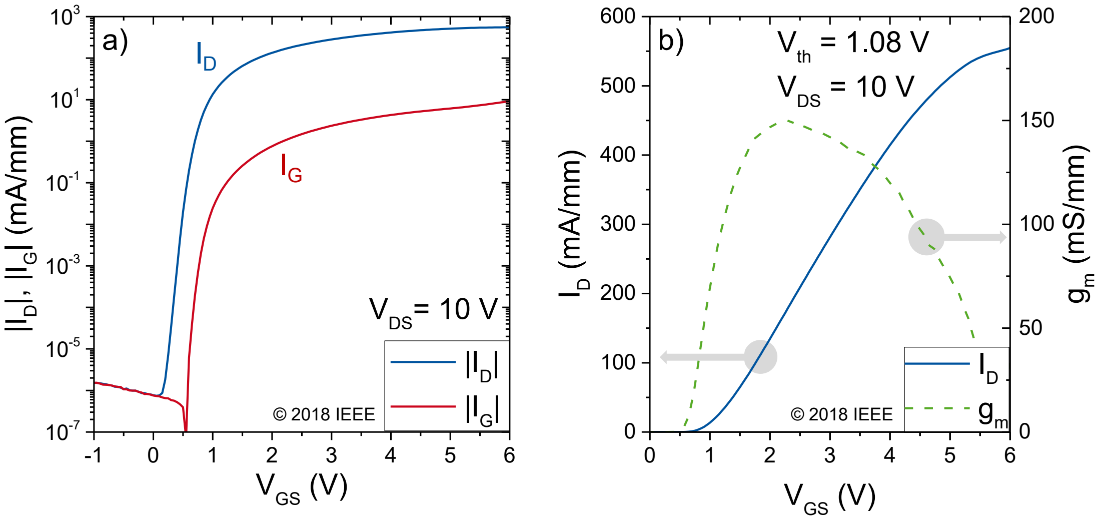
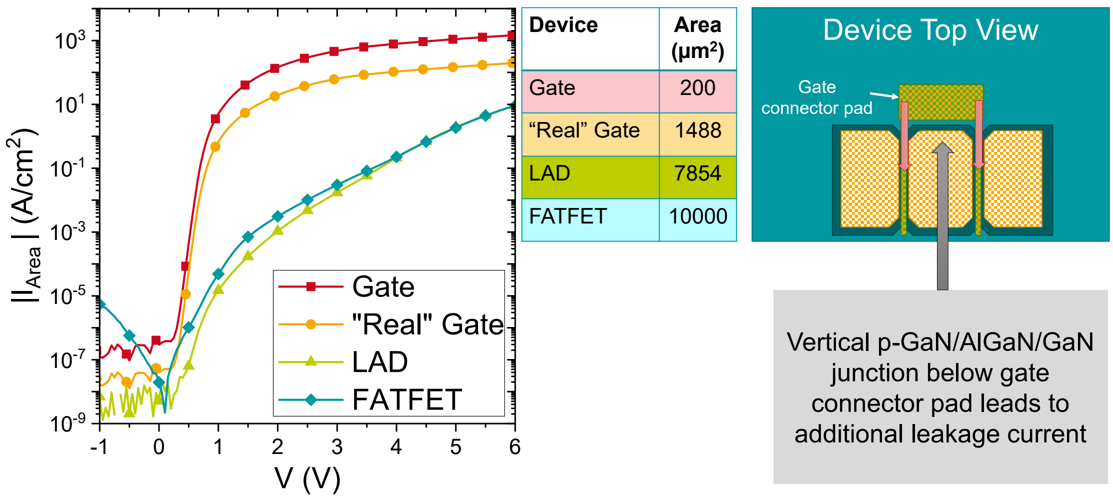


Figure 6.11.: Transfer characteristics of the p-GaN-gated HFET at $V_{DS} = 10$ V in semilogarithmic a) and linear scale b). Blue solid line: I_D. Green dashed line: g_m. Red solid line: I_G.

gate-first process, the gate finger tips and the connector pad, which are also defined in the gate module, are located on top of the p-GaN/AlGaN/GaN junction. This junction becomes conductive under gate forward bias, which adds additional leakage current (see right side of Fig. 6.12). Therefore, two different area normalizations are shown in Fig. 6.12: the gate curve, which considers only the gate fingers, and the "real" gate, which considers the whole area.

The high current of the gate diode does not scale to large devices and is higher than the FATFET or LAD for $V > 0.5$ V even with the "real" normalization. Thus, the leakage current is most likely not directly related to the vertical p-GaN/AlGaN/GaN junction, but to the mesa edge or passivation.

To analyze the dynamic performance, pulsed measurements under high OFF-state bias stress were performed. The device was stressed at $V_{GS,quiet} = 0$ V, $V_{DS,quiet}$ = 0 V …200 V in 50 V steps for 1 s and measured at $V_{GS} = 4$ V, $V_{DS} = 0$ V… 10 V for 5 ms. The results are presented in Fig. 6.13. The unstressed I-V curve ($V_{DS,quiet} = 0$ V) peaks at 418 mA/mm and shows a negative output conductance beyond the knee voltage of $V_{DS} = 6.5$ V. This is due to the fairly long measurement pulse length of 5 ms, which causes self-heating of the device (as is also evident by the similar characteristic of the DC curve). As the stress bias rises, charge trapping occurs at the SiN_x/AlGaN interface and inside the GaN buffer [115], which results in an increased ON-resistance and a reduced ON-current. The ON-resistance of the unstressed device is extracted at $I_D = 100$ mA/mm to $R_{ON} = 10.7$ Ωmm. Fig. 6.13(b) presents the R_{ON} evolution with in-



Device	Area (µm²)
Gate	200
“Real” Gate	1488
LAD	7854
FATFET	10000

Vertical p-GaN/AlGaN/GaN junction below gate connector pad leads to additional leakage current

Figure 6.12.: Area-normalized leakage current of Schottky gate diodes for the gate diode (area of 200 µm²), a large-area diode (area of 7854 µm²) and a FATFET (area of 10000 µm²). The common normalization to the gate fingers on top of the mesa is not valid for the presented p-GaN-gated HFET since the gate connector pad is located on top of conductive material which is explained on the right side of the figure. Therefore, the gate diode normalized to the whole metallization area is also shown as "real" gate diode (area of 1488 µm²).

creasing OFF-state stress. An R_{ON} increase of 45% for the highest stress bias can be observed, which leads to $R_{ON,200\,V} = 15.5\,\Omega$mm. Given that the device has no field plates and is processed on a heavily carbon-doped GaN buffer, this observed increase is quite small [115]. Unpassivated devices with a similar p-GaN etching process can have a dynamic R_{ON} increase by a factor of 120 or, in the case of an AlO_x passivation, a factor of 20 [125]. Another passivated p-GaN gated HFET presented in [137] with a double source field-plate shows an dynamic R_{ON} increase by the factor of 1.85. The low R_{ON} increase with $V_{DS,quiet}$ can be attributed to a small trap density at the SiN_x/AlGaN interface, which again suggests a low-damage etching process. The dynamic R_{ON} could be improved further by employing a state-of-the-art triple field plate, an optimized buffer with AlGaN back barrier or a hybrid p-GaN drain [23, 138–140], which can completely suppress the dynamic R_{ON} increase up to a maximum $V_{DS,quiet} = 850$ V [23].

The high-voltage capabilities were characterized by three-terminal and vertical breakdown measurements with a grounded substrate and are shown in Fig. 6.14. The device was kept in OFF-state at $V_{GS} = 0$ V while increasing V_{DS}. Breakdown voltages of 560 V at 1 µA/mm and 788 V at 1 mA/mm were obtained. Since I_G (red) increases only slightly despite the rising drain current (blue), the breakdown voltages are limited by the buffer. The vertical breakdown measurement taken from another sample with the same epi-

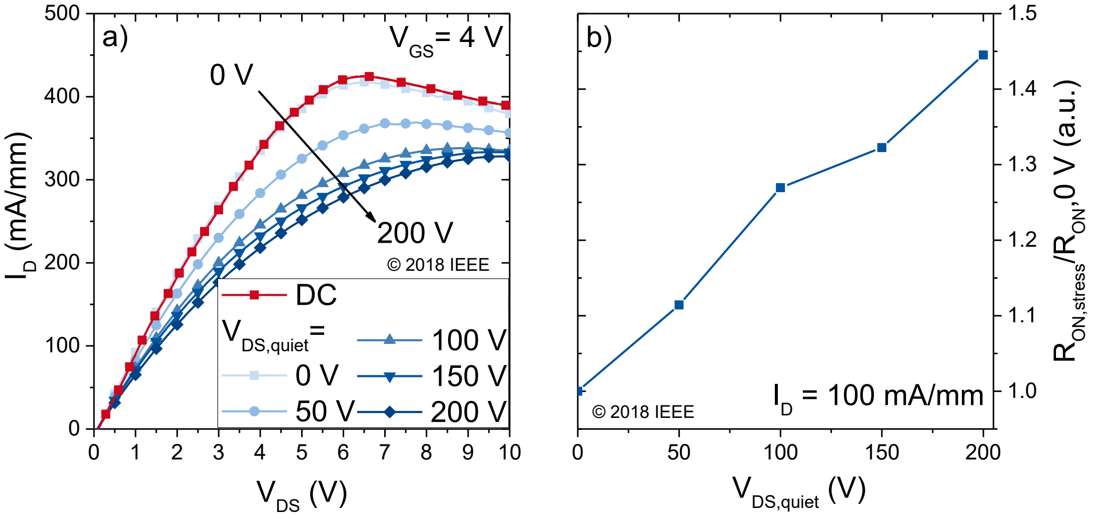


Figure 6.13.: (a) Pulsed (5 ms ON-state) output characteristics measured at $V_{GS} = 4$ V from variable OFF-state (1 s) stress biases. OFF-state was set to $V_{GS,quiet} = 0$ V and $V_{DS,quiet}$ from 0 V to 200 V. The DC measurement shows the same characteristic as 0 V stress-bias showing the self-heating. (b) Dynamic R_{ON} evolution extracted for $I_D = 100$ mA/mm^{-1} under different stress biases $V_{DS,quiet}$.

taxial stack reveals a similar I-V characteristic (green), therefore the limitation is most likely originating from vertical buffer leakage.

6.5.1. Elevated-Temperature Operation

In power electronic systems based on silicon, the operation temperature is currently limited to a maximum of 125 °C due to intrinsic carrier generation [141]. For group III nitride devices, the large bandgap suppresses intrinsic carrier generation and higher operation temperatures up to 1000 °C are possible [142, 143]. Possible applications for high temperature electronics can be found in the automotive sector, in aircrafts (jet engine), for deep/oil gas extraction or space exploration [141]. The most promising topology for normally-off operation at high temperatures is the p-GaN-gated HFET. The gate dielectric of the MIS-hybrid HFET or MISHFET makes their employment challenging, since the dielectric typically suffers from reliability issues at elevated temperatures [144]. Furthermore, emission processes of the interface traps exhibit an exponential temperature dependence (see section 4.2), which can lead to increased V_{th} instabilities [145]. In this section, the suitability of p-GaN-gated HFET for high-temperature operation will be analyzed and later, temperature limitations of the current device design and possible solutions will be discussed.

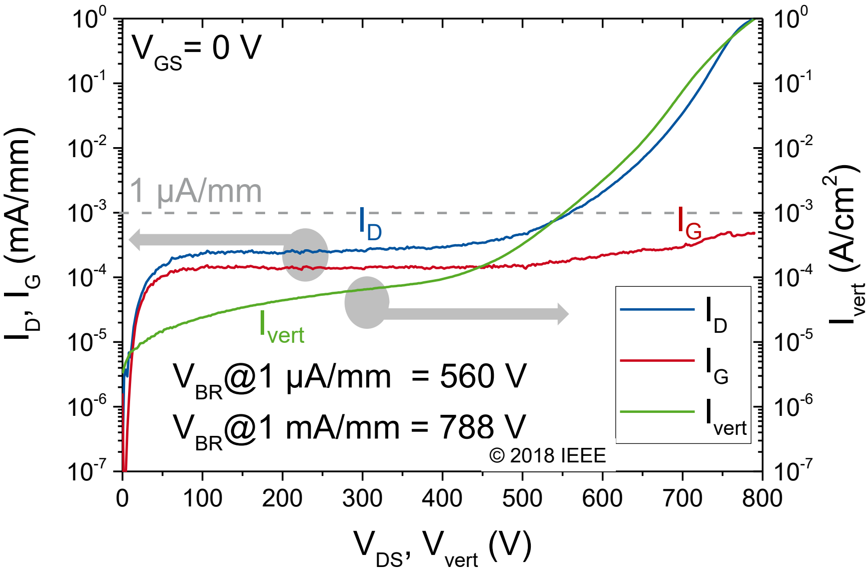


Figure 6.14.: Three-terminal and vertical breakdown measurements. For the three-terminal breakdown, the device was kept in OFF-state at $V_{GS} = 0\,V$ while V_{DS} was increased until I_D=1 mA/mm. For the vertical breakdown, V_{vert} was increased until $I_{vert} = 1$ A/cm^2. The vertical-breakdown measurement was performed on another sample with the same epitaxial stack.

Higher operation temperatures have an impact on different device properties. As described in section 2.4, the electron mobility has a negative exponential temperature dependence due to optical phonon scattering. Therefore, lower ON-currents at higher temperatures are expected. Furthermore, the contact resistance will decrease for the Schottky contact, which primarily leads to an increased gate leakage current. The Mg acceptors of the p-GaN gate have a high activation energy of 135-192 meV [146, 147] leading to temperature-dependent ionization. Thus, the conductivity of the p-GaN gate increases at higher temperatures under the assumption, that the hole mobility is reduced by a factor smaller than the ionization. This would further increases the gate leakage current. Theoretically, the higher ionization should also lead to V_{th} shift to more positive voltages, but this effect is negligible (see section 6.1). Another temperature-dependent property is the buffer leakage, which increases at higher temperatures [148]. In conclusion, during high temperature operation, the ON-current is reduced by the declining carrier mobility, while the OFF-current is increased by gate and buffer leakage currents.

To investigate the high temperature behavior of the presented p-GaN-gated HFET, DC characterization at elevated temperatures was performed. The results of the measured transfer characteristics are shown in Fig. 6.15. The sweeps were performed from 6 V to –2 V and back for temperatures ranging from room temperature (RT) up to 500 °C under

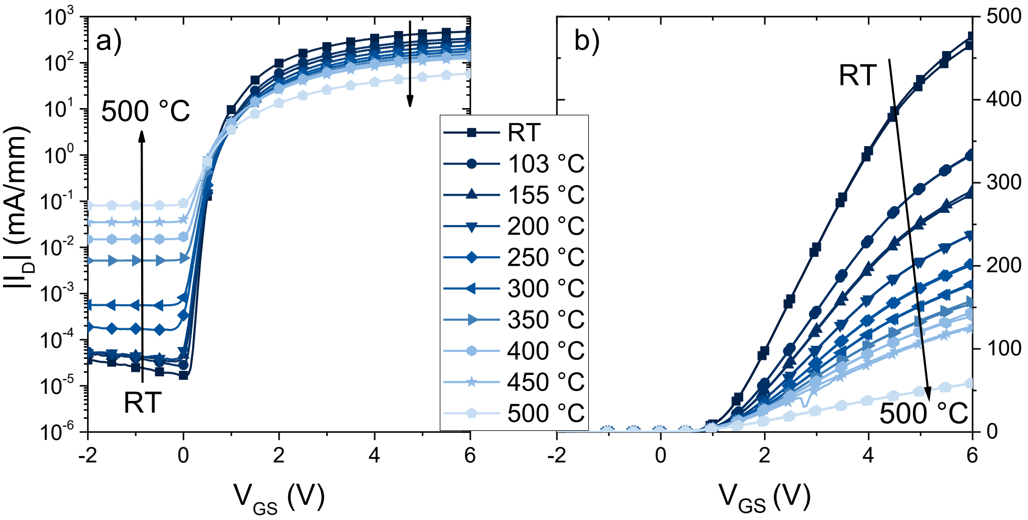


Figure 6.15.: Transfer measurement of a p-GaN-gated HFET up to a temperature of 500 °C. The sweeps were performed from 6 V to -2 V and back. a) The semilogarithmic transfer curve shows a stable OFF-current at V_{GS} = -2 V up to 200 °C and rises towards 500 °C. The ON-current at V_{GS} = 6 V is declining. b) Linear transfer curves from V_{GS} = 6 V to -2 V and back. The to- and back-sweep show no hysteresis.

vacuum. The device type is an HFET with $L_{GS}/L_G/L_{GD}/L_{DS}/W_G$ of 2 / 2.5 / 2.5 / 7.0 / $2{\cdot}50$ µm, respectively. First, the general measurement results of semilogarithmic transfer and input characteristics are presented. Afterwards, the results of both measurements are summarized and discussed together.

Fig. 6.15(a) shows the semilogarithmic transfer curves. At room temperature, the OFF-current at zero bias starts at $1.7 \cdot 10^{-5}$ mA/mm and increases slightly to $5.8 \cdot 10^{-5}$ mA/mm at 200 °C. For higher temperatures, a stronger increase in OFF-current up to $9.0 \cdot 10^{-1}$ mA/mm at 500 °C can be observed. While the OFF-current has a positive temperature coefficient, the ON-current is decreasing with temperature. The current at V_{GS} = 6 V reaches 477 mA/mm at room temperature and declines monotonically down to 127 mA/mm at 450 °C, whereas the last temperature step has a higher relative reduction to 58 mA/mm. The ON-current declines by a total of 88%. The ON/OFF-ratio at room temperature of 10^7 is reduced to 10^3 at 500 °C.

The threshold voltage V_{th} extracted I_D = 1 mA/mm equals 0.65 V at room temperature and stays within the range of 0.53 V to 0.72 V throughout the different temperatures without a clear trend. In Fig. 6.15(b), the transfer curves in linear scale from 6 V to -2 V and back are shown. No V_{th} hysteresis is visible indicating a stable behavior even for high temperatures.

Fig. 6.16(a) shows a semilogarithmic plot of the corresponding input characteristic.

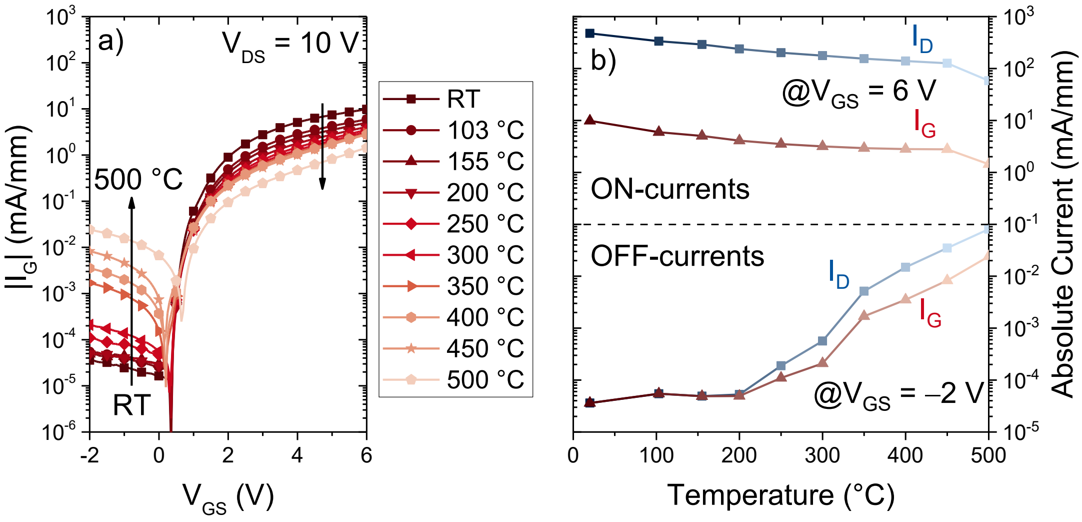


Figure 6.16.: a) Semilogarithmic input characteristic. b) Drain and gate current extracted at V_{GS} = -2 and 6 V versus temperature.

The curves have a profile similar to that of the transfer curves with a stable OFF-current at V_{GS} = -2 V of approximately $4.0 \cdot 10^{-5}$ mA/mm up to 200 °C. Beyond, a stronger rise in the current can be observed up to 500 °C, but weaker than for the drain current. The decline in forward gate current at V_{GS} = 6 V follows exactly the same trend as the drain current with a constant offset to lower current values starting from $9.8 \cdot 10^{-1}$ mA/mm to $1.4 \cdot 10^{-1}$ mA/mm. The forward gate current declines by a total of 86%, which is approximately the same as the 88% of the drain current.

The results from the temperature-dependent I-V characterization are summarized in Fig. 6.16(b), which shows the gate and drain current at V_{GS} = –2 V (OFF-currents) and 6 V (ON-current) plotted against temperature. The steady decline of the ON-current over temperature is originating from the reduced electron mobility for increasing temperatures. The steeper step from 450 °C to 500 °C is resulting from a softening of the Au contact pads. At this temperature, the contact pads start to peel off the semiconductor surface and are distorted, which leads to a higher series resistances. This effect also limits the temperature to 500 °C for the measurement and the overall device operation.

The OFF-current has the same values for drain and gate current up to 200 °C. In this range, the OFF-current is most likely dominated by leakage current over the SiN_x passivation [see Fig. 6.17(1)], which is indicated by its V_{GS} dependence. Unpassivated devices have an OFF-current of approximately 10^{-7} mA/mm at room temperature (not shown here), which is two order of magnitude smaller than for passivated devices. Therefore, the thermal activation of other leakage current paths may be hidden by the

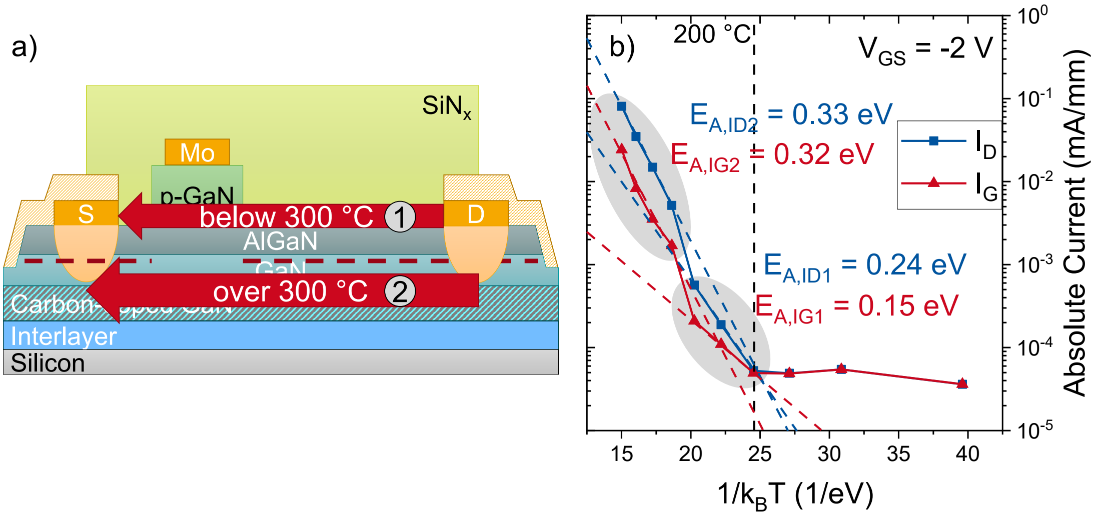


Figure 6.17.: Schematic of the device with the dominant leakage paths a) and an Arrhenius plot of the device OFF-currents b) at V_{GS} = -2 V. (1) Leakage path over the SiN$_x$/AlGaN interface and Mg atoms diffused into the AlGaN barrier dominant up to 300 °C. (2) Buffer leakage related to transport through the carbon-doped buffer at elevated temperatures over 300 °C.

dominant passivation leakage. For temperatures higher than 300 °C, the current rises in a similar way for the drain and gate current, whereas the gate current always exhibits a lower value. While the gate current is still dependent on V_{GS} above 300 °C [see Fig. 6.16(a)], the drain current now shows a constant current value below $V_{GS} = 0$ V for each respective temperature [see Fig. 6.15(a)]. Thus, the device OFF-current is no longer limited by the gate current and the buffer leakage current becomes dominant [see Fig. 6.17(2)].

An Arrhenius plot is used to analyze the activation energies of the thermal effects and is shown in Fig. 6.17(b). Activation energies of 0.24 eV and 0.15 eV in the 200 °C-300 °C range and of 0.33 eV and 0.32 eV in the 300 °C-500 °C are extracted for the drain- and gate current, respectively. While the energy levels for the higher temperature range ($E_{A,ID2}$ and $E_{A,IG2}$) can be correlated with a thermally activated transport process inside the carbon-doped GaN buffer [115], the energy levels in the lower temperature range ($E_{A,ID1}$ and $E_{A,IG1}$) are most likely linked to Mg acceptors. $E_{A,IG1}$ of 0.15 eV for the gate current corresponds to the Mg-acceptor activation energy between 0.135 eV and 0.192 eV in GaN [146, 147], while $E_{A,ID1}$ of 0.24 eV can be related to the activation energy of Mg in AlGaN [149]. Therefore, a small amount of Mg may have been diffused into the AlGaN barrier during growth.

In conclusion, the normally-off concept of a p-GaN-gated HFET has proven its suitability for high temperature applications. The main challenges are the buffer leakage current and leakage currents regarding the PECVD SiN_x passivation, as well as softening of the Au-capped contacts at higher temperatures. The analysis of the activation energies has indicated a possible charge transport over carbon dopants inside the buffer. This can be avoided employing an insulating AlGaN/GaN/AlGaN double heterostructure (AlGaN back barrier) [116] instead of a carbon doped buffer. To further minimize the leakage current, only a thin GaN buffer could be employed to reduce the semiconductor volume which conducts the current [150]. The PECVD SiN_x passivation, which is deposited at 350 °C, can be exchanged with a more robust SiN_x deposited by LPCVD at 700 °C [65]. LPCVD SiN_x commonly shows better insulating properties and the higher deposition temperature increases the durability under high temperature operation. The remaining issue is an Au-free high temperature ohmic contact. The metals, which are forming the actual contact, Ti/Al, have proven to be temperature-stable [151]. The Ni/Au-capping layer could be exchanged with a platinum cap layer [152] or a tungsten cap layer [153], which have much higher melting points than gold (1064 °C) of 1768 °C and 3422 °C, respectively. The gate metallization of the presented process already consists of the refractory metal Mo, which has a high melting point of 2623 °C.

6.6. Increased-Threshold-Voltage Device

The electrostatics presented at the beginning of this chapter show that V_{th} of p-GaN-gated HFET is primarily defined by the thickness and composition of the AlGaN barrier. To achieve higher threshold voltages, the epitaxial layer design was adjusted, and a second set of p-GaN-gated HFET was processed. The aluminum content of the barrier was reduced to 24% and its nominal thickness to 11 nm, whereas the p-GaN thickness was set to 60 nm without changing the doping level of $3 \cdot 10^{19}\,\mathrm{cm}^{-3}$. More detailed wafer information can be found in the appendix A.2 (Wafer VI). Calculating the threshold voltage from Eq. (6.1) leads to $V_{th} = 1.33\,\mathrm{V}$ for this device. Furthermore, the GaN buffer lacks a carbon-doped buffer, and thus has no high voltage capabilities. For verification of the epitaxial layer stack stack, transmission electron microscope (TEM) images were prepared, which are presented in Fig. 6.18. The left image a) shows the complete stack, starting with the silicon substrate on the left, AlN nucleation, AlGaN staircase for strain relief, GaN buffer, AlGaN barrier and p-GaN cap layer. Fig. 6.18(b) is a zoomed-in image of the area indicated by the white square in the left image. The GaN buffer is shown on the left, followed by the AlGaN barrier and the p-GaN cap layer. The image reveals

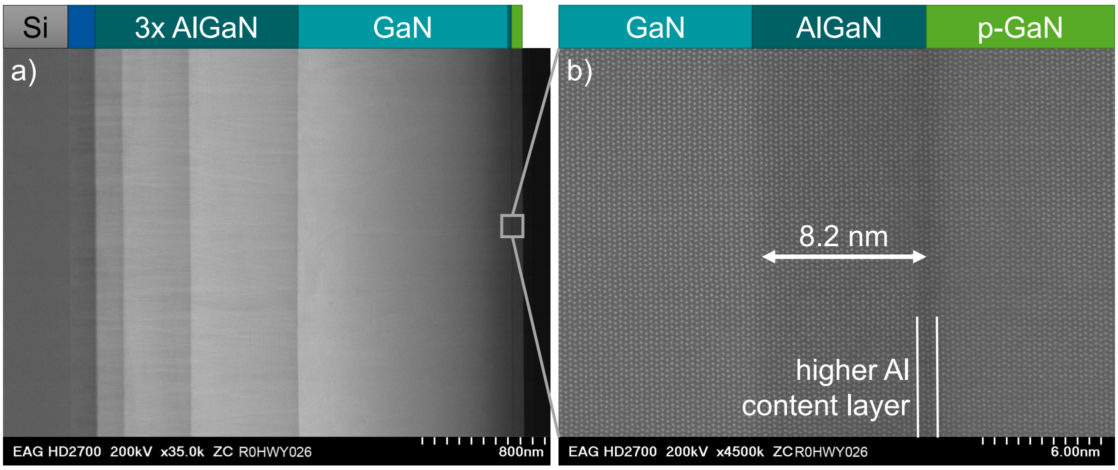


Figure 6.18.: TEM image of the complete epitaxy stack a) starting from the silicon substrate on the left, AlN nucleation, triple AlGaN staircase for strain relief, the GaN buffer, AlGaN barrier and p-GaN cap layer. b) Zoomed-in image of the AlGaN barrier, which shows an AlGaN thickness of 8.2 nm and a thin darker layer at the AlGaN/p-GaN interface. The darker contrast indicates an increased aluminum content.

an AlGaN barrier thickness of only 8.2 nm with a thin darker layer at the AlGaN/p-GaN interface, which indicates an increased aluminum content. During cool down from the AlGaN growth conditions to those of the p-GaN growth, an etching of AlGaN most likely occurred. The Al atoms of the removed 3 nm AlGaN were then apparently incorporated during the p-GaN growth start leading to the thin high-Al-content layer with an approximate thickness of 0.9 nm. On the other hand, this layer should increase the selectivity of the p-GaN dry etch and act as a more effective etch stop layer.

The experimental transfer characteristics of the p-GaN-gated HFET are shown in Fig. 6.19. Due to the buffer without high voltage capabilities, a basic HFET device geometry is used instead of a high-voltage design (cf. Fig. A.5). From Eq. (6.1), with a thickness of 8.2 nm and an Al content of 24%(neglecting the thin high Al-content layer), a threshold voltage V_{th} of 1.78 V can be estimated. The semilogarithmic plot [see Fig. 6.19(a)] shows a V_{th} of 2.1 V extracted at 1 µA/mm, which is close to the calculated value. Apparently, the high Al content layer does not significantly shift V_{th} to more negative values. The sub-threshold swing (SS) equals 150 mV/dec, which is rather high in comparison to 75 mV/dec for the high-voltage device. The increased SS is caused by the already high gate current at V_{th}, which is detrimental for the electrostatic control of the gate over the 2DEG. The gate leakage current is similar to that of the high-voltage device (see section 6.5) with a maximum value of 7.6 mA/mm at $V_{GS} = 6$ V. Fig. 6.19(b) shows the linear transfer characteristics. The linearly extrapolated V_{th} is extracted to

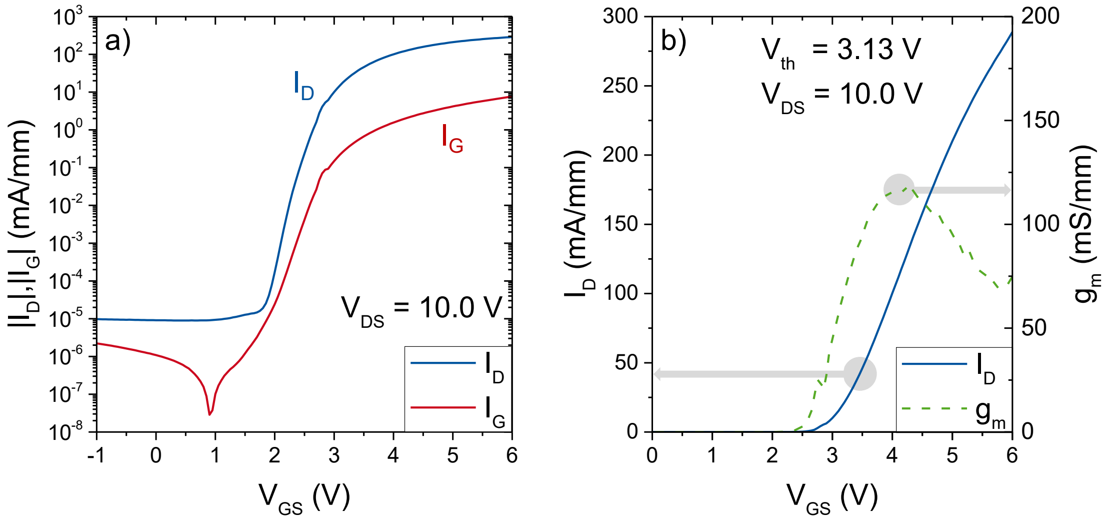


Figure 6.19.: Transfer characteristics of the high-V_{th} p-GaN-gated HFET at $V_{DS} = 10$ V in semilogarithmic a) and linear scale b).

3.13 V.

In comparison to the previous high-voltage p-GaN-gated HFET stack, the linearly extracted V_{th} is increased from 1.08 V to 3.13 V. However, a reduced SS, $g_{m,max}$ and saturation ON-current (even for the smaller devices shown here, see Fig. A.5) shows the trade-off between V_{th} and the resistance of the access regions of p-GaN-gated HFET as discussed in section 6.1.

Fig. 6.20 depicts the saturation current versus threshold voltage for different p-(In)GaN-gated HFETs from literature. Additionally, the gate-drain distance of the respective devices is given. A large gate-drain distance commonly leads to lower saturation currents.

The devices presented in this work show a higher saturation current at approximately the same threshold voltage in comparison to literature values. This proves the advantages of the presented concept and paves the way for further p-GaN-gated HFET device performance improvements. The main challenge for this process lies in the analysis and reduction of the gate leakage currents, since the current values are 2-4 orders of magnitude higher than values from the literature presented in Fig. 6.20.

6.7. Advanced Concepts

A drawback of the p-GaN-gated HFET is the use of the same AlGaN barrier for the gate and access regions, which leads to the trade-off between V_{th} and R_{ON} (see above). If

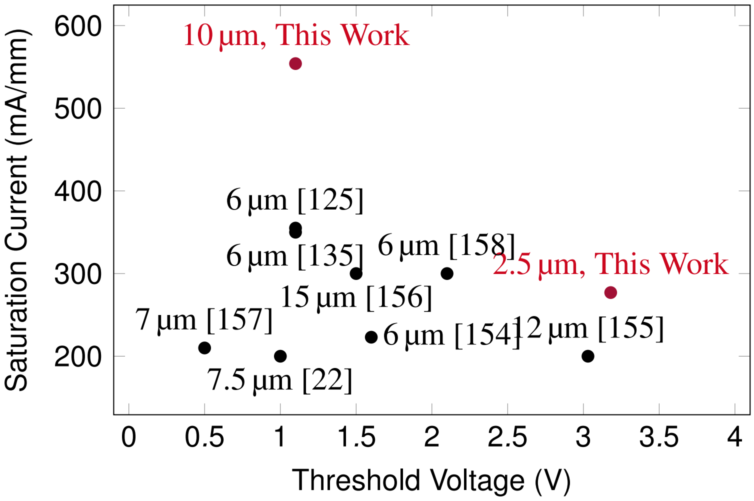


Figure 6.20.: Saturation current versus threshold voltage for E-mode p-GaN-gated HFET. All V_{th} values were extracted from linear extrapolation. The text labels show the gate-drain distance L_{GD} of the respective devices. For an E-mode p-GaN-gated HFET, a high saturation current with a large threshold voltage is desired (top right corner).

one could employ barriers which are locally different, the individual properties could be optimized independently. This can be achieved by barrier etching and using a selective-area regrowth (SAR) technique of the p-GaN layer instead of a continuously grown p-GaN/AlGaN/GaN stack [159].

6.7.1. Selective-Area Regrowth p-GaN-gated HFET

The process for SAR is depicted in Fig. 6.21. It starts with a basic AlGaN/GaN HFET stack with standard barrier thickness. The wafer is then coated with a masking material (e.g. aluminum oxide or silicon oxide), and the gate areas are opened by plasma etching. Now, the barrier is recessed similarly to the MOS-hybrid HFET (see section 5.1) down to a defined thickness depending on the desired V_{th}. The masked sample is then transferred to the MOCVD system, and p-GaN is grown selectively into the etched openings. A similar process can be found in [160] with a planar regrowth.

In this device, the low resistance access region is now combined with a normally-off gate area, which boosts the overall performance. The disadvantage of this process scheme is the need for a second epitaxy step, which leads to strong increase in production cost. Additionally, the regrowth is very sensitive to the sample surface, thus plasma etching and air storage introduce additional challenges [161].

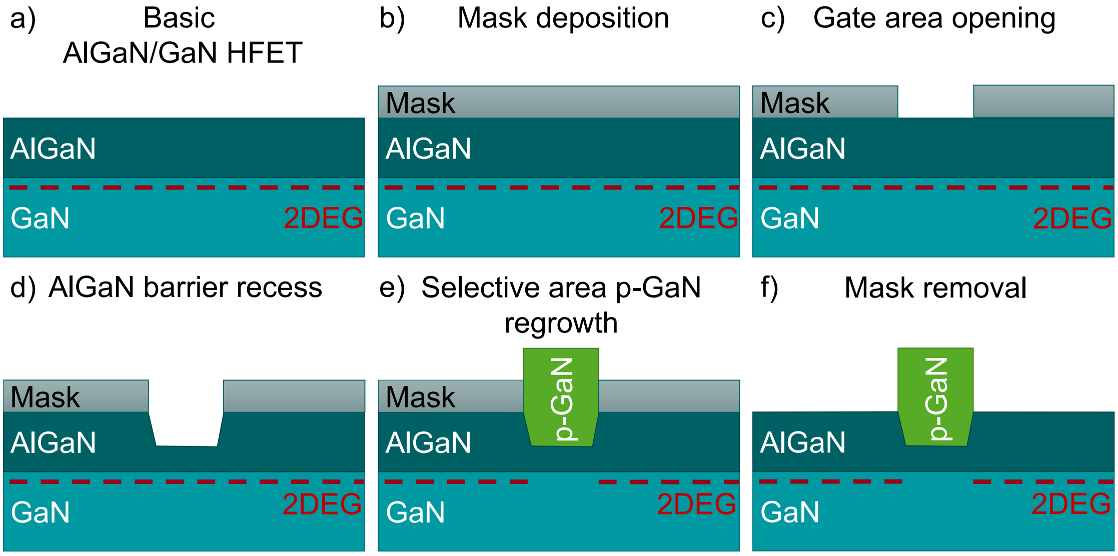


Figure 6.21.: Schematic of the selective-area regrowth p-GaN-gated HFET process with a recessed AlGaN barrier.

6.7.2. p-GaN Hybrid Drain

The p-GaN regrowth process cannot only avoid the trade-off between V_{th} and R_{ON}, but also enables a "hybrid drain" in p-GaN-gated HFET [23]. For this approach, an additional p-GaN island is deposited in direct proximity to the drain and is connected to the same drain potential. Due to the thick AlGaN barrier below the p-GaN island (AlGaN only recessed in the gate region), the 2DEG below is not fully depleted (see Fig. 6.5). A schematic of this device is shown in Fig 6.22. The hybrid drain on a thin AlGaN barrier would lead to a partial depletion of the 2DEG, because the drain voltage is low during ON-state. Thus, the ON-resistance would be increased.

A major challenge of conventional HFET carbon buffers is current collapse (see section 3.3). This effect occurs after high OFF-state V_{DS}, which leads to electron injection into buffer traps. The hybrid drain inhibits the negative charging by also injecting holes during OFF-state of the device. Due to the carrier injection of both polarities, no charge build-up takes place. This effectively suppresses the current collapse and dynamic R_{ON} increase. In [23], the p-GaN-gated HFET shows a dynamic R_{ON} increase over V_{DS} of 550 V, whereas the device with a hybrid drain has stable R_{ON} up to 800 V (device breakdown at 1000 V).

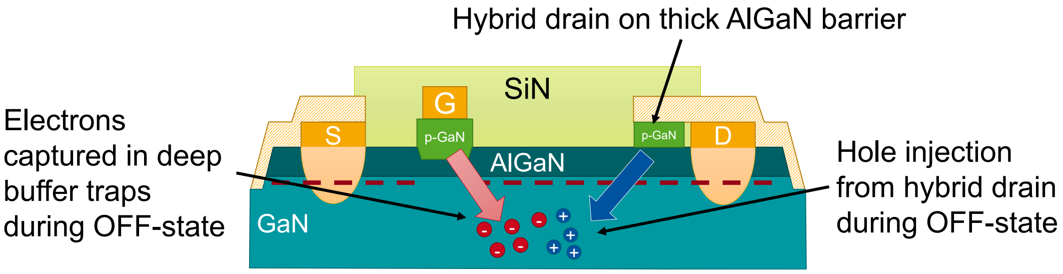

Hybrid drain on thick AlGaN barrier
SiN
G
S
D
p-GaN
p-GaN
AlGaN
GaN
Electrons captured in deep buffer traps during OFF-state
Hole injection from hybrid drain during OFF-state

Figure 6.22.: Schematic of a hybrid-drain p-GaN-gated HFET. During OFF-state, electrons and holes are injected into the buffer, which inhibits current collapse from buffer charging.

6.7.3. Monolithically-integrated GaN Cascode

The SAR p-GaN-gated HFET with a recessed AlGaN barrier is able to boost the device performance, but might introduce new points of failure. The major degradation mechanism in gallium nitride HFET is the electrical degradation of the AlGaN barrier at the drain-side gate edge. Due to the high electrical field concentrated at the edge and the inverse piezoelectric effect, pit-like defects can form, leading to a decline in electrical performance (see Fig. 6.23) [162]. In the case of the SAR p-GaN-gated HFET, this electric field peak is located at the etch and regrowth interface, which has an inherently weaker structural integrity than a continuously grown AlGaN barrier. An approach to shift the electric field peak away from the regrowth area is a cascode configuration [163].

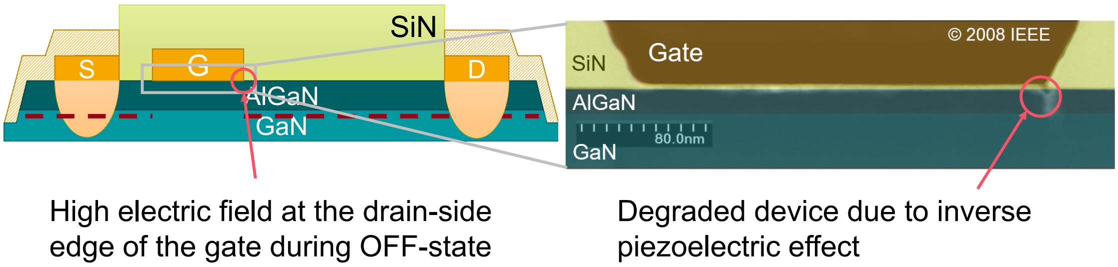

SiN
S
G
D
AlGaN
GaN
SiN
Gate
© 2008 IEEE
AlGaN
80.0nm
GaN
High electric field at the drain-side edge of the gate during OFF-state
Degraded device due to inverse piezoelectric effect

Figure 6.23.: Structural degradation of GaN HFET by the inverse piezoelectric effect due to the high electric fields at the drain-side gate edge during operation. SEM image taken from [162] and colored.

Working Principle of a Cascode

The cascode is a configuration of two transistors in which the gate potential of one transistor is used to control the circuit and the other one has a fixed gate potential and blocks the voltage in OFF-state. The cascode itself has three terminals, drain (D), source (S) and gate (G). A circuit diagram of the configuration is shown in Fig. 6.24(a). The upper transistor (block) is of normally-on type, and its gate potential is fixed to the source potential of the lower transistor (control), which is of normally-off type. Therefore, without any applied voltages, the block transistor is in ON-state while the control one is in OFF-state.

Fig. 6.24(b) shows the ON-state of the cascode. D is connected to a voltage source with a potential φ_D of V_D, S is connected to ground with a potential φ_S of 0 V and at terminal G, a potential φ_G higher than the threshold voltage of the control transistor $V_{th,control}$ is applied. Both transistors are in ON-state and a current flow I_D between terminal D and S is established.

When the cascode is switched to OFF-state ($\varphi_G < V_{th,control}$) depicted in Fig. 6.24(c), the control transistor initially blocks the current path between D and S, while the block transistor is still in ON-state. A current flow between D and the node between the two transistors leads to a rise in the potential φ_{inter} between the two transistors. When φ_{inter} reaches $V_{th,block}$, the block transistor and the whole cascode switches to the OFF-state. Now, the voltage drop over the block transistor equals the high potential $V_D - V_{th,block}$, while the voltage drop over the control transistor is only $V_{th,block}$. In conclusion, the voltage drop over the cascode in OFF-state is distributed over the two transistors, whereas the upper block transistor takes most of the voltage shielding the lower control transistor. Another advantage is the decoupling of the gate terminal from the drain terminal which mitigates the impact of the increased gate-drain capacitance due to the Miller effect [51].

In GaN technology, this principle is already used to fabricate normally-off devices by combining a high voltage normally-on GaN power transistor as blocking transistor and a conventional normally-off Si MOSFET as control transistor [12, 13]. The disadvantages of this normally-off topology are increased packing costs, an operation temperature limited by the Si MOSFET and an increased R_{ON} due to employment of two transistors. To circumvent these drawbacks, the full GaN cascode integration of a SAR p-GaN-gated HFET with a recessed AlGaN barrier is proposed, parts are already published in [164].

Monolithic GaN Integration

The core idea of the monolithically-integrated GaN cascode is the combination of the two transistors into one structure [51]. The process starts with the AlGaN barrier recess and SAR, which are shown in Fig. 6.21 on a standard AlGaN/GaN HFET wafer. The subsequent processing is depicted in Fig. 6.25. After SAR, the sample is subjected to

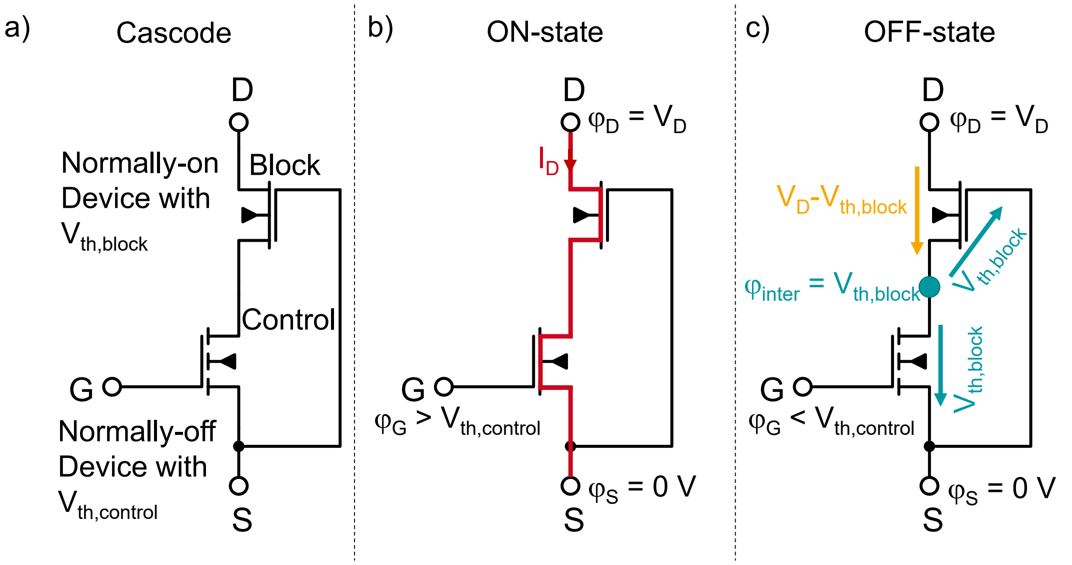

a)
Cascode
D
Normally-on
Device with
V_{th,block}
Block
Control
G
Normally-off
Device with
V_{th,control}
S
b)
ON-state
D
φ_D = V_D
I_D
G
φ_G > V_{th,control}
φ_S = 0 V
S
c)
OFF-state
D
φ_D = V_D
V_D-V_{th,block}
φ_{inter} = V_{th,block}
V_{th,block}
G
φ_G < V_{th,control}
V_{th,block}
φ_S = 0 V
S

Figure 6.24.: Schematic of a cascode configuration.

the basic HFET process: ohmic contact deposition and annealing, mesa formation by dry etching and a Mo gate metallization [see Fig. 6.25(b)]. The device is passivated by a thin 10 nm SiN_x layer [see Fig. 6.25(c)], and the gate electrode for the second normally-on HFET is deposited [see Fig. 6.25(d)]. The finished device is shown in Fig. 6.25(e). The entire structure now consists of two separate intrinsic HFET: below the recessed barrier and p-GaN, a normally-off HFET is formed, which is intrinsically connected to the second normally-on HFET over the 2DEG, located below the gate electrode on top of the SiN_x. The source and drain contacts as well as the access regions are shared by both transistors. If the normally-on gate is now connected to the source contact, a cascode configuration is established. This structure is similar to a device with a source field plate [165], the difference is the distance between the normally-on gate electrode and the 2DEG which is a lot smaller in this case (10 nm vs. 400 nm), thus enabling the cascode gate to switch off the transistor.

The benefits of the cascode, which are expected from the circuit considerations, are now analyzed by physics-based simulations. As a reference, a SAR p-GaN-gated HFET with a recessed barrier without second gate (referred to as p-GaN-gated HFET in the following) but otherwise equal geometries is taken. The dimensions of the discussed devices are gate-source distance L_{GS} of 1.5 µm, normally-off gate length L_{G1} of 2 µm, gate-to-gate distance L_{GG} of 2 µm, normally-on gate length L_{G2} of 2 µm and a gate-drain distance L_{DS} of 19 µm. Fig. 6.26 shows simulated electric field distributions and the gate-drain capacitance of the two devices. The devices are in OFF-state at $V_{GS} = 0$ V with a medium drain bias of $V_{DS} = 100$ V. For the p-GaN-gated HFET, the electric field

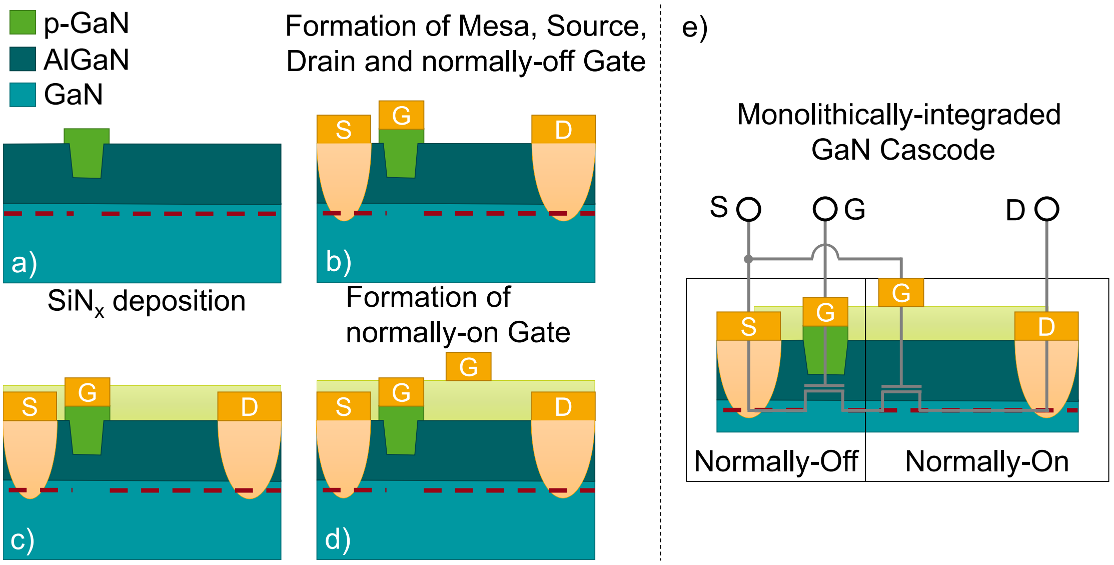

p-GaN
AlGaN
GaN
Formation of Mesa, Source, Drain and normally-off Gate
S
G
D
a)
b)
SiN$_x$ deposition
Formation of normally-on Gate
c)
d)
e)
Monolithically-integraded GaN Cascode
S
G
D
Normally-Off
Normally-On

Figure 6.25.: Schematic of the monolithically-integrated GaN cascode. a) AlGaN/GaN HFET with an already recesses barrier and SAR p-GaN (see Fig 6.21). b) Deposition and annealing of ohmic contacts as well as gate metallization. c) Passivation of the device by thin SiN$_x$ acting as gate dielectric for the second gate. d) Deposition of the second gate electrode. e) Monolithically-integrated GaN cascode with a superimposed equivalent circuit.

peak is located at the gate edge of the device, whereas the major peak is shifted to the second gate in the cascode configuration with only a small electric field peak remaining at the normally-off gate. In this example, the field peak at the normally-off gate is reduced by 74% confirming the screening effect of the second normally-on HFET. Since the potential offset between the two gates is defined by the threshold voltage of the normally-on HFET, the electric field peak at the normally-off gate will stay constant even for higher V_{DS}.

For high-voltage devices, the gate length usually needs to be sufficiently large due to a possible punch-through of the depleted channel in OFF-state [166]. Due to the potential screening mentioned above, this design constraint for the normally-off control part is circumvented, allowing for shorter gates and therefore a reduced gate-source capacitance C_{GS}.

Additionally, the potential screening reduces the Miller capacitance C_{GD}, which couples the drain node to the gate node. In the standard transistor design, C_{GD} appears increased by the amplification of the transistor, the so-called Miller effect [167], which is avoided in a cascode [51]. Fig. 6.26(b) shows a SPICE simulation of C_{GD} for the p-GaN-gated HFET and the cascode. A reduction by more than one order of magnitude can be seen as long as V_{DS} is greater than V_{th} of the normally-on HFET (otherwise the normally-on HFET is not switched off in the OFF-state of the cascode). Due to the re-

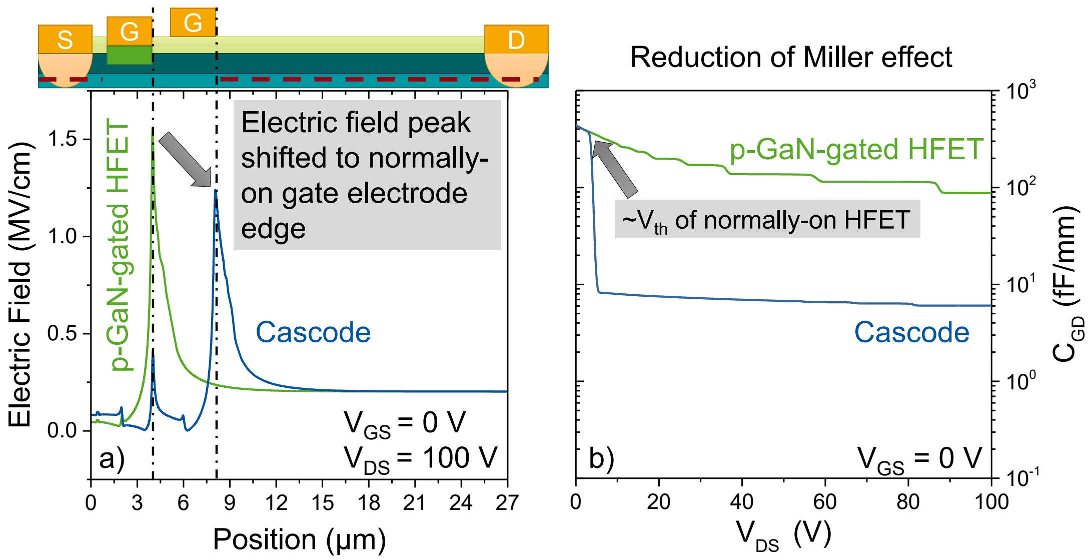


Figure 6.26.: Simulated electric field distribution between the source and drain contacts a) and gate-drain capacitance b) of the p-GaN-gated HFET (green) and the GaN cascode (blue).

duction of the total input capacitance C_{GS}+C_{GD}, this enables faster switching transients of the device. This is particularly important for devices operated in a hard-switched mode, e.g. in a DC-DC converter.

In this chapter, the advantages of the p-GaN-gated HFET were discussed. The simple electrostatic model shows that a p-GaN layer on top of the AlGaN barrier can deplete the underlying 2DEG leading to normally-off operation. The parameters defining the threshold voltage were presented and their respective effects were illustrated by simulations of energy bands and I-V curves. The results show a trade-off between highly-positive threshold voltages in the intrinsic HFET and the sheet carrier density in the access regions. Afterwards, a complete process for the manufacturing of p-GaN-gated HFET was presented. For the removal of GaN outside of the gate area, a selective $Cl_2/O_2/N_2$ dry-etching process was adopted and a self-aligned encapsulated Mo gate was introduced. The complete process was then used to manufacture two types of devices: one aimed at large saturation currents and breakdown voltages with a threshold voltage of 1 V and one with a higher threshold voltage of 3 V. Additionally, the suitability of the high performance devices for operation at elevated temperatures was investigated. In the last part, advanced concepts for the p-GaN-gated HFET based on selective-area regrowth of p-GaN are presented, such as the hybrid drain and the fully-integrated GaN cascode.

7. Comparison of MISHFET, MIS-hybrid HFET and p-GaN-gated HFET

In this chapter, the important performance indicators of transistors for radio-frequency (RF) and power applications, respectively, are presented. Based on this information, the most suitable application of each device topology of the previous chapters will be discussed.

For RF applications, one of the central properties is the limit of operation frequency. Two characteristic values are defined to classify devices, the maximum oscillation frequency f_{max}, for which the power amplification equals unity, and the transit frequency f_t, for which the short-circuit current amplification equals one. In a simple transistor model, f_t can be calculated with the following equation [168]:

$$f_t = \frac{g_m}{2\pi \cdot C_{GS}} \tag{7.1}$$

where g_m is the transconductance of the device and C_{GS} the gate-source capacitance. Thus to maximize f_t, C_{GS} has to be minimized, i.e. the gate area should be as small as possible, and g_m, which is given by the following equations, has to be maximized [169]:

$$g_{m,i} = C_{n,gate} \cdot v_s \left(1 - \frac{1}{\sqrt{1 + 2\,\frac{\mu \cdot e \cdot n_s}{C_{n,gate} \cdot v_s \cdot L_G}}} \right) \tag{7.2}$$

$$g_m = \frac{g_{m,i}}{1 + g_{m,i} \cdot (R_C + R_{GS})} \tag{7.3}$$

where $C_{n,gate}$ is the area-normalized capacitance between the gate metal and 2DEG (see Fig. 3.2). From the equation for the transconductance of the intrinsic HFET $g_{m,i}$ follows that high mobilities (μ) and sheet carrier densities (n_s) are needed as well as short gate lengths (L_G) and thin barriers and insulators ($C_{n,gate}$). Furthermore, the extrinsic

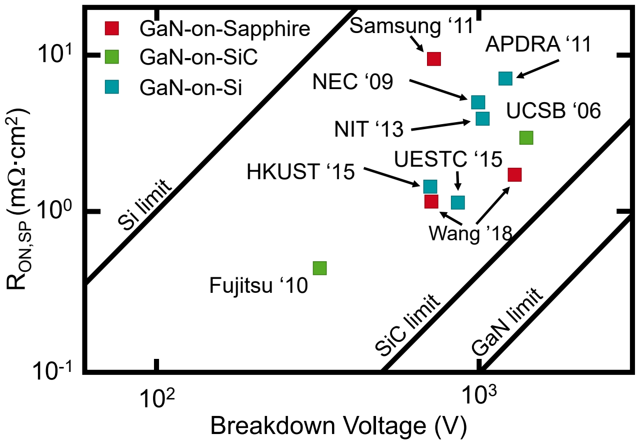


Figure 7.1.: Baliga's figure-of-merit with state-of-the-art normally-off power HFET and the different theoretical material limits. Image after [171].

transconductance of the whole device g_m is reduced by the contact resistance of the source contact R_C and the resistance of the access region between gate and source R_{GS}. Thus, those resistances should also be minimized for RF operation.

For power devices, one set of performance indicators are the device ON-resistance R_{ON} and breakdown voltage V_{BR}. They can be evaluated from the physical properties of mobility, sheet carrier density and device geometry. While RF devices are aggressively downscaled for maximum frequency operation [52] (see above), power devices are targeted at certain V_{BR} (e.g. 200 V or 650 V) while minimizing R_{ON} [170]. The main scaling parameter of the HFET for breakdown voltage is the gate-drain distance L_{GD} (part of the access regions). By increasing L_{GD}, the gate-drain voltage is dropping over a longer distance and thus, the electric field within the device is reduced and V_{BR} increases. But at the same time a larger L_{GD} increases R_{ON}. This relationship is expressed by the Baliga's figure-of-merit in Fig. 7.1, which is used to compare material systems and devices with different geometries. The plots shows that GaN devices in general are already well past the Si limit, but still need further optimization to reach the GaN limit.

In the following, three state-of-the-art devices are taken from literature to show the R_{ON} bottleneck for RF and high-voltage applications. Fig. 7.2 shows a schematic of an HFET with the different components of R_{ON}: twice the contact resistance R_C, the channel resistance of the intrinsic HFET R_{Ch} below the gate, and the resistance of the access regions R_{GS} and R_{GD}. On the right side of the image, the resistances for the three HFET are shown in absolute (b) and relative values (c):

- RF,ON: normally-on radio-frequency HFET [52]

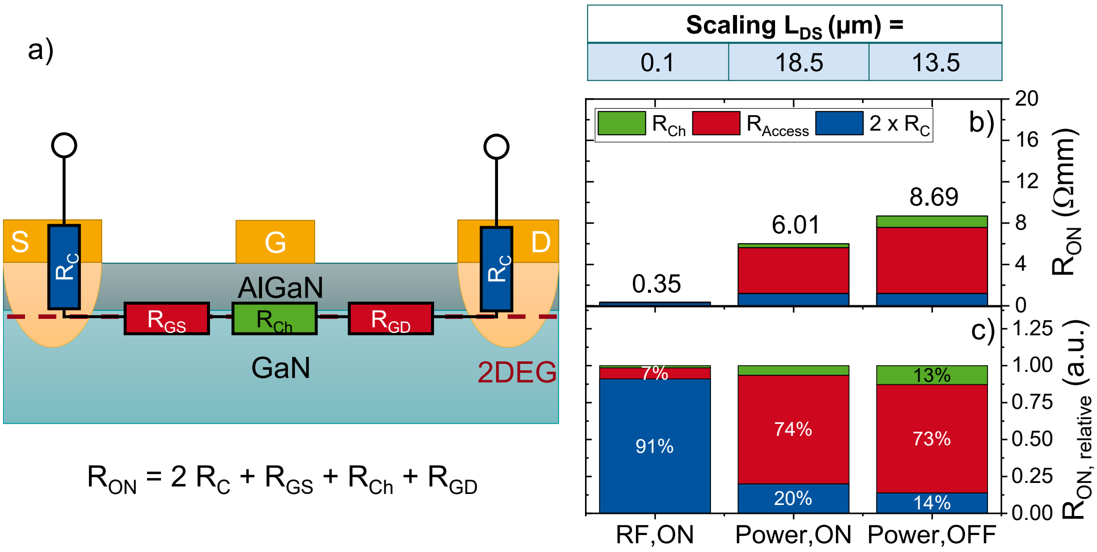


Figure 7.2.: Equivalent circuit of R_{ON} in an HFET [52, 117, 172]. a) Schematic of an HFET with the respective resistors. b) Absolute resistance values of the three different example devices. Values are normalized to the gate width. c) Relative resistance values normalized to the total R_{ON}.

- Power,ON: normally-on power HFET [172]
- Power,OFF: normally-off power HFET [117]

The resistances are normalized to the gate width and are calculated from the mobility, sheet carrier density and geometry.

RF,ON shows the lowest R_{ON} resistance due to downscaling ($L_{DS} = 0.1\,\mu m$) and is dominated by the contact resistance (91%). Here, the resistance of the access regions has only a minor impact. For both of the power transistors however, the resistance of the access regions is the major resistive component (74% and 73%). This shows that for power transistor performance, a low resistance in the access regions is vital, which can be achieved by high electron mobilities and densities.

Based on these considerations for RF and power applications, the different topologies will now be evaluated. Further information on power circuits, which employ these different topologies, can be found in [173].

The normally-off MISHFET is a standard HFET structure, in which the AlGaN barrier below the gate is recessed down to a few nanometers and a gate dielectric is deposited [see Fig. 7.3(a)]. Vital for a positive V_{th} are the dielectric and barrier thickness as well as the interface charge density between the two. Due to the small distance between the gate electrode and the 2DEG, theses devices exhibit an excellent channel control and high transconductance. Additionally, the remaining AlGaN barrier leads to

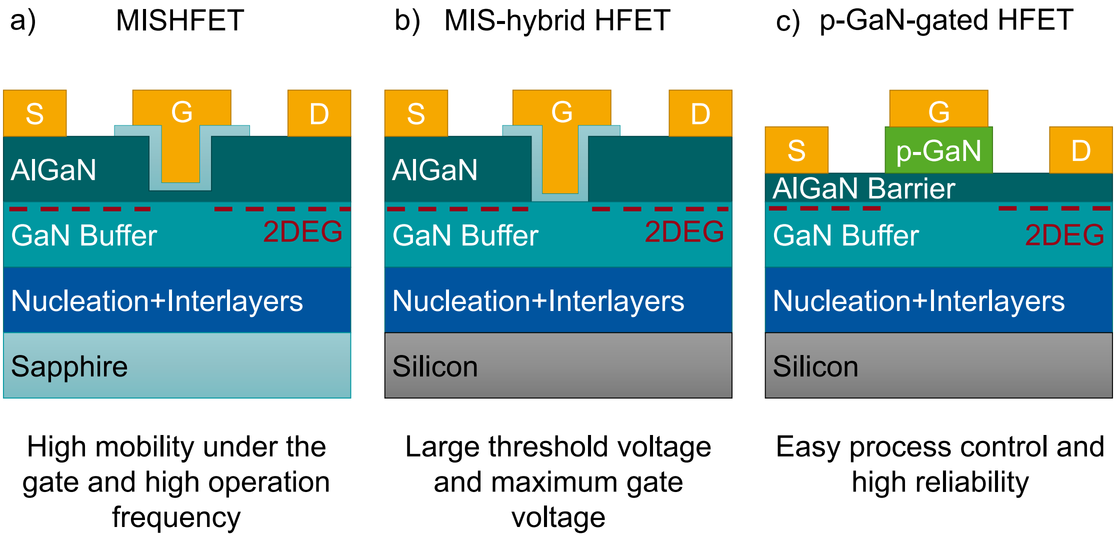

a) MISHFET
b) MIS-hybrid HFET
c) p-GaN-gated HFET
S
G
D
AlGaN
GaN Buffer
2DEG
Nucleation+Interlayers
Sapphire
S
G
D
AlGaN
GaN Buffer
2DEG
Nucleation+Interlayers
Silicon
G
S
p-GaN
D
AlGaN Barrier
GaN Buffer
2DEG
Nucleation+Interlayers
Silicon
High mobility under the gate and high operation frequency
Large threshold voltage and maximum gate voltage
Easy process control and high reliability

Figure 7.3.: Schematic cross section of the three different normally-off topologies for lateral AlGaN/GaN HFET. a) MISHFET with an ultrathin AlGaN barrier. b) MIS-hybrid HFET with a completely removed barrier. c) p-GaN-gated HFET with a medium thick barrier and p-GaN cap layer.

high electron mobilities, thus large f_t are expected. Originating from these properties, normally-off MISHFET represent the fastest normally-off topology with the lowest positive threshold voltages and ON-resistances (see discussion above). A downside is the need of a precise dry-etch process for the barrier recess and the excellent control of interface charge density. Both aspects can be very challenging, particularly homogeneous processes on large wafer areas. Furthermore, the low positive V_{th} makes this topology unsuitable for power switches, because the transistor can accidentally turn to ON-state, and is better used in continuous-wave amplifiers.

Similar to the normally-off MISHFET is the MIS-hybrid HFET [see Fig. 7.3(b)]. Here, the AlGaN barrier below the gate is completely removed, commonly even a few nanometers of the GaN channel below. Afterwards, a gate dielectric and the electrode are deposited. This device is therefore a combination of a MISFET in the gate area and an HFET in the access regions. In comparison to the MISHFET, the MIS-hybrid HFET loses the superior mobility in the gate area, but also removes the V_{th} limitations. This allows for high threshold voltages and, through thick gate dielectrics, a large maximum forward gate bias (>10 V). To avoid the low-mobility bottleneck of the gate area, the topology is best suited for high-voltage devices with a large gate-drain distance and thus a limitation by the access resistance instead of the channel resistance below the gate (see above). Due to the complete removal of the barrier, the recess by dry etching has a higher error margin, but the interface charge density still needs to be well controlled.

Both of the technologies above suffer from the lack of a high quality dielectric with a low interface density, good insulation properties and high stability. The most promising candidates are amorphous aluminum nitride or oxide and LPCVD silicon nitride. All of these dielectrics are already employed for normally-on devices to reduce gate leakage currents and, due to the avoidance of the spill-over regime, a stable V_{th}. In normally-off devices, the dielectrics have higher requirements regarding stability to meet V_{th} hysteresis limits and device lifetime standards, particularly at higher junction temperatures. However, if these challenges are overcome in the near future, the devices will be an attractive addition to the landscape of semiconductor devices. In the meantime, the normally-off topology without a necessary dielectric, the p-GaN-gated HFET has started to penetrate the mainstream market.

In a p-GaN-gated HFET, normally-off operation is achieved by a barrier thickness in between the low thickness required for a normally-off MISHFET and the high thickness in an standard HFET, in combination with a p-GaN layer on top, which locally depletes the 2DEG [see Fig. 7.3(c)]. The p-GaN has shown a wide process window in terms of thickness and doping, which eases process control requirements. In contrast to the MIS technologies, the as-grown wafers are normally-off and the 2DEG is re-accumulated in the access regions by the removal of the p-GaN cap layer. This can be carried out by a highly selective dry-etch process, which avoids the loss of sheet carrier density in the access regions due to unintentional AlGaN barrier thinning. Based on these advantages, large-scale production is possible, which makes these devices cost efficient. Device operation up to 500 °C was already shown, which enables electronics in harsh environments. Drawbacks of this topology are rather slow devices due to switching over a pn-like junction and the limitation of forward gate voltage to below 7 V to avoid premature gate breakdown [173].

8. Conclusion and Outlook

Throughout this work, three different approaches to turn the inherently normally-on HFET into a normally-off device were presented: the MISHFET, the MIS-hybrid HFET and the p-GaN-gated HFET. The basic concept is a local modification of the intrinsic HFET in the gate area to achieve a positive threshold voltage, while retaining the key properties of the heterostructure, high electron mobility and large carrier densities in the access regions.

For the two MIS topologies, an insulator is required, which is deposited on a partially or completely-recessed AlGaN barrier for the MISHFET and MIS-hybrid HFET, respectively. It was shown that the insulator can shift the threshold voltage, while the direction and magnitude depend on the positive fixed charge density at the insulator/semiconductor interface. The effective net charge density can change during operation due to electron capture in interface traps at positive bias of the gate diode. While electrons in shallow traps lead to threshold voltage hysteresis, electrons in deep traps act as quasi-permanent fixed charge, which shifts the threshold voltage to more positive values. This effect can also be utilized in a flash-like memory device based on the MISHFET, for which an erasing technique through hole supply from a buried 2DHG was proposed and verified by experiments. These proof-of-concept devices already require lower programming/erasing voltages than conventional flash memory, but further investigations regarding charge retention and switching speeds are necessary. For MISHFET however, the positive fixed interface charge and shallow trap density need to be minimized. Two approaches, post-deposition annealing of the deposited insulator and oxygen plasma annealing of the semiconductor surface prior to deposition were presented. Both processes result in a lower positive charge and trap density. Through oxygen plasma annealing immediately after the AlGaN barrier recess, these values could be sufficiently reduced below the GaN polarization [see Eq. (2.14)], which led to a pronounced positive threshold voltage shift. This effect is attributed to the formation of a two-monolayer oxide at the AlGaN surface. Transport through ambient air between barrier recess in an ICP-RIE tool and insulator deposition in a PEALD tool already caused a partial surface oxidation, which deteriorated the quality of the interface. A cluster tool of ICP-RIE and PEALD or in-situ cleaning steps in the PEALD tool prior to insulator deposition could be used, which should further improve the interface quality.

From an electrostatic model, the limitations for the threshold voltage shift by an insulator were derived. It was shown that the onset of hole accumulation limits the potential drop over the insulator, and thus also the achievable positive threshold voltage shift. The maximum potential drop was calculated to approximately 1.8 V, with only minor variation for different dielectrics on top of an AlGaN barrier.

Since the AlGaN barrier always causes a negative threshold voltage shift, the MIS-hybrid HFET, in which the barrier is completely-recessed, is investigated. A major drawback of this topology is the reduced mobility in the gate area due to the electron transport at the insulator/GaN interface. Inserting an amorphous AlN spike between gate oxide and GaN channel has proven to increase the mobility. For the PEALD AlN deposition, a new process with TMAl and a forming gas (H_2 in Ar)/N_2 mixture was developed.

The results from both MIS topologies have shown that the control of AlGaN etch depth and the interface charge properties are important. Small variations of these values can already cause a significant threshold voltage shift, which makes achieving homogeneous results challenging, particularly on large wafers.

A normally-off topology which does not require a gate insulator or an AlGaN barrier recess is the p-GaN-gated HFET. Here, the AlGaN barrier thickness on the pristine wafer is already in the range of 10 nm, and the underlying 2DEG is depleted by a p-GaN cap layer. By removing the p-GaN outside of the gate area, the 2DEG is restored and the sheet carrier density is further increased by SiN passivation. To enable precisely controlled processes, a selective dry-etching process, which automatically stops at the AlGaN barrier, and a self-aligned Mo gate-first process were introduced. It was also shown that theses p-GaN-gated HFET are able to operate at temperatures up to 500 °C. This may enable electronics, which operate in high-temperature environments such as furnaces, drill heads and turbines.

But due to the continuous AlGaN barrier in the gate area and access regions, a trade-off between threshold voltage and sheet carrier density in the access regions was encountered. This trade-off can be avoided by employing a thicker AlGaN barrier, recess-etching in the gate area and selective-area regrowth of p-GaN into the resulting gate trench. This process chain also enables other advanced concepts such as the hybrid drain or fully-integrated GaN cascode.

In comparison of all three normally-off topologies, the MIS approaches promise the best electrical properties. They offer inherently low gate leakage currents, strong resilience against gate overdrive voltages and the highest achievable threshold voltages. But the success of these devices is directly related to the maturity of the involved dry-etching and insulator deposition processes. In-situ cleaning, precise atomic layer etching or barrier regrowth steps are necessary to achieve a reliable process, which is a reason why these topologies have not been commercialized yet. In contrast, the p-GaN-gated HFET has already achieved a sufficient process maturity to be used in consumer products together with Si/GaN cascode devices. Both present an excellent bridging technology for GaN normally-off until the MIS devices are ready to enter the market.

A. Appendix

A.1. Parameters for Calculations

Table A.1.: Parameters for calculating the n_s vs. t_{AlGaN} profiles of Fig. 2.9.

Al content	ϕ_B**-**ΔE_C [36]	ε_{AlGaN} [29]	σ_{AlGaN}**-**σ_{GaN}	m^*_{GaN} [29]
Units	(V)	(-)	(C/m^2)	(-)
5%	1	$10.2815\cdot\varepsilon_0$	0.00295	$0.228\cdot m_e$
10%	1	$10.2830\cdot\varepsilon_0$	0.00610	$0.228\cdot m_e$
15%	1	$10.2845\cdot\varepsilon_0$	0.00945	$0.228\cdot m_e$
20%	1	$10.2860\cdot\varepsilon_0$	0.01302	$0.228\cdot m_e$
25%	1	$10.2875\cdot\varepsilon_0$	0.01680	$0.228\cdot m_e$
30%	1	$10.2890\cdot\varepsilon_0$	0.02081	$0.228\cdot m_e$
35%	1	$10.2905\cdot\varepsilon_0$	0.02505	$0.228\cdot m_e$

A.2. Wafer List

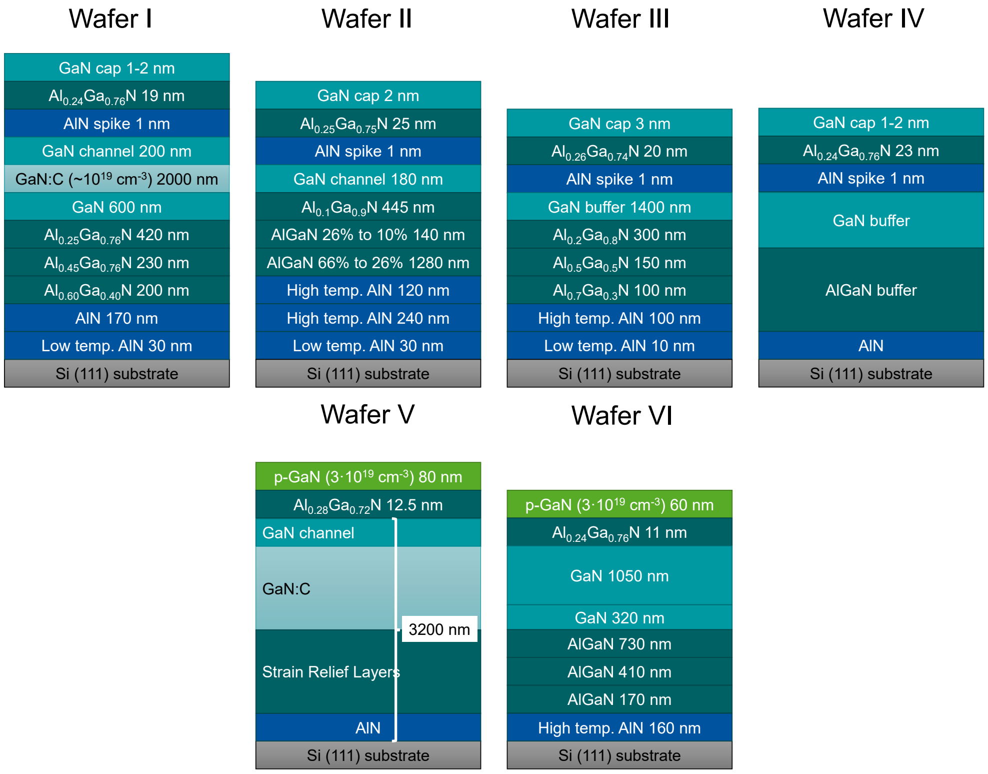
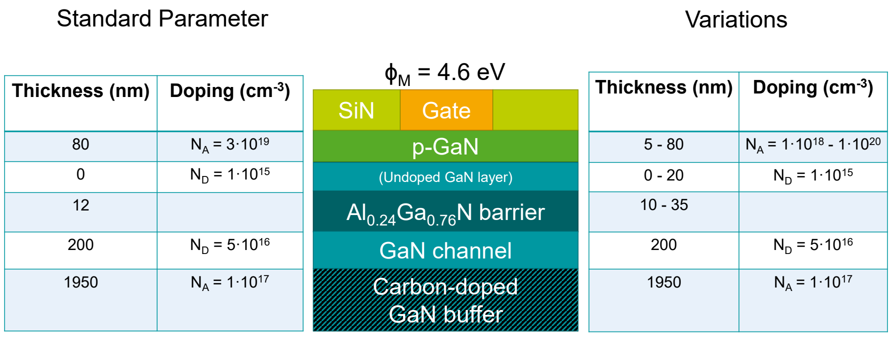

Wafer I
GaN cap 1-2 nm
$Al_{0.24}Ga_{0.76}N$ 19 nm
AlN spike 1 nm
GaN channel 200 nm
GaN:C (~10^{19} cm^{-3}) 2000 nm
GaN 600 nm
$Al_{0.25}Ga_{0.76}N$ 420 nm
$Al_{0.45}Ga_{0.76}N$ 230 nm
$Al_{0.60}Ga_{0.40}N$ 200 nm
AlN 170 nm
Low temp. AlN 30 nm
Si (111) substrate
Wafer II
GaN cap 2 nm
$Al_{0.25}Ga_{0.75}N$ 25 nm
AlN spike 1 nm
GaN channel 180 nm
$Al_{0.1}Ga_{0.9}N$ 445 nm
AlGaN 26% to 10% 140 nm
AlGaN 66% to 26% 1280 nm
High temp. AlN 120 nm
High temp. AlN 240 nm
Low temp. AlN 30 nm
Si (111) substrate
Wafer III
GaN cap 3 nm
$Al_{0.26}Ga_{0.74}N$ 20 nm
AlN spike 1 nm
GaN buffer 1400 nm
$Al_{0.2}Ga_{0.8}N$ 300 nm
$Al_{0.5}Ga_{0.5}N$ 150 nm
$Al_{0.7}Ga_{0.3}N$ 100 nm
High temp. AlN 100 nm
Low temp. AlN 10 nm
Si (111) substrate
Wafer IV
GaN cap 1-2 nm
$Al_{0.24}Ga_{0.76}N$ 23 nm
AlN spike 1 nm
GaN buffer
AlGaN buffer
AlN
Si (111) substrate
Wafer V
p-GaN ($3 \cdot 10^{19}$ cm^{-3}) 80 nm
$Al_{0.28}Ga_{0.72}N$ 12.5 nm
GaN channel
GaN:C
3200 nm
Strain Relief Layers
AlN
Si (111) substrate
Wafer VI
p-GaN ($3 \cdot 10^{19}$ cm^{-3}) 60 nm
$Al_{0.24}Ga_{0.76}N$ 11 nm
GaN 1050 nm
GaN 320 nm
AlGaN 730 nm
AlGaN 410 nm
AlGaN 170 nm
High temp. AlN 160 nm
Si (111) substrate

Figure A.1.

A.3. Overview TCAD-Simulations p-GaN-gated-HFET


ϕ_M = 4.6 eV
SiN
Gate
p-GaN
(Undoped GaN layer)
$Al_{0.24}Ga_{0.76}N$ barrier
GaN channel
Carbon-doped GaN buffer

Standard Parameter

Thickness (nm)	Doping (cm^{-3})
80	$N_A = 3 \cdot 10^{19}$
0	$N_D = 1 \cdot 10^{15}$
12	
200	$N_D = 5 \cdot 10^{16}$
1950	$N_A = 1 \cdot 10^{17}$

Variations

Thickness (nm)	Doping (cm^{-3})
5 - 80	$N_A = 1 \cdot 10^{18} - 1 \cdot 10^{20}$
0 - 20	$N_D = 1 \cdot 10^{15}$
10 - 35	
200	$N_D = 5 \cdot 10^{16}$
1950	$N_A = 1 \cdot 10^{17}$

Figure A.2.

A.4. Basic HFET Processing

In this section, a standard process for the manufacturing of a double-finger HFET will be introduced briefly. Similar processes to the presented one are used for all the devices throughout this work. The single steps will be shown in order of their occurrence within the process chain and are visualized in Fig A.3 + A.4.

Ohmic Contacts

The first step is the formation of ohmic source- and drain contacts for a low-resistance contact to the 2DEG. The contact areas are defined by optical lithography with an image reversal process and metal lift-off. Afterwards, a barrier recess by dry-etching is performed to thin down the AlGaN barrier to approximately 10 nm improving the contact resistance [174]. Subsequently, the sample is loaded into an electron beam evaporator. The deposited ohm metal stack consists of Ti/Al/Ni/Au with thicknesses of 15/100/40/50 nm, respectively [175]. Contact annealing is performed in a rapid thermal annealing (RTA) process at 825 °C for 30 sec in N_2. The defined contacts and annealing are shown in Fig A.3(a)+(b).

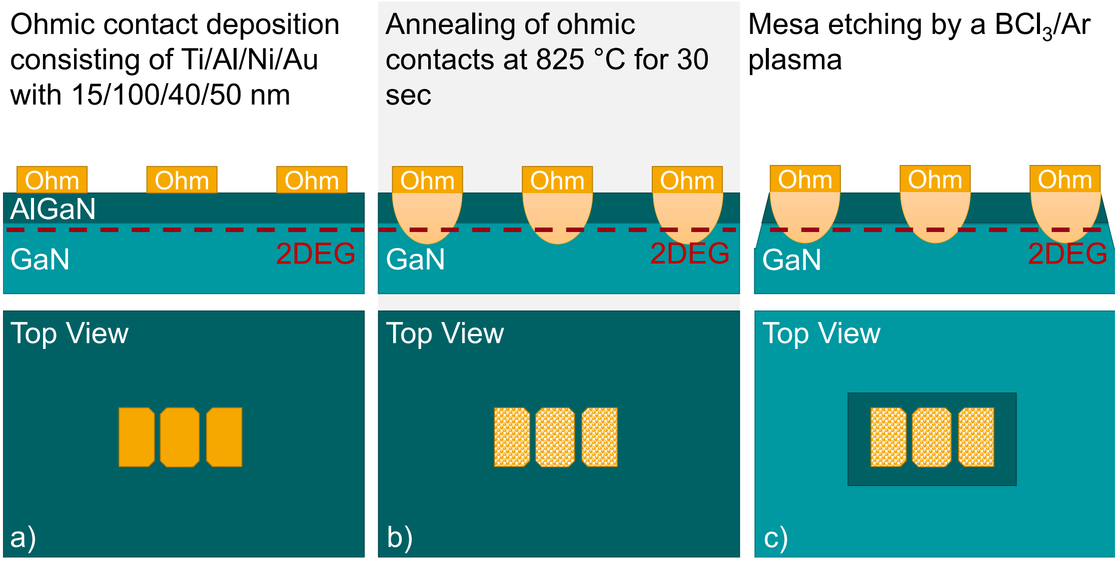

Ohmic contact deposition consisting of Ti/Al/Ni/Au with 15/100/40/50 nm
Annealing of ohmic contacts at 825 °C for 30 sec
Mesa etching by a BCl_3/Ar plasma
Ohm
Ohm
Ohm
AlGaN
GaN
2DEG
Top View
a)
b)
c)

Figure A.3.: Schematic of the first process steps for a double-finger HFET. a) Ohmic contact deposition by electron beam evaporation. b) Rapid thermal annealing of the ohmic contacts. c) Mesa definition by dry-etching in a BCl_3/Ar plasma.

Mesa Definition

Device area definition and isolation is achieved by mesa dry-etching. The mesa area is defined by a positive lithography process. The AlGaN barrier and parts of the GaN are then removed by a BCl_3/Ar dry-etch with an etch depth of 100 nm [176]. The mesa etch is performed after the ohmic contact anneal to mitigate high temperature degradation of the GaN surface leading to higher buffer leakage currents. This step is depicted in Fig A.3(c). Another possibility for mesa isolation is ion implantation which has the advantage of a more planar processing [177]. The ohmic contacts are located entirely on the mesa area.

Gate Schottky Contact

The gate metalization is deposited by electron beam evaporation and consists of Ni/Au with thicknesses of 50/200 nm, respectively [178], which forms a Schottky (S) contact to AlGaN. The contacts are defined by optical lithography in a two layer photoresist process (lift-off + positive resist) and metal lift-off [see Fig A.4a)]. The gate fingers are located on the mesa, while the gate connector pad and the finger tips are protruding over the mesa edge onto the GaN buffer.

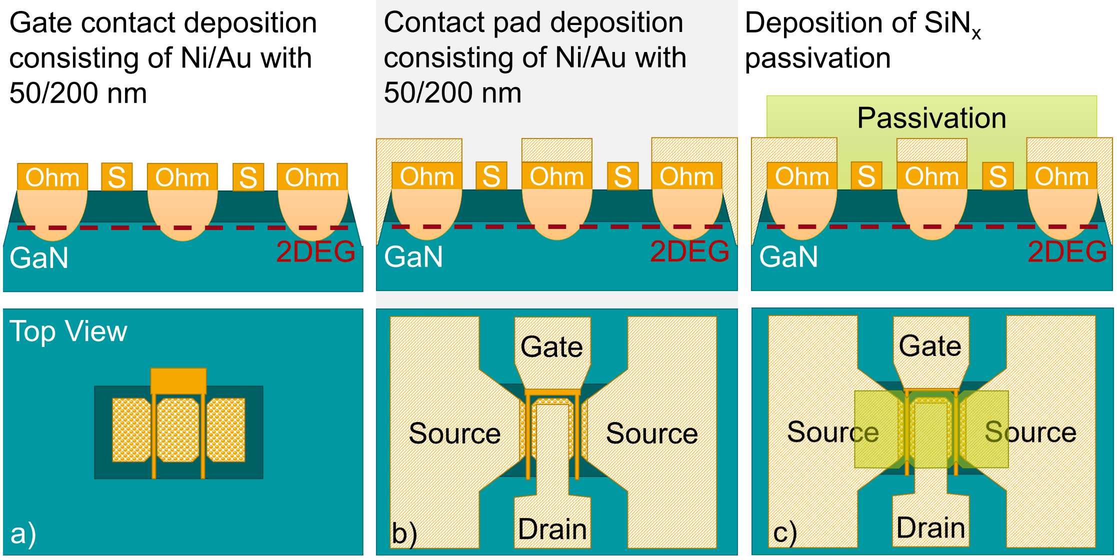

Gate contact deposition consisting of Ni/Au with 50/200 nm
Contact pad deposition consisting of Ni/Au with 50/200 nm
Deposition of SiN$_x$ passivation
Passivation
Ohm
S
Ohm
S
Ohm
GaN
2DEG
Top View
a)
Gate
Source
Source
Drain
b)
c)

Figure A.4.: Schematic of second process part. a) Gate metalization by electron beam evaporation. Gate connector pad and finger tips protrude over the mesa edge onto the GaN buffer. b) Contact pad deposition. c) SiN_x device passivation deposited by PECVD.

Contact Pads

The contact pads simplify the electrical measurements of the devices. They consist of Ni/Au with thicknesses of 50/200 nm, respectively (same as gate metalization) patterned by an image reversal lithography and lift-off. The pads are connected to the ohmic contacts as well as the gate connector pad. They protrude over the mesa edge onto the GaN buffer, which is depicted in Fig A.4(b).

Surface Passivation

The surface passivation is employed to shift the actual surface further away from the 2DEG and to passivate AlGaN surface states. Both helps in mitigating charge trapping effects and the accompanying current collapse (see section 2.6.2). The passivation consists of silicon nitride with a non-perfect stoichiometry (SiN_x) and is deposited by a PECVD on the whole sample. Prior to the deposition, the surface is cleaned and conditioned by an ammonia (NH_3) plasma [179]. After the deposition, the patterning is performed by lithography and a subsequent CF_4/O_2 dry-etching step to expose the contact pads. This step and the finished device are shown in Fig. A.4(c).

A.5. Device Geometries

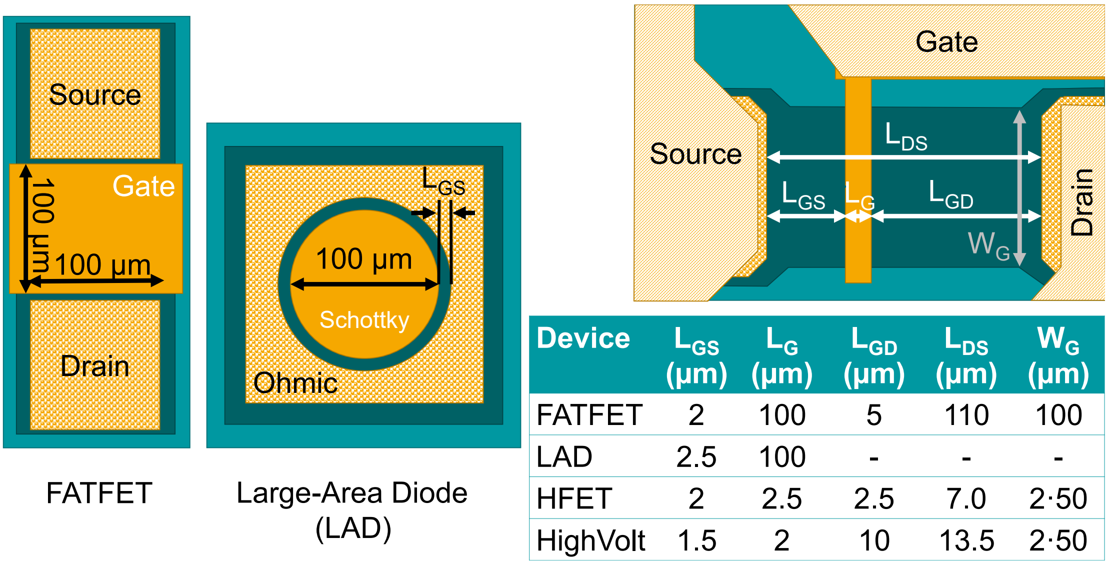
A short overview of the devices geometries, which are used throughout this work will be given. A top view of the different devices as well as a table of the geometry parameters are shown in Fig. A.5.

The **FATFET** is an HFET with a very long gate $L_G = 100\,\mu m$ which is equal to the gate width $W_G = 100\,\mu m$. The ohmic contacts are located on a mesa without any contact pads. Therefore, the contacts are not protruding over the mesa edge. The gate metalization is slightly overlapping to ensure a complete pinch-off of the 2DEG at $V_{GS} = V_{th}$.

The **large-area diode (LAD)** is a lateral Schottky diode which is entirely located on top of a single mesa. A Schottky contact with a diameter of 100 µm is surrounded by an ohmic contact. The distance between contacts is 2.5 µm.

The **HFET** are typically double-finger transistors with a geometry of L_{GS} / L_G / L_{GD} / L_{DS} / W_G of 2 / 2.5 / 2.5 / 7.0 / $2 \cdot 50$ µm, respectively. The contact pads are connected to the ohmic contacts and protrude over the mesa edge on top of the GaN buffer. The area of the pads on top of the GaN buffer is significantly larger than the active device area.

For the **high voltage HFET** the gate-drain distance L_{GD} is increased from 2.5 µm to 10 µm. Due to the higher distance, the maximum operation voltage is increased but at the cost of an increased ON-resistance. This trade-off is commonly expressed through the Baliga figure-of-merit [180].



FATFET

Large-Area Diode (LAD)

Device	L_{GS} (µm)	L_G (µm)	L_{GD} (µm)	L_{DS} (µm)	W_G (µm)
FATFET	2	100	5	110	100
LAD	2.5	100	-	-	-
HFET	2	2.5	2.5	7.0	$2 \cdot 50$
HighVolt	1.5	2	10	13.5	$2 \cdot 50$

Figure A.5.: Geometries of the different devices used throughout this work. Shown are a FATFET, a large-area diode (LAD) and a zoomed-in image of the active region of an HFET with the respective distances.

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3. G. Lükens, H. Yacoub, H. Kalisch, A. Vescan, "Investigation of plasma treatments on the AlOx/AlGaN interface after recess etching," *39th Workshop on Compound Semiconductor Devices and Integrated Circuits*, 2015.

Acknowledgements

Ich möchte ich mich bei allen Personen bedanken, mit deren Unterstützung diese Arbeit erst ermöglicht wurde. Insbesondere danke ich

- Prof. Dr.-Ing. Andrei Vescan, der mir die Möglichkeit gegeben hat, diese Arbeit im Lehr- und Forschungsgebiet Technologie der Verbindungshalbleiter durchzuführen und weiterhin immer genug Freiraum gegeben hat, meine eigenen Ideen und Projekte umzusetzen.
- Prof. Dr.-Ing. Max Christian Lemme für die Übernachme des Zweitgutachtens.
- Dr. Holger Kalisch für seinen unermüdlichen Einsatz in der Qualitätssicherung diverser Texte und Vorträge.
- Dr. Herwig Hahn für die Einführung in das experimentelle Arbeiten und die Betreuung meiner studentischen Abschlussarbeiten.
- Meinen langjährigen Bürokollegen, Dr. Hady Yacoub und Thorsten Zweipfennig, für die fachlichen und als auch die nachmittaglichen Gespräche.
- Simon Kotzea für die sehr gute fachliche Zusammenarbeit und bei der Instandhaltung des Labors, Jan Gruis für den steten Support in der Informations- und Reinraumtechnologie, Annika Grundmann für die Hilfe bei der Sortierung meiner Gedanken in Schriftform.
- Frank O. Jessen für die stetige Versorgung mit Kaffee und seinem Einsatz in der Reinraumtechnologie.
- Sonja Buchholz-Trappe und Gabriele Nogueira-Glenski für ihre Unterstützung in der Lithographie.
- Der gesamten Arbeitsgruppe für das hervorragende und freundliche Arbeitsklima!