Optimal Transistor Dimensioning in T-Type Topology for Reduced Quasi-2-Level Switching Loss

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Abstract

A quasi-2-level switching T-type topology reduces hard-switching loss compared to half-bridges, but requires more semiconductor area. This work shows that the middle transistor can be dimensioned smaller than the high/low-side transistors, which further reduces both the switch node capacitance and switching loss. The paper also presents a scalable transistor model, which is used in simulations of inductive-load hard-switching to determine switching losses and reveal a loss-optimal transistor dimensioning. Furthermore a double pulse setup (600 V-rated GaN HEMTs in a T-type topology) with 2 ground referenced shunts is proposed to determine switching energy of middle and low side transistors simultaneously. To verify the concept of loss-optimal transistor dimensioning in Q2L T-type topology, switching energy was measured at 200 V and 1 A, with the middle transistors area reduced by half compared to high/low side, resulting in a measured reduction from 4.44 µJ to 2.18 µJ (-51%) which is similar to the simulated reduction (2.39 µJ to 1.43 µJ, -40%). This method allows reduction of Q2L switching-loss with optimal transistor area and can be used for a wide range of applications.

1 Introduction

The increasing environmental demands to reduce fossil fuel consumption and its related impacts have prompted a global focus on enhancing the efficiency and power density of electrical energy conversion[1]. One method to achieve higher efficiency in power electronics is the reduction of switching losses compared to conventional 2-level half-bridges by the use of Quasi-2-Level (Q2L) switching [2][3]. T-type [4] topologies are currently in the research focus because they can benefit from emerging monolithic bidirectional GaN switches [5][6]. The T-type topology can also be used in a wide range of applications like traction inverters [7], photovoltaic grid inverters, PFC rectifiers [8] and electrocaloric heat pumps [9][10][11].
However, the additionally required semiconductors reduce the resource-efficiency of the resulting converter system compared to 2-level half bridges. The approach of this work is to reduce the semiconductor dimensioning (area, which is inversely related to on-state resistance) of the middle transistor compared to the high/low-side transistors. This will reduce the switch-node capacitance and thus the switching loss. This work investigates how the resulting switching loss depends on the middle-to-outer transistor dimensioning (factor k), switched current, and the delay between the Q2L voltage steps. Figure 1 shows the investigated T-type topology (3-level), where the middle level is realized by two discrete common-drain connected GaN HEMTs. By Q2L switching, first only half of the input voltage is switched through a hard-switching turn-on transition by the middle transistor

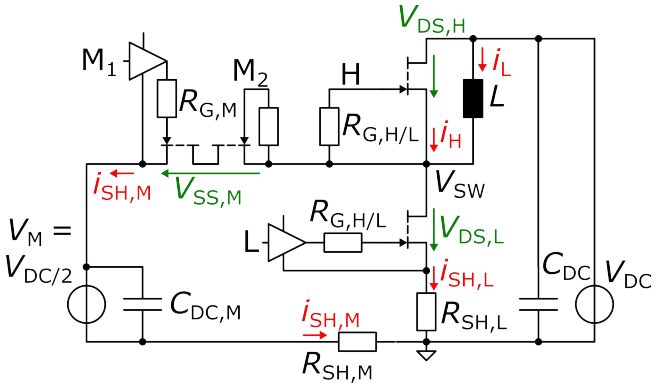

Fig. 1: T-type topology for Q2L switching and energy measurement with two shunts $R_{\mathrm{SH,M}}$ and $R_{\mathrm{SH,L}}$.

M_1 (see Fig. 2). Then, after a delay time t_D, the

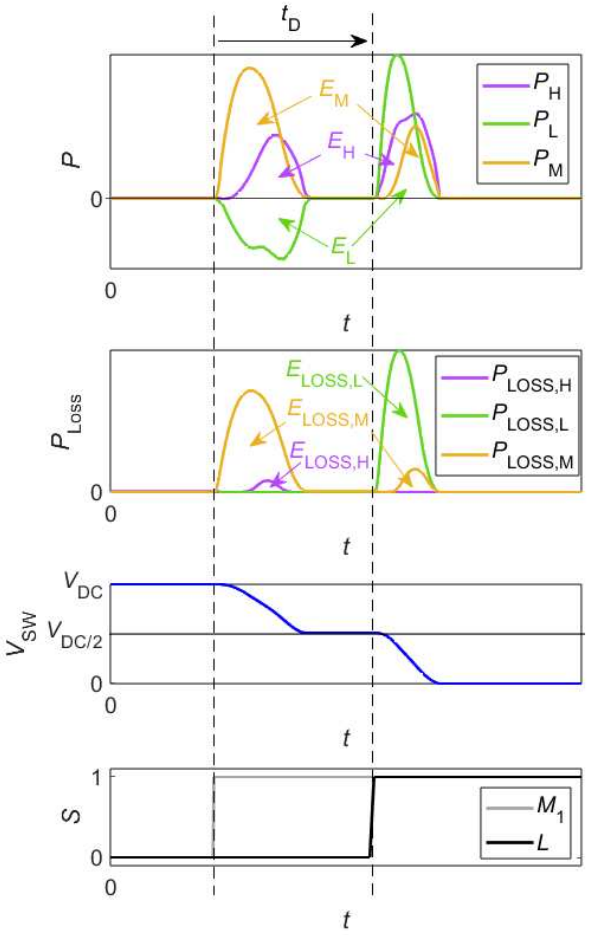

Fig. 2: Time delayed turn on (t_D) of transistors M_1 and L with switch node voltage (V_SW), switching power (P_H, P_L, P_M) and energy (E_H, E_L, E_M) of transistors with corresponding switching losses $P_\mathrm{LOSS,H}$, $P_\mathrm{LOSS,L}$, $P_\mathrm{LOSS,M}$, $E_\mathrm{LOSS,H}$, $E_\mathrm{LOSS,L}$, $E_\mathrm{LOSS,M}$.

low-side transistor T_L is switched through a hard-switching turn-on transition. High H and mid M_2 transistors are continuously in the off-state during the investigated switching transitions. The switching power of low side ($P_\mathrm{L} = I_\mathrm{SH,L} \cdot V_\mathrm{DS,L}$) and middle ($P_\mathrm{M} = I_\mathrm{SH,M} \cdot V_\mathrm{SS,M}$) transistors is determined by using the shunts $R_\mathrm{SH,L}$ and $R_\mathrm{SH,M}$. The switching energy for low- and middle transistor is defined as $E_\mathrm{L} = \int_{t_1}^{t_2} P_\mathrm{L}\,dt$ and $E_\mathrm{M} = \int_{t_1}^{t_2} P_\mathrm{M}\,dt$ whereby t_1 and t_2 describe the time span of a full turn-on transition of transistors L and M_1 (V_SW decreases from $\approx V_\mathrm{DC}$ to $\approx 0\,\mathrm{V}$). Since a transistor's output-capacitance related switching loss is at least proportional to the square of switched voltage, Q2L switching over two steps will theoretically half the minimum switching loss (at low switched current). Switching power losses are described by $P_\mathrm{LOSS,L} = I_\mathrm{CH,L} \cdot V_\mathrm{DS,L}$ (respective $P_\mathrm{LOSS,M} = I_\mathrm{CH,M} \cdot V_\mathrm{SS,M}$ for middle path) with $I_\mathrm{CH,L}$ and $I_\mathrm{CH,M}$ as channel currents that lead to switching losses $E_\mathrm{LOSS,L} = \int_{t_1}^{t_2} P_\mathrm{LOSS,L}\,dt$ (low-side), $E_\mathrm{LOSS,M} = \int_{t_1}^{t_2} P_\mathrm{LOSS,M}\,dt$ (middle path). Calculations of power (P_H)/energy (E_H)/losses ($P_\mathrm{LOSS,H}$, $E_\mathrm{LOSS,H}$) for high-side transistor are similar to those of low-side by using I_H, $V_\mathrm{DS,H}$ and $I_\mathrm{CH,H}$ instead of $I_\mathrm{SH.L}$, $V_\mathrm{DS,L}$ and $I_\mathrm{CH,L}$. For real setups, the additional output capacitance of the additional middle transistors however will add to the switch node capacitance. Dimensioning of the middle transistor is a trade-off: A smaller and higher-resistance transistor will reduce the additional capacitance, but also slow down the switching, and also be ultimately limited when it cannot carry the current any more. This work investigates the dimensioning of the ratio $k = \dfrac{R_\mathrm{DS,H/L}}{R_\mathrm{DS,M1/2}}$ between the on-resistances $R_\mathrm{DS,H/L}$ of the high/low-side transistors (H, L) and the middle transistors (M_1, M_2).

2 Methods

2.1 Simulations

2.1.1 Scalable transistor model

A common problem in determining switching losses by simulation is the lack of availability of transistors models with variable (scalable) R_DS. Often, simulation models are only available for the transistors that are actually commercially available, and these only cover a few discrete values of R_DS. In the following, a way to circumvent this problem is presented using a scalable transistor model, which scales the transistor based on an available SPICE model.

A. Electrical modeling

A 600 V GaN HEMT level three (L3) SPICE model (GaN_LTspice_GS-065-004-1-L_L3V3P1.lib from GaN Systems) has been modified in LTSpice (see Fig. 3, inner model) to make it scalable. Package stray inductances of the inner model were set to zero for simplification. The basic idea is to use this available SPICE model (inner model) and build an outer model around it so that it behaves scalable at the outer terminals. Scaling takes place with the aid of current-controlled current sources that amplify the current of the inner transistor model. For $k = 1$ the entire current flows into the inner model

(used for H/L-transistors). Otherwise, current is delivered ($k < 1$) or absorbed ($k > 1$) by the outer model (used for scaling $R_{\mathrm{DS,M1/2}}$). The turn on resistor (gate) for high- and low side is set to a fixed value (15 Ω). To scale the gate resistance of middle transistors $R_{\mathrm{G}} = \frac{R_{\mathrm{G,1}}}{k}$ is used, where $R_{\mathrm{G,1}} = 15\,\Omega$ is the nominal gate resistance for the unscaled ($k = 1$) inner transistor model.

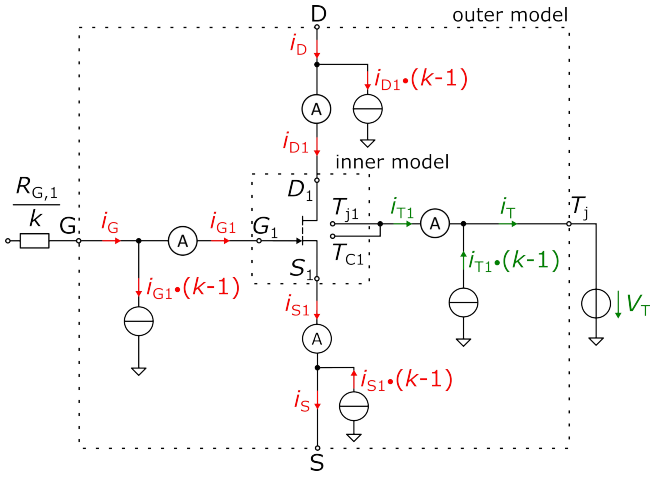

Fig. 3: By factor k scalable transistor model.

B. Thermal modeling

The SPICE model used (see electrical modeling) also includes a thermal model (based on a Cauer model). For calculation of the scaled switching losses, the heat (complementary green current in Fig. 3) must flow from inner junction T_{j1} to outer junction T_{j} and also has to be scaled. To avoid heat flow from T_{J1} to case T_{C1} - which would occur because of the Cauer model - the case and junction connections are short-circuited in this work. Thereby, the externally measurable heat flow (current in the electrical equivalent circuit) from the T_{J} is equivalent to the instantaneous electrical power loss of the transistor. This model approach based on a L3 SPICE model enables direct power loss simulation and does not require additional model equations as in [12]. The heat-scaling is realized similar to the electrical scaling already described. The output of the outer model is set to room temperature (25 °C) which enables heat flow from T_{J1} to T_{J}. As a result heat is supplied instantaneous to T_{J} (which describes all scaled losses of the transistor model). At the thermal output (connector T_{J}) losses are calculated for all transistors (exemplified here for the low-side transistor) as $P_{\mathrm{LOSS,L}}(electr.) = P_{\mathrm{LOSS,L}}(therm.) = I_{\mathrm{T}} \cdot 1\,\mathrm{V}$ where the junction temperature T_{J} equals the case temperature and all thermal capacities are deactivated.

2.1.2 Determination of switching losses

To determine the switching losses the scalable transistor model of previous section was used in T-type topology (Fig. 1). The inductor was replaced by current source. The switching energy E (derived from the drain-source terminal voltage and drain currents), which includes the change of stored energy in the transistor's parasitic capacitances, and the actual switching loss E_{LOSS} (derived directly from the thermal output of the transistor as described in previous chapter) was extracted for each transistor and summed up (E_{LOSS} = $E_{\mathrm{LOSS,H}}$ + $E_{\mathrm{LOSS,M}}$ + $E_{\mathrm{LOSS,L}}$).

Switching losses depend on k, I_{L} and t_{D}. To determine the minimum switching loss a sweep of t_{D} for $I_{\mathrm{L}} = 0 \ldots 2\,\mathrm{A}$ and fixed k is carried out in a first step as shown in Fig. 4 (with $V_{\mathrm{DC}} = 200\,\mathrm{V}$ and $V_{\mathrm{M}} = \frac{V_{\mathrm{DC}}}{2} = 100\,\mathrm{V}$). Lowest switching losses in the range of $I_{\mathrm{L}} = 0...2\,\mathrm{A}$ can be identified for $t_{\mathrm{D}} \approx 5...10\,\mathrm{ns}$. High switching losses can be observed in 2L operation ($t_{\mathrm{D}} \leq 0$). Furthermore a wide range of t_{D} for optimal switching losses can be observed, which reduces slightly with increasement of I_{L} (for $k = 0.5$). Increasement of losses for high switching delay is caused by conduction losses in the middle path.

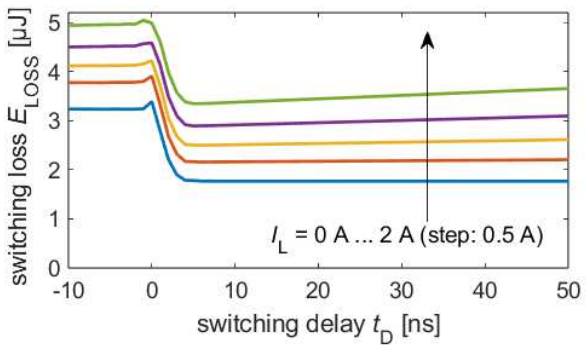

Fig. 4: Simulated turn-on switching losses at $V_{\mathrm{DC}} = 200\,\mathrm{V}$ for middle-to-outer transistor ratio $k = 0.5$ and different delay time t_{D}

Figure 5 shows the simulated hard-switching turn-on energy loss E_{LOSS} for different $k = 0 \ldots 1.5$, with step width of 0.01 and different switched inductor currents between 0 A and 2 A, at 200 V and $t_{\mathrm{D}} = 10\,\mathrm{ns}$. Here, $k = 0$ is used to simulate a conventional 2-level half-bridge as reference (middle

branch removed). For $k = 0.5$ (which was realized as hardware-design), and 1 A, the simulated switching loss was reduced from 3.73 µJ to 2.51 µJ, which is a reduction by -33%. Maximum of switch-

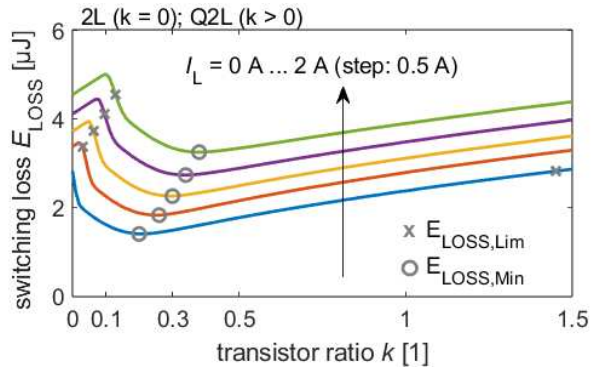

Fig. 5: Simulated turn-on switching losses at 200 V for different middle-to-outer transistor ratios k and a fixed delay $t_{\mathrm{D}} = 10\,\mathrm{ns}$

ing loss reduction for a given current $I_{\mathrm{L}} = 0 \ldots 2\,\mathrm{A}$ and switching delay $t_{\mathrm{D}} = 10\,\mathrm{ns}$ with corresponding optimal transistor ratio k is shown in Fig. 6. At low currents, switching loss reduction is most pronounced. Minimum switching loss $E_{\mathrm{LOSS,Min}}$ for given I_{L} and t_{D} depends on k whereby the optimal ratio k ($k > 0$) increases with I_{L}.

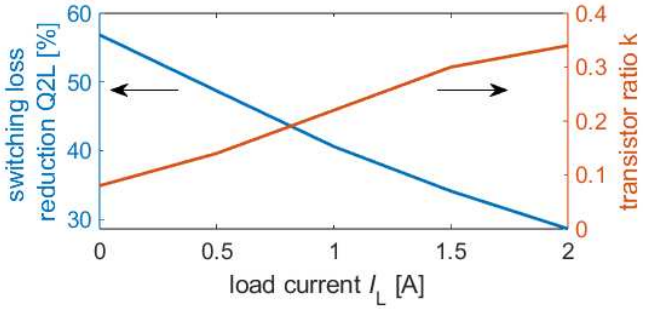

Fig. 6: Maximum switching loss reduction and corresponding optimal transistor ratio k at 200 V with Q2L compared to 2L for $t_{\mathrm{D}} = 10\,\mathrm{ns}$

Switching losses in Q2L are not for all ratios k lower than in 2L-configuration. This method not only allows to find $E_{\mathrm{LOSS,Min}}$ for Q2L depening on I_{L} and k, it also allows to find the transition $E_{\mathrm{LOSS,Lim}}$ where Q2L exhibits lower switching losses compared to 2L and vice versa (see Fig. 5).

2.2 Measurements

A double pulse setup [13] using 600 V class GaN transistors was built (see Fig. 7). Due to the limited availability of GaN transistors, the ratio $k = 0.5$ was experimentally implemented and differs from the theoretical optimal values which was in the range of $k = 0.1 \ldots 0.35$. Therefore, two transistor devices with different on-resistance were selected: GS-065-004-1-L (450 mΩ), and GS-065-008-1-L (225 mΩ). A standard gate driver circuit (also with scaled gate on resistors $R_{\mathrm{G,M}} = 30\,\Omega$ $R_{\mathrm{G,H/L}} = 15\,\Omega$) and a 100 µH inductive load was used. It should be mentioned that due to availability the middle transistors were also 600 V devices, even though 300 V-rated devices would be sufficient. Also, the 200 V operation is below the typical 400 V operation voltage of 600 V transistors. Due to limitations of the used equipment and observed false turn-on of transistors at higher operation voltage, this work carries out all measurements at 200 V.

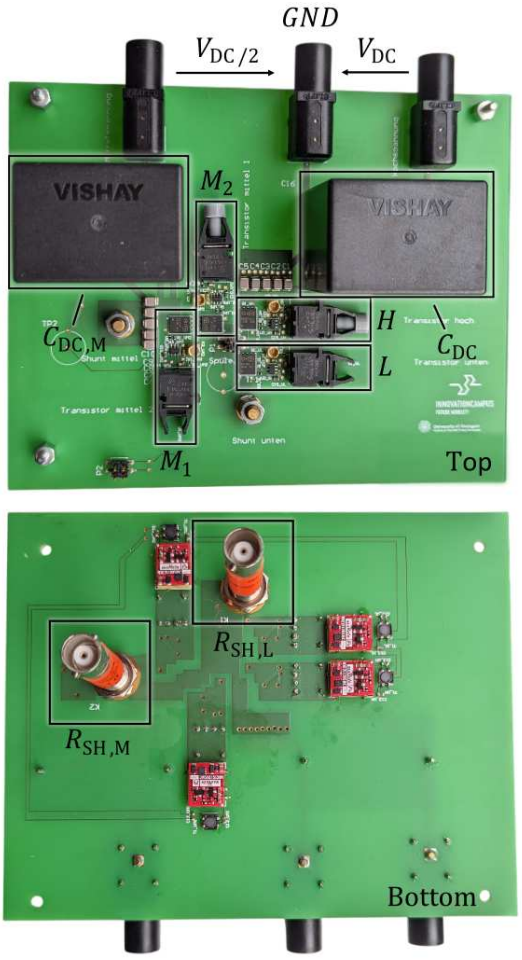

Fig. 7: Photo of the T-type power converter with two shunts $R_{\mathrm{SH,M}}$ and $R_{\mathrm{SH,L}}$

One common problem of non-isolated high bandwidth current measurement in this topology is simultaneously measurement of mid- and low side current, which is necessary for precise switching energy calculation. If the shunt $R_{\mathrm{SH,M}}$ is placed in middle path, no common ground could be used in

non-isolating measurement. To solve this problem $R_{\mathrm{SH,M}}$ was placed as shown in Fig. 1 at the GND node instead of the middle DC voltage. in PCB layout. For high bandwidth current measurement, two coaxial shunts (T&M Research SSDN, 100 mΩ, bandwidth 2 GHz) were used. Both are connected by 2 m coax cables (deskewed) to a 1 GHz oscilloscope, which also measures V_{SW}, V_{M} and I_{L}. For voltage measurements 1 GHz passive probes and a 1 GHz oscilloscope was used. The measurements were carried out at 200 V.

Figure 8 exemplary shows the measured switching transitions (Q2L, 1 A, 200 V, 10 ns), and the calculated instantaneous powers from both shunts, from which then the summed energy is calculated after integration. Figure 8 clearly shows how the time-delayed switching of the M and L transistors results in a 2-step discharging of the switch-node, where during the first step energy is dissipated in the middle transistor (visible as P_{M}, related to $I_{\mathrm{SH,M}}$) and during the second step energy is dissipated in the low side transistor (visible as P_{L}, related to $I_{\mathrm{SH,L}}$).

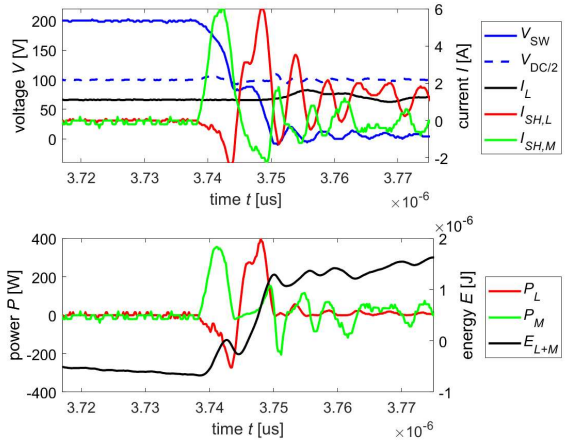

Fig. 8: Measurement results for Q2L at 200 V, 1 A, $t_{\mathrm{d}} = 10\,\mathrm{ns}$, $k = 0.5$

2.3 Validation

In this section, the switching energy E_{ON} and not the switching loss E_{LOSS} is shown and discussed, because in the double pulse test only the switching energy can be directly measured. Figure 9 compares the experimentally measured switching energy and the simulated energy as a function of current, and for both, the conventional 2L switching, and the Q2L switching. The switching energy E_{ON} includes the switching energy of low-side and mid-transistors ($E_{\mathrm{ON}} = E_{\mathrm{L}} + E_{\mathrm{M}}$) which can be measured by using the 2 grounded shunts. Exemplarily for $I_{\mathrm{L}} = 1\,\mathrm{A}$ the switching energy results in a reduction from 4.44 µJ to 2.18 µJ (-51%) for measurement and from 2.39 µJ to 1.43 µJ for simulation (-40%, simulated with scaled transistor model in Q2L-T-type topology). The higher switching energy

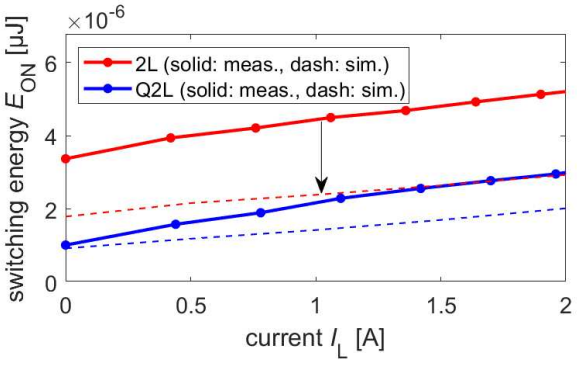

Fig. 9: Simulated and measured switching energy of 2L ($k = 0$) and Q2L ($k = 0.5$) for $t_{\mathrm{D}} = 10\,\mathrm{ns}$

during 2L measurements (compared to simulations) is partly due to parasitic inductances, which are less effective at Q2L switching, and were not included in simulations. For 2L the switching node was not physically disconnected from middle path; instead the shunt $R_{\mathrm{SH,M}}$ was removed. This could lead to additional parasitic capacitance and higher switching energy in measurement. Another influencing factor is uncertainty in deskew which also could lead to errors in reported switching energy. Nevertheless the basic idea of minimizing switching losses by different transistor ratio area (k) for different I_{L} has been proven.

3 Conclusion

Quasi-2-level switching T-type topology can be used to reduce hard switching losses compared to 2-level half bridges. This work demonstrated a method to find the optimal middle-to-outer transistor ratio to minimize the switching losses. Using this work's approach, a T-type topology for Q2L switching can not only be made more energy efficient (less switching loss), but at the same time also more resource efficient (less semiconductor area). The method also can be used to analyze the range of k in which Q2L switching has lower switching loss compared to 2L switching. For non-isolated simultaneously current measurement of the low-side and middle transistor currents, two high bandwidth coaxial shunts were used and placed in a GND-referenced configuration.

In future works switching losses at higher switching

voltage ($\geq 400\,\mathrm{V}$) should be investigated. For analysis of the deviation between measurement and simulation the 2-level half bridge should be physically disconnected from Q2L mid path avoiding influences due to parasitic capacitance (at switching node). Furthermore parasitic inductance should be further minimized in PCB or should be taken into account also in the simulation in order to achieve a better agreement between simulation and measurement. Emerging monolithic bidirectional GaN switches should also be investigated and used in the middle path of the T-type topology with Q2L switching to improve the resource efficiency. The results (optimal transistor dimensioning) should also be used to demonstrate its advantages in case of an actual application.

Acknowledgment

The authors would like to thank the Ministry of Science, Research and Arts of the Federal State of Baden-Württemberg for the financial support of the projects within the InnovationCampus Future Mobility (ICM). In particular: DEMO14 and LAB19.
This work was supported in part by the European Union's Horizon Europe The European Innovation Council (EIC) Pathfinder Challenges 2023 Program under Grant 101161087, project: Cooling with Electrocaloric Polymers (COOLPOL).
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