Fabrication and Characterisation of AlGaN/GaN High Electron Mobility Transistors for Power Applications

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Chapter 1

Introduction

Beside the classical group IV semiconductor materials (Si, Ge, ...) and conventional GaAs based III–V material systems, the III–Nitrides were intensively studied during the last few years. III–Nitrides cover a band gap range from $0.7eV$ for InN to $6.2eV$ for AlN. In comparison to other systems they have a much smaller lattice constant what files them into the group of very high mechanically stable materials (figure 1.1). The wide band gap predicts high breakdown fields. Thanks to these properties, the devices based on III-Nitrides are candidates for possible applications in the field of high–temperature, –power and –frequency electronics. GaN based devices offer a compromise between the high frequency but low power material systems such as InP and the high power but low frequency materials such as SiC (figure 1.2).

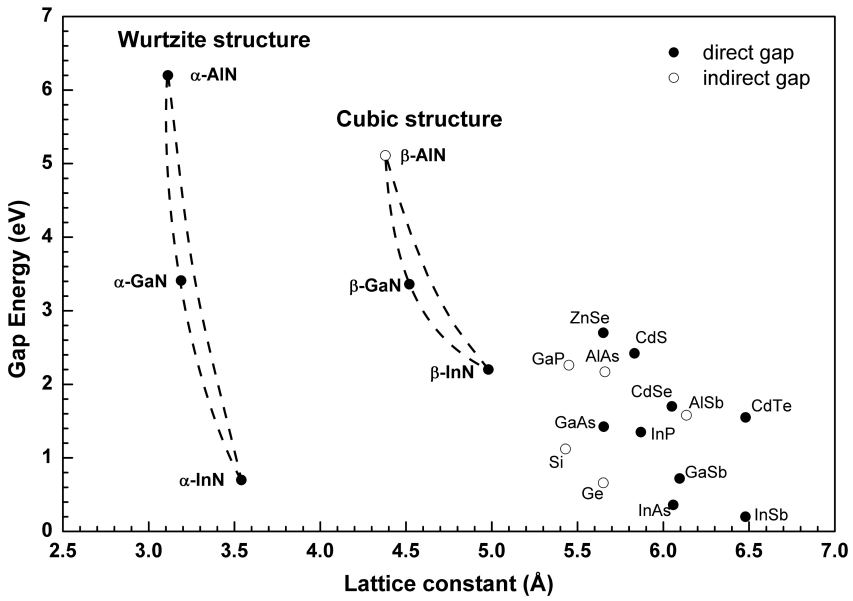


Figure 1.1: Comparison of the band gap versus lattice constant for selected semiconductors.

But not only the electrical behaviour of wide band gap semiconductors are of interest. The driving force that brought the GaN-based material system into research was its optoelectronic behaviour which allows us to produce lasers and photodetectors working in the UV range [1, 2].

This work is divided into three parts. The first one contains an introduction followed by present status analysis and the definition of the main tasks to be accomplished.

The second part covers the theory of gallium–nitrides, explains the formation of heterostructures using AlGaN/GaN including transport mechanisms and transport boundaries, introduces the basic principles of high electron mobility transistors (HEMTs), followed by a discussion of special effects concerning the GaN–based material system.

The final part describes the technological processes and geometrical variations used for device fabrication, outlines the characterisation of fabricated HEMTs, and discusses the measured effects with respect to worldwide published data. The work is closed with a conclusion.

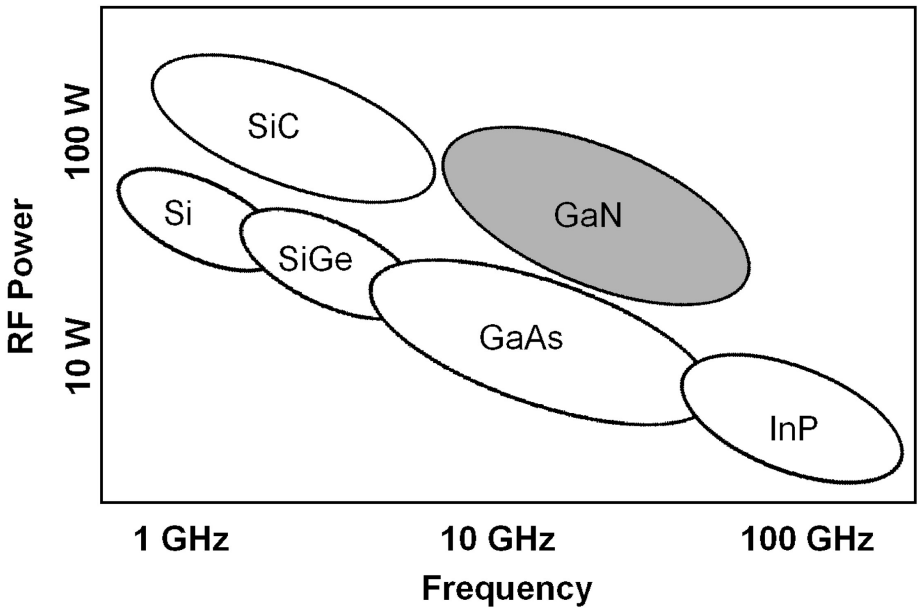


Figure 1.2: Dependence of the rf power on the frequency for different materials.

Chapter 2

Motivation and Present Status of AlGaN/GaN HEMTs

This chapter will motivate this work by discussing the advantages of GaN–based systems in comparison to Si–, InP– and GaAs–based structures. Furthermore, the present status of the main high electron mobility transistor parameters is summarised. Collected data will provide better orientation in worldwide published results.

2.1 Motivation

Advantages of AlGaN/GaN heterostructures originate in the Gallium Nitride material. Beside this, the formation of 2DEG[1] based on polarisation effects makes the AlGaN/GaN system very attractive for research. Due to the strong gradient of the polarisation at the AlGaN/GaN interface, the 2DEG sheet densities are 3 to 10 times higher in comparison to GaAs– and InP– based structures (see table 2.1). To reach fast transport properties, the low–field mobility of 2DEG, the peak velocity of the bulk, and the bulk saturation velocity are desired to be high. The AlGaN/GaN with its comparably high peak velocity and 3 times higher saturation velocity (see table 2.1) in comparison to GaAs– and InP–based heterojunctions is major of interest in spite of its smaller low–field mobility.

As well as the quality of the AlGaN/GaN heterostructure also the used substrate influences the device parameters. Nowadays, frequently used are sapphire, Si, and SiC substrates, but the first native AlN and GaN substrates have been introduced also. Figure 2.1 roughly describes the substrate influences. It shows that usage of the native substrate results in the defect density of $10^2\,\mathrm{cm}^{-2}$ to $10^5\,\mathrm{cm}^{-2}$ in active region in contrary to non–native substrates where the active region defect density is much higher ($10^{10}\,\mathrm{cm}^{-2}$). Detailed substrate description is given in chapter 3.

[1] Two dimensional gas

Heterojunction (barrier/channel)	**ΔE_C [eV]**	**2DEG sheet concentration n_s [$\times 10^{12} cm^{-2}$]**	**Low-field mobility [cm^2/Vs]**	**Peak velocity [$\times 10^7 cm/s$]**	**Saturation velocity [$\times 10^7 cm/s$]**
$Al_{0.3}Ga_{0.7}As/GaAs$	0.22	1.5	8000	2.0	0.8
$Al_{0.25}Ga_{0.75}As/In_{0.2}Ga_{0.8}As$	0.36	3.0	7000	2.3	0.7
$In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$	0.52	4 - 5	10000	2.6	0.7
$Al_{0.3}Ga_{0.7}N/GaN$	**0.42**	**10 - 15**	**1400**	**2.5**	**2.0**
Si	–	–	700	1.0	1.0
4H SiC	–	–	600	2.0	2.0

Table 2.1: Comparison of heterojunction parameters [70].

New record results are published frequently, indicating the steady improvement of the growth and processing technology of GaN–based HEMTs. But what is the main reason for such a high GaN interest during the last few years? I can determinate three main reasons:

1. Due to very high peak velocity and good low–field mobility of AlGaN/GaN the frequency limits of GaN–based HEMTs are high. (see figure 2.2).

2. AlGaN/GaN HEMTs have a high breakdown voltage (breakdown field of GaN is about one order of magnitude higher than in other III–V semiconductors) and very large sheet carrier concentration of the 2DEG and thus are predetermined for very high output power. The comparison of published output power data of AlGaN/GaN with other material systems is depicted in figure 2.3.

3. Due to the big band gap of GaN–based systems (tunable from $3.4eV$ to $6.2eV$) it is an appropriate candidate for fabrication of lasers and detectors working in UV

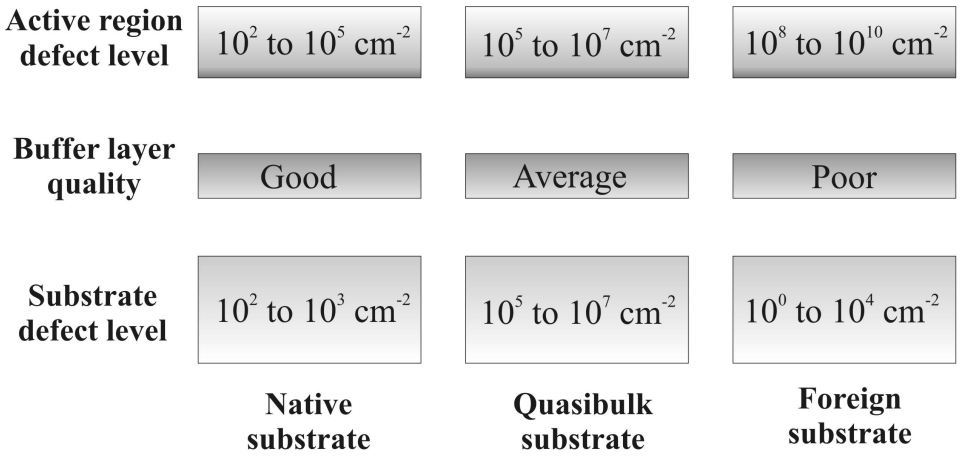


Figure 2.1: Dependence of the defect level on the substrate [71].

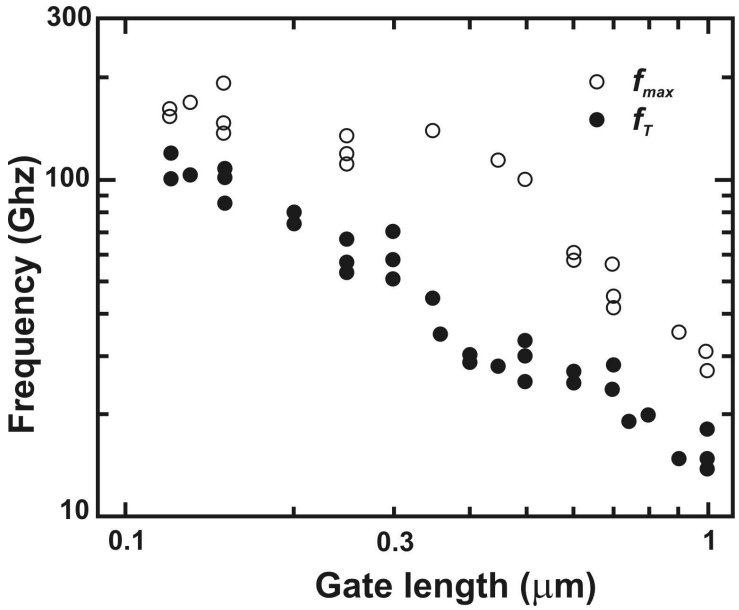


Figure 2.2: Cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}) of AlGaN/GaN HEMTs as a function of the gate length [70].

range.

GaN–based devices are able to work in the frequency range above 100 GHz (see figures 2.2 and 2.3) and reach output power of above 10 W/mm. Using these properties we are able to build very small and powerful devices what is nowadays one of the most significant industry requirement.

But there are still open questions concerning AlGaN/GaN heterostructures, which are not answered yet. Often discussed is the current collapse (or dc/rf dispersion) [72–75], appropriate surface passivation [65,66,77,79,80], the source of electrons in 2DEG [70], or usage of field plate technology [81,82,85,87–89].

This work should help to find answers on the given open questions. Furthermore, improvement possibilities of static, small–signal, and large–signal properties will be investigated and the origin of still not well understood effects mentioned above will be discussed.

2.2 GaN-based HEMTs in numbers

The growth techniques and processing technologies have been rapidly improved since the first HEMT on AlGaN/GaN heterostructure with the saturation current of $I_d^{sat} = 60\,mA/mm$ and extrinsic transconductance of $g_m = 27\,mS/mm$ was introduced by Khan *et al.* in 1994 [42]. The most published data summarised in this work use non–native substrates mentioned in the previous section (Si, SiC, sapphire). The presented overview

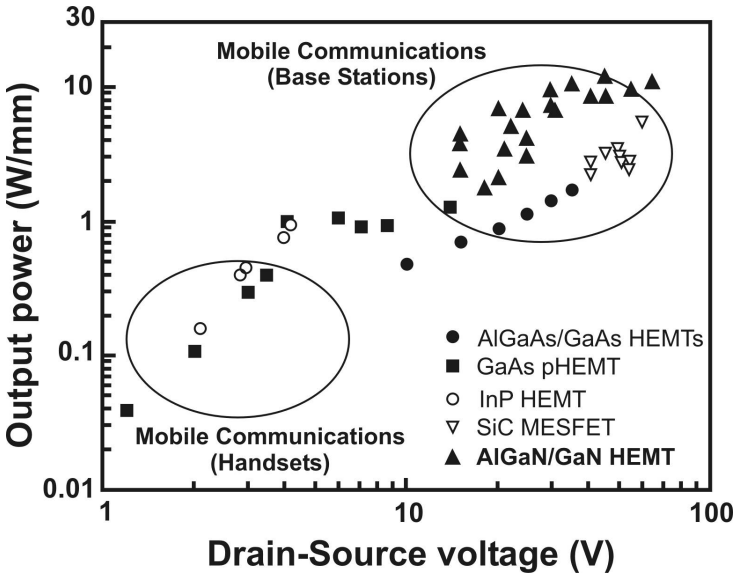


Figure 2.3: Output power of AlGAN/GaN HEMTs as a function of drain–source bias [70].

shows the best values found in literature. Furthermore, the summarised data are divided according the used channel length. Nowadays, the channel length is usually less than one micrometre depending on the application.

High boundary frequencies are reached using small gate lengths. A transistor with the gate length of $0.12\,\mu m$ was introduced by Lu *et al.* [60]. The maximum cut off frequency of $f_T = 101\,GHz$ and the maximum frequency of oscillations of $f_{max} = 155\,GHz$ were reported. The device was fabricated using AlGaN/GaN layer structure grown on SiC substrate. The saturation current of $1.19\,A/mm$ and the extrinsic transconductance of $217\,mS/mm$ were reported.

Devices using sapphire substrate demonstrated high boundary frequencies f_T and f_{max} of $67\,GHz$ and $102\,GHz$ comparable to those reached with SiC–based devices, respectively [63]. The device showed output power of $4.2\,W/mm$ measured at $10\,GHz$.

To compare these results with HEMTs fabricated on the silicon substrate, devices with the same gate length of $0.25\,\mu m$ were reported by Behtash *et al.* showing the saturation current of $1.1\,A/mm$ and $g_m = 240\,mS/mm$. The output power at $2\,GHz$ was reported to be $6.6\,W/mm$. The boundary frequencies of $f_T = 27\,GHz$ and $f_{max} = 81\,GHz$ were presented [43].

The published properties of HEMTs for high power applications profit from the gate length of $0.3\,\mu m$, $0.5\,\mu m$, and $0.7\,\mu m$ [46–48]. Used structures were growth on the SiC substrate due to better thermal conductivity and higher dissipating power discussed in chapter 3. The maximum output power of $P_{out} = 10.7\,W/mm$ at $10\,GHz$ was reported [46].

The device was biased at $V_{ds} = 45V$ what means that in class A operation the breakdown voltage was higher than $90V$. The reported dependence of the output power on the drain-source voltage shows the saturation of the output power at $V_{ds} = 40V$. These excellent results were reached due to high breakdown voltages of fabricated devices. The influence of the drain-source distance on the breakdown voltage was studied by Vertiatchikh *et al.* and shows a strong dependence [48].

In order to reach best performances of fabricated devices, different types of passivation were studied [65, 66]. An improvements, as well as degradations of behaviour were presented after the surface passivation. A Si_3N_4 passivation layer is shown as one of the possible candidate, but also Al_2O_3, SiO_2, Sc_2O_3, and MgO are intensively studied [61, 65–68, 77, 78, 103].

Chapter 3

Material Systems Based on GaN

3.1 Properties of GaN

The III–Nitrides material systems allow us to use the advantage of its wide band gap. Nowadays, Gallium Nitride (GaN) as one of the basic representative of this group is widely studied. In this part, the selected material and electrical properties of GaN will be introduced and compared with the other commonly used semiconductors.

First reports on GaN are dated to the year 1969 [3]. The quality of the epitaxial growth was poor but a high n-doping background concentration of GaN layer was already noticed. The reason of this poor quality was based on the fact that no suitable lattice matched and thermally compatible substrate was known. In spite of an improvement of the growth quality of GaN during the last few years the problem with suitable substrate is still actual. Nowadays, three basic substrates for the GaN growth are used: Sapphire substrate (Al_2O_3); Silicon substrate (Si); and Silicon Carbide substrate (SiC) (table 3.1). The other possibility is to grow the GaN epitaxial layer on the GaN substrate. This provides the lattice and the thermal match, good control of the polarity and no need of interlayers reducing the stress. The obstacle is availability of just very small frameless GaN substrates and its price is too high to use them widely.

Substrate	**GaN**	**Al_2O_3**	**SiC**	**Si**
Thermal conductivity [W/cmK]	1.3	0.5	3.0 – 3.8	1.0 – 1.5
Lattice mismatch [%]	–	-16	+3.5	-17
Resistivity	high	high	high	mediate
Cost	high	low	high	low
Wafer size [inch]	small	6"	3"	12"

Table 3.1: Comparison of substrate properties used for growth of GaN [10].

Sapphire substrates are commonly used substrates for GaN growth with very high resistivity, large area and good quality. A big disadvantage of sapphire is a lattice mismatch to GaN (16 %) and low thermal conductivity. In spite of this is often used because of its low costs.

Silicon substrates offer also a good possibility for GaN growth. Its better thermal conductivity in comparison to sapphire improve properties of material system but the lattice mismatch of 17 % to GaN produce the growth problems resulting to surface cracks. Silicon substrates open possibility to produce GaN–based high power electronics compatible with good developed silicon technology.

Very progressive and in the last few years often used substrate for GaN is Silicon Carbide. Regardless its high costs, SiC has the lattice mismatch just 3.5 % to GaN and the thermal conductivity is in the range of $3.0 - 3.8\,W/cm\,K$.

The substrate choice difficulties affect also the epitaxial growth of the GaN layer. The Gallium Nitride has two thermodynamically stable phases: cubic phase and wurtzite phase (figure 3.1). After few studies the wurtzite phase was find out as a more suitable phase thanks to the less concentration of defects in the GaN layer [12].

The wurtzite GaN is characterised by two lattice constants a and c and by the polarity which can be Ga–faced or N–faced (figure 3.2). The polarity depends on the use of AlN nucleation layer. If a thin nucleation layer is present between the substrate and the GaN film the Gallium Nitride has a Ga–faced polarity (Gallium atoms at the top). The N–face polarity is reached by direct growth of GaN on the substrate [12]. GaN layers are for the device application mostly grown by three methods: Molecular Beam Epitaxy (MBE); Metal-Organic Chemical Vapour Deposition (MOCVD); and Hybride Vapour Phase Epitaxy (HVPE). The properties of grown films depend on used method and will be discussed later.

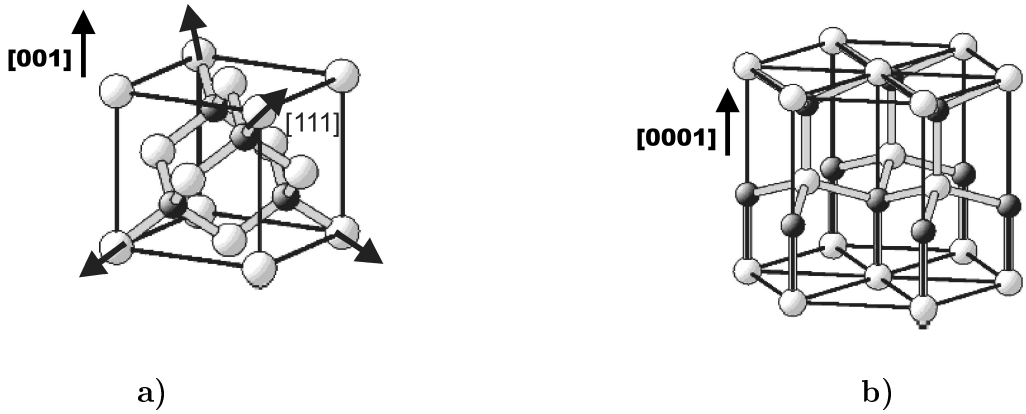


Figure 3.1: Cubic phase (a) and wurtzite phase (b) of GaN epitaxial layer.

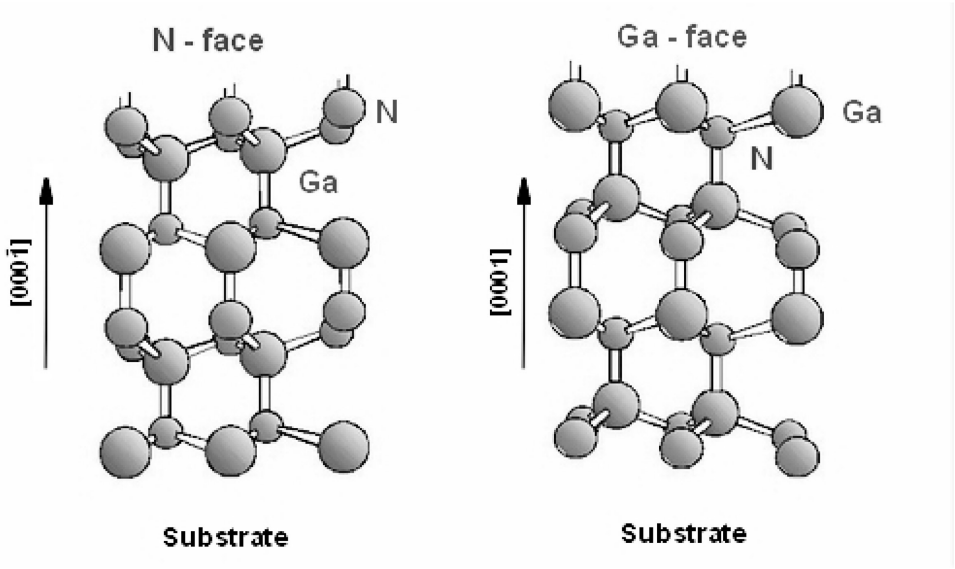


Figure 3.2: N–faced and Ga–faced polarity of GaN [14].

The key electrical and material properties of GaN epitaxial layer are collected in the table 3.2 and are compared to the other semiconductors used for device fabrication. Besides the high thermal conductivity of GaN, that is four times higher than that for GaAs, the breakdown field is much higher in comparison to the GaAs- and Si-based systems. Excellent electron transport properties of GaN enable it to operate in high frequency range. These parameters of GaN-based systems allow us to produce highly improved devices e.g. high electron mobility transistors (HEMTs), Metal-Semiconductor-Metal Diodes (MSM), Lasers etc.

	GaN	**AlN**	**InN**	**SiC**	**GaAs**	**Si**
Band Gap [eV]	3.39	6.20	0.70	3.10	1.43	1.12
Electron Mobility by $300\,K$ [cm^2/Vs]	1000	135	3200	<400	6000	1350
Optical Phonon Energy [meV]	91.2	99.2	89.0	95.0	33.2	62.9
Electron Affinity [eV]	4.20	1.90	–	–	4.07	4.05
Dielectric Constant	8.9	8.5	15.3	9.6	12.5	11.8
Saturation Velocity [$\times 10^7$cm/s]	2.5	1.4	2.5	2.0	1.3	1.0
Breakdown Field [MV/cm]	>2.5	–	–	3.5	0.65	0.6

Table 3.2: Material and electrical properties of GaN in comparison to other semiconductors. [3–10].

3.2 2DEG in AlGaN/GaN Material Systems

High electron mobility transistors take advantage of the two-dimensional electron gas (2DEG) formed in the layer structure. The two-dimensional electron gas can be defined as the charge of carriers fixed in z-axis with the possibility to move just in two directions x and y. This "charge plate" creates the area with very high mobility and sheet concentration of carriers ($2000\,\mathrm{cm^2/V\,s}$ and $\sim 1 \times 10^{13}\,\mathrm{cm^{-2}}$ for AlGaN/GaN heterostructure by $300K$, respectively [13, 14]). This part describes the origin of 2DEG formation in AlGaN/GaN heterostructures.

A heterostructure is the layer system where two semiconductors with different band gaps E_g are grown one on the other (figure 3.3). In the thermodynamical equilibrium, when both semiconductors are "connected" together, the Fermi-level energy (E_F) of the Semiconductor I and Semiconductor II must be in the line what cause the discontinuity in the conductance (E_C) and valence (E_V) band and the band bending [11]. This results in the formation of the triangular quantum well where carriers are fixed in one axis and the 2DEG is formed.

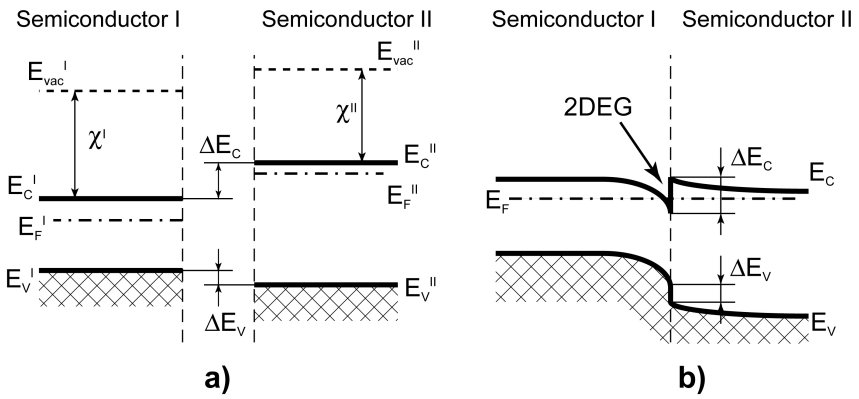


Figure 3.3: Band diagram of the heterostructure formed by lightly n-doped narrow gap semiconductor I and heavily n-doped wide gap semiconductor II divided one from another (a) and together in thermodynamical equilibrium. [11]

The accumulation of the charge in the quantum well in AlGaN/GaN heterostructure is caused by the spontaneous p_{sp} and piezoelectric p_{pe} polarisation in strained AlGaN layer and the spontaneous polarisation in the GaN layer. The total polarisation in AlGaN layer is the sum of the piezoelectric and spontaneous polarisation. The piezoelectric polarisation, present just in the AlGaN layer, originate of the tensile strain in the not matched lattice. If the total polarisation induced charge density is positive, free electrons will tend to compensate the polarisation induced charge resulting in the formation of a 2DEG. For the Ga–face polarity the positive polarisation induced sheet charge is found to be in AlGaN near the bottom GaN/AlGaN interface (see figure 3.4 a) and therefore

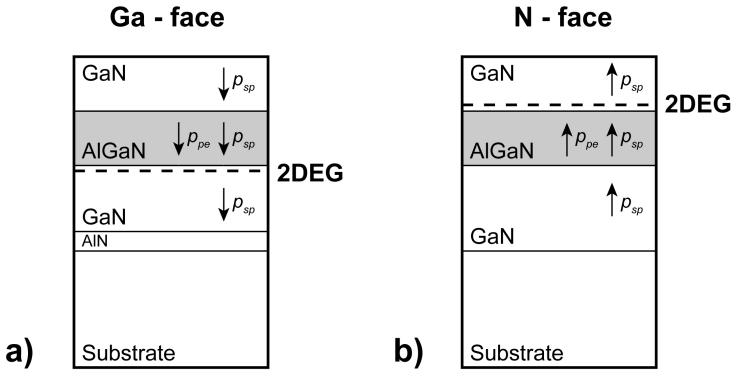


Figure 3.4: Polarisation induced charge in Ga–faced (a) and N–faced (b) GaN/AlGaN/GaN heterostructure.

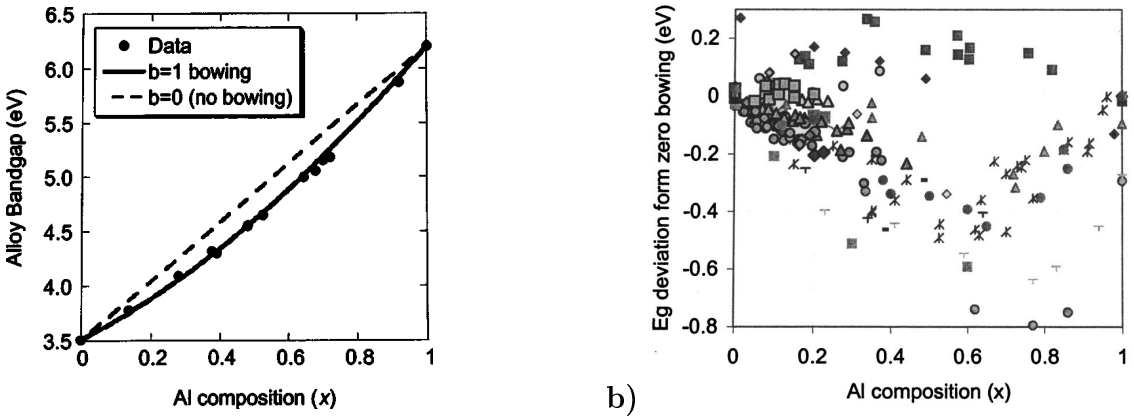
the 2DEG is formed in GaN close to this interface. For the N–face polarity has the total polarisation opposite direction what results to the formation of the 2DEG in GaN close to the top interface (figure 3.4 b) [15].

The reason why the AlGaN/GaN heterostructure is so intensively studied last years is the fact, that the polarisation in the layer system is large enough to form 2DEG with very high sheet carrier concentration without a necessity to have an intentionally doped layer in the system.

The sheet carrier concentration of 2DEG is given by the band offset at the AlGaN/GaN interface and the polarisation induced electric field. This is connected with Al fraction in AlGaN what changes the band gap of the layer and therefore the band offset of the heterostructure. The change of the band gap E_g with changing Al fraction is shown in figure 3.5 [16]. Measured points are fitted using expression of alloy energy band gap: $E_g(x) = E_g^1 x + E_g^0(1-x) - bx(1-x)$, where E_g^0 and E_g^1 are energy band gaps of GaN (3.505 eV at 4 K) and AlN (6.20 eV at 2 K) binary end points, respectively, and b is the bowing parameter. The band gap of $Al_xGa_{(1-x)}N$ was determined using more appropriate photoreflectance measurements in comparison to a photoluminiscence measurements. In spite of that the band gap determination is the main source of any notable inaccuracy what causes that the bowing parameter in $Al_xGa_{(1-x)}N$ is not well established yet as figure 3.5 (b) shows.

3.3 Electron Transport in AlGaN/GaN

The 2DEG formed without an intentional doping modulation in AlGaN/GaN heterostructures offers a novel phenomena that must be taken into account by the determining of the transport properties. However, the electron mobilities in AlGaN/GaN heterostructure are still lower as in AlGaAs/GaAs 2DEG where the mobility is limited by Coulomb



a) b)

Figure 3.5: Dependence of the band gap E_g on the Al fraction in AlGaN (a) and experimental data from published works plotted as deviation from zero bowing (b) [16].

scattering by remote ionised donors [25, 26].

The electron transport in GaAs–based heterostructures is already well known and was used as a base for the investigation of 2DEG transport properties. The scattering sources presented in AlGaAs/GaAs heterostructure as ionised impurities, interface roughness at the barrier, alloy scattering due to penetration of the 2DEG wavefunction into the barrier, and phonons are included also in AlGaN/GaN heterostructure [24]. In addition, the dislocations and charge surface donors and its effects on transport have to be accounted for the GaN–based heterostructure.

Ionised Impurity

As was already mentioned, the separation of the 2DEG from ionised donors in AlGaN/GaN heterostructure is due to the polarisation effect. This separation causes the reduction of the scattering and improving of the electron mobility. Therefore the ionised impurity transport scattering in this system is caused just by the background doping concentration that is usually in the order of 10^{16}cm^{-3}.

Interface Roughness

The interface roughness scattering could be taken to the account if the 2DEG density is high, because the 2DEG tends to shift closer to the interface as the sheet carrier concentration increases. For two-dimensional gas in quantum well with the thickness L has this scattering a characteristic L^{-6} dependence [28].

Alloy Scattering

Alloy disorder scattering originates from the randomly varying alloy potential in the barrier. This scattering influence the mobility in alloy channel heterostructures, but in binary compounds heterostructures occurs as a result of the finite penetration of the 2DEG

wavefunction into the barrier. In AlGaAs/GaAs heterostructures this scattering effect is negligible but in AlGaN/GaN heterostructures, the combination of the large electron mass, the high sheet carrier concentration, and the large alloy scattering potential make this scattering strong.

Phonons

The phonon scattering limits the mobility in 2DEG in the rage of temperatures above $80K$. The transport is affected by potential acoustic phonons, piezoelectric acoustic phonons, and polar optical phonons. By acoustic phonons the scattering is considered as elastic. The polar optical phonon scattering is highly inelastic and the energy of the polar optical phonon for the wurtzite GaN crystal lattice is much higher as by the other semiconductors (see table 3.2). The detailed treatment of this scattering is introduced in [24].

Dislocations

After growing of a GaN epitaxial layer on the substrate (SiC, Al_2O_3, Si), typically $1 \div 100 \times 10^8\,\mathrm{cm}^{-2}$ of dislocations are formed due to the lattice mismatch between the GaN and the substrate [28]. The origin of these dislocations is in the nucleation layer at the interface. The dependence of the mobility affected just by charged scattering dislocations as a function of the 2DEG sheet concentration and the concentration of dislocations is depicted in figure 3.6 [28].

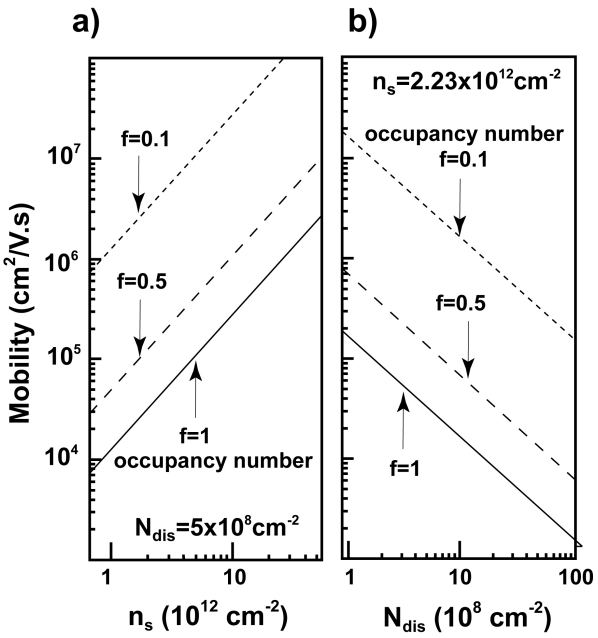


Figure 3.6: dependence of 2DEG mobility (affected by charged scattering dislocations) on the 2DEG sheet carrier concentration (a) and the dislocation density (b). [28]

Charge Surface Donors

The question of the 2DEG electron source becomes out by the creation of the channel with a sheet carrier concentration of $1 \times 10^{13}\,\mathrm{cm}^{-2}$ in the system without an intentional doping. Mentioned background concentration is not enough high to produce a 2DEG with so high sheet density. Therefore, as a possible source of electrons seems to be surface donor states. The creation of the positive surface charge as a dipole with the 2DEG which neutralises the polarisation dipole was introduced by Rizzi *et al.* [27]. The surface donor states will form a source of scuttering identical to a delta–doped remote donor layer and in the same way can be the transport scattering rate treated.

3.3.1 Low Temperature Mobility

Figure 3.7 shows the low temperature mobility as a function of the 2DEG sheet carrier density. The calculation has been done at University of California, USA, by Mishra leaded group and considers with a dislocation density of $5 \times 10^{8}\,\mathrm{cm}^{-2}$, the occupancy number of $f = 0.1$, background density of $10^{16}\,\mathrm{cm}^{-3}$, and surface donor density $n_{surf} = n_s$. The alloy composition is $x = 0.09$ and interface roughness parameters $L = 10$Å, $\Lambda = 2$Å. Every source of scattering was included for the calculation. The temperature at which the calculation has been done was not introduced.

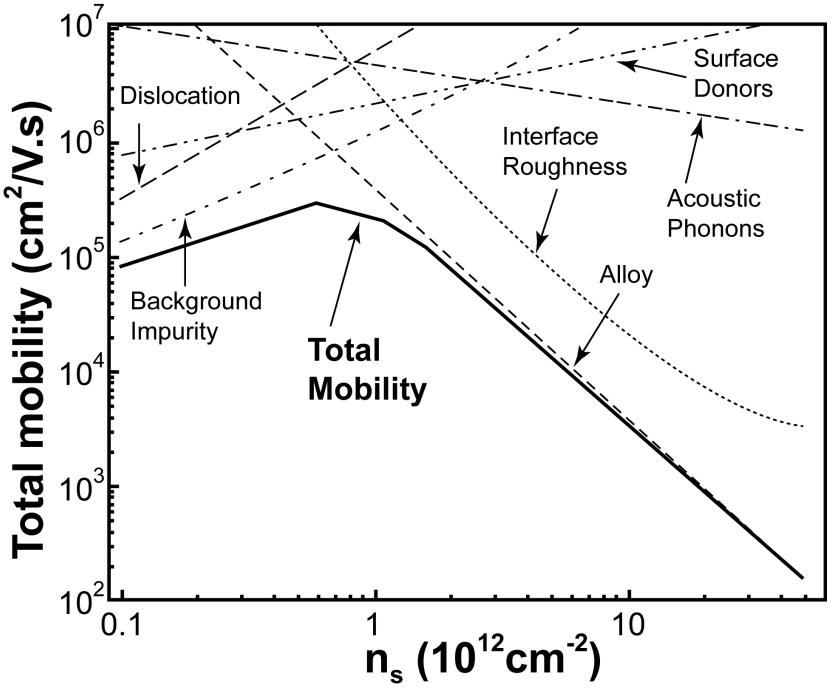


Figure 3.7: Dependence of the low temperature mobility on the sheet carrier concentration of 2DEG [28].

The maximum of total mobility is shown for a low 2DEG sheet densities ($\leq 10^{12} cm^{-2}$) and is bordered by background impurities, surface donors, and dislocations. By higher densities of $n_s \geq 10^{12}\,\mathrm{cm}^{-2}$ dominate alloy scattering or interface roughness scattering, depending on the AlGaN/GaN barrier. It means, that for 2DEG densities above $10^{12}\,\mathrm{cm}^{-2}$ removal of charged defects (dislocations, background impurities, etc) will not improve the total mobility. Therefore the maximum mobilities are predicted for low 2DEG densities $< 10^{12}\,\mathrm{cm}^{-2}$.

3.3.2 High Temperature Mobility

The high temperature mobility ($T > 100K$) is affected by the acoustic and optical phonon scattering as figure 3.8 shows. The comparison of measured and theoretically calculated mobility is included in the figure. The difference at high temperature region is caused by the parallel channel mobility which is added to the 2DEG channel mobility. At temperature Hall effect measurements the contribution of the both mobilities is measured. If the conduction through the parallel channel is negligible, then the measured mobility will reach the theoretical one, that is bordered by polar optical phonon scattering [28].

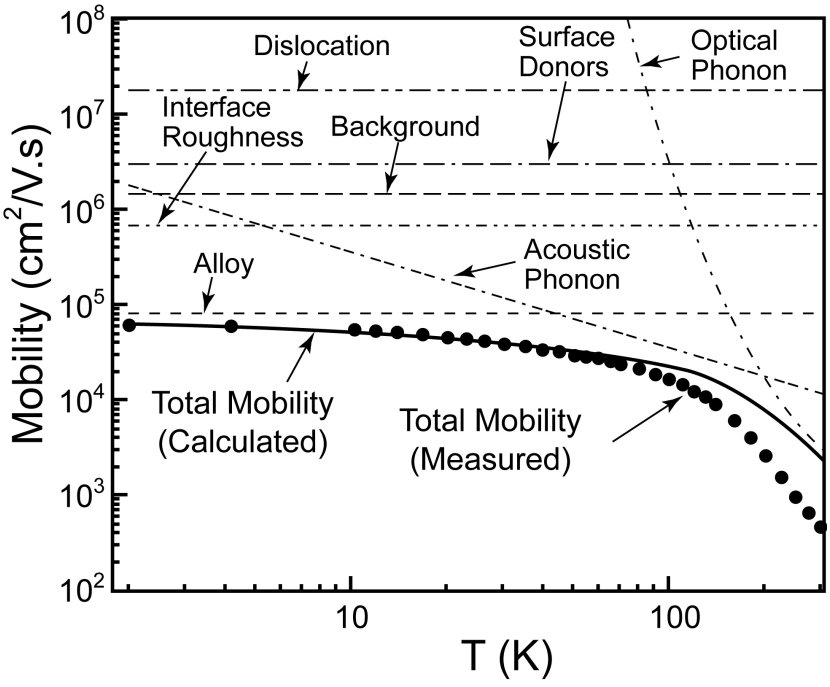


Figure 3.8: Dependence of the 2DEG mobility on the temperature [28].

Chapter 4

High Electron Mobility Transistor

An idea to produce high electron mobility transistor (HEMT) becomes from the fact that the measured mobility of highly doped layers used by MESFET was three times lower at $300K$ as the theoretical value of the mobility [17]. This reduction of mobility was caused by the ionised impurity scattering and therefore in the late 70's was presented an idea of dopant separation from the electrons in the channel. This improvement offers a great increase of the mobility in the channel by unchanged (very high) sheet carrier concentration. The first HEMT was introduced by Mimura *et al.* (1980) and demonstrated a dramatic enhancement in the device current and transconductance.

The same effect is also exploited by HEMTs fabricated on AlGaN/GaN heterostructure and this chapter presents the direct-current (dc), small-signal, and large-signal theoretical behaviours of these devices.

4.1 Basic Principles of HEMTs

The HEMT is a three terminal device (figure 4.1) and is geometrically characterised by the gate length L_g, the gate width W_g, and by the Source-Drain distance S_D. The electron transport provided by 2DEG is between two ohmic contacts: Drain and Source. The current flow is controlled by applying of a bias on the middle Schottky contact (Gate). The control principle is shown in figure 4.2. When zero bias is applied the depletion region under the Schottky contact is just in touch with 2DEG (2DEG is not depleted) and the structure is in the thermodynamical equilibrium (figure 4.2 a). After applying a negative bias on the Gate the depletion region starts to penetrate the 2DEG (conduction band shifts up above the Fermi-level energy, figure 4.2 b) what cause emptying of the 2DEG and "closing" of the channel. The dependence of the 2DEG sheet carrier concentration n_s on the applied gate-source voltage V_{gs} at small drain-source biases can be expressed by equation [17, 18]:

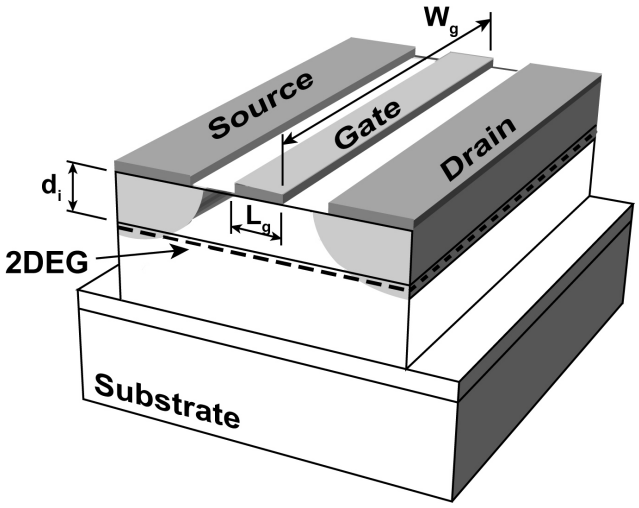


Figure 4.1: Schematic draw of HEMT.

$$n_s = \frac{\varepsilon \cdot (V_{gs} - V_{th})}{q \cdot (d_i + \Delta d)} \tag{4.1}$$

where V_{th} is the threshold voltage, q is the electron charge, d_i and ε are the thickness and the dielectric permeability of the wide band gap semiconductor (in this case AlGaN), respectively, and Δd is the effective thickness of the 2DEG. Equation 4.1 is valid in the above threshold voltage range, where the threshold voltage is defined as the gate voltage when the conductance of the channel drop to the zero:

$$V_{th} = V_{bi} - V_p \tag{4.2}$$

where V_{bi} is the built-in voltage and V_p is called the pinch-off voltage. The capacitance per unit area between the gate and the 2DEG channel can be identified as:

$$c_0 = \frac{\varepsilon}{(d_i + \Delta d)} \tag{4.3}$$

The extrinsic (eq. 4.4) and intrinsic (eq. 4.5) conductivity of the channel per unity area in the linear region are given by [17]:

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi} \cdot (R_s + R_d)} \tag{4.4}$$

and

$$g_{chi} = q n_s \mu_n \frac{W_g}{L_g} \tag{4.5}$$

where R_s and R_d are the series source and drain resistances, respectively, and μ_n is the

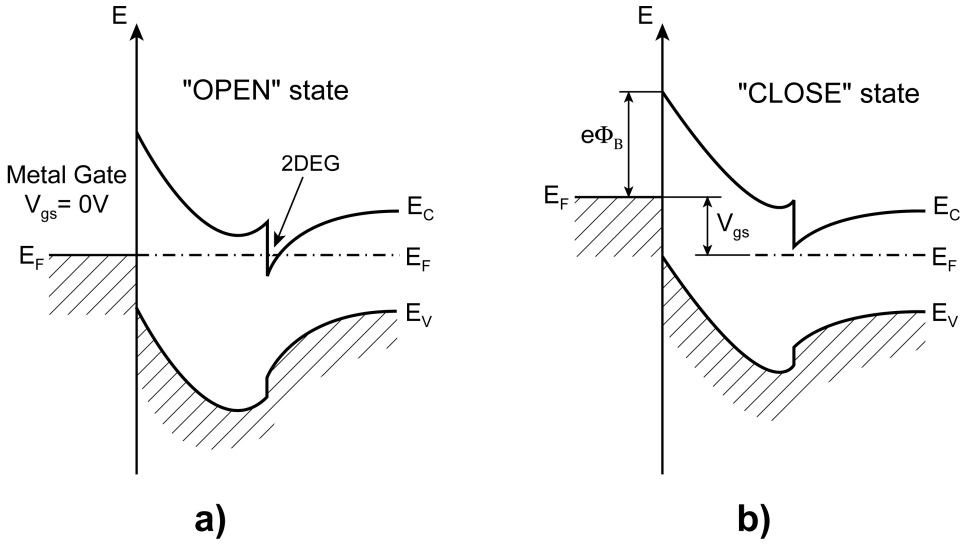


Figure 4.2: The band diagram of HEMT under the gate contact in thermodynamical equilibrium (a) and after applying a negative bias (b) [11].

mobility in the channel. Initially will be assumed no extrinsic source and drain resistances R_s and R_d, and the gate-to-channel capacitance c_0 independent of n_s, then we can rewrite equation 4.1 to the form:

$$qn_s(x) = c_0 \left[V_{gs} - V_{th} - V(x)\right] \tag{4.6}$$

where x is changing along the channel. Using the field-dependent-mobility model where the dependence of the carrier velocity on the lateral electric field is approximated as [18]:

$$\nu = \frac{\mu_0 \mathbf{E}}{1 + \frac{\mathbf{E}}{\mathbf{E}_c}} \tag{4.7}$$

where μ_0 is the low-field mobility independent of the V_{gs} or n_s, and $\mathbf{E}_c$ is a critical field at which the carrier velocity reaches half its value given by:

$$\nu_{sat} = \mu_0 \mathbf{E}_c \tag{4.8}$$

then using equations 4.6 to 4.8 and follow-up integration between the limits $0 < x < L_g$ than the dc drain current is expressed as:

$$I_d \left(1 + \frac{V_{ds}}{L_g \mathbf{E}_c}\right) = \mu_0 c_0 \frac{W_g}{L_g} \left(V_g V_{ds} - \frac{V_{ds}^2}{2}\right) \tag{4.9}$$

where

$$V_g = (V_{gs} - V_{th}) \tag{4.10}$$

If the extrinsic source and drain resistances R_s and R_d will be considered then the following substitution must be included in equation 4.9:

$$V_g = (V'_{gs} - V_{th} - I_d R_s) \tag{4.11}$$

$$V_{ds} = V'_{ds} - I_d(R_s + R_d) \tag{4.12}$$

V'_{gs} and V'_{ds} are the voltages applied to the external gate-source and drain-source terminals of the device.

By assuming the saturation velocity model valid for high electric fields (short channel HEMTs) where ν_s is responsible for the current saturation the saturation current I_d^{sat} can be calculated by applying the condition:

$$\frac{dI_d}{dV_{ds}} = 0 \tag{4.13}$$

and after the simplification can be expressed as [18]:

$$I_d^{sat} = c_0 W_g (V_g - V_{ds}^{sat}) \cdot \nu_{sat} \tag{4.14}$$

where

$$V_{ds}^{sat} = \sqrt{(L_g \mathbf{E}_c) + 2 L_g \mathbf{E}_c V_g} - (L_g \mathbf{E}_c) \tag{4.15}$$

and then the saturation drain current versus gate voltage can be derived:

$$I_d^{sat} = \frac{c_0 L_g W_g}{2} \nu_{sat} \mathbf{E}_c \left(\sqrt{1 + \frac{2V_g}{L_g \mathbf{E}_c}} - 1 \right)^2 \tag{4.16}$$

and simplified to:

$$I_d^{sat} = \frac{\nu_{sat} \cdot \varepsilon}{d} W_g \cdot (V_{gs} - V_{th}) \tag{4.17}$$

For the long channel HEMTs the Shockley model (Constant-electron-mobility model) should be assumed with the low field velocity:

$$\nu(\mathbf{E}) = \mu_0 \mathbf{E} \tag{4.18}$$

and the drain saturation current defined as:

$$I_d^{sat} = \frac{\mu_0 \cdot \varepsilon}{L_g \cdot d} W_g \cdot (V_{gs} - V_{th})^2 \tag{4.19}$$

After these extrapolations and from equations 4.9 and 4.17 (4.19) the final model

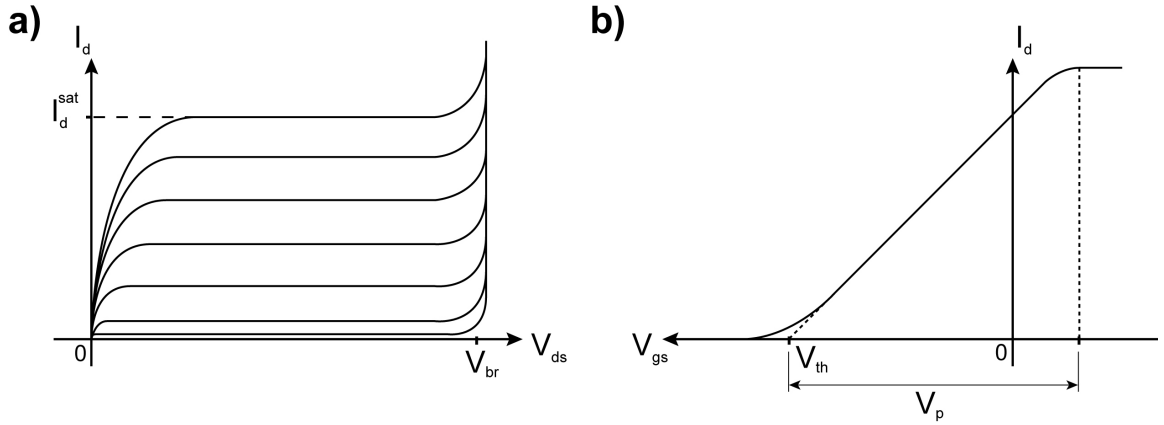


Figure 4.3: Ideal output (a) and transfer (b) characteristics of HEMT.

dependencies of the drain current I_d on the drain-source and gate biases can be plotted. These output characteristics of the transistor are shown in figure 4.3a. The next important parameter which can be derived from output characteristics is the breakdown voltage V_{br}. The breakdown voltage is defined as the drain-source voltage when the electric field in the material reach the critical value $\mathbf{E}_c$ and the breakdown begins as the consequence of the avalanche ionisation in the material. The avalanche ionisation causes increase of the current and therefore the temperature in the material. This increase of the temperature cause the next increase of the current and it repeats till the material breakdown.

4.1.1 Drift Mobility

The drift mobility in the channel can be determined from the intrinsic channel conductivity given by equation 4.5. It is important to stress, that this equation is valid just for the linear region of the HEMT, i.e. for small drain–source biases $(0.1 \div 0.3V)$. Also the influence of the extrinsic parasitics must be minimised and counted out. Then the intrinsic conductance of the channel is calculated as [29]:

$$g_{chi} = \frac{1}{R_{ds} - 2R_c - R_{gs} - R_{gd}} \tag{4.20}$$

where R_{ds} is the total resistance between the drain and source contacts, $2R_c$ is the contact resistance of the drain and source (when the same contact resistance for drain and source is considered), and R_{gs} and R_{gd} are the source–gate and drain–gate resistances, respectively (figure 4.4). The R_c and the sheet resistivity R_{sheet} can be determine from TLM measurements (see chapter 5) and then R_{gs}, and R_{gd} are expressed as:

$$R_{gs} = R_{sheet} \cdot \frac{L_{gs}}{W_g} \tag{4.21}$$

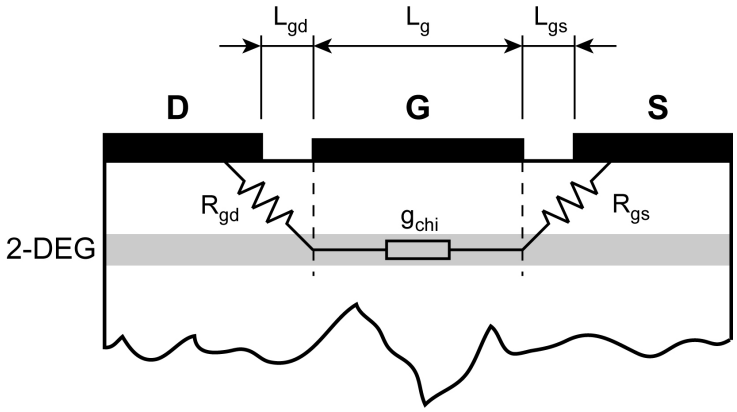


Figure 4.4: Parasitic resistances by determination of the channel conductance.

$$R_{gd} = R_{sheet} \cdot \frac{L_{gd}}{W_g} \tag{4.22}$$

To minimise the influence of these resistances, the large gate transistor must be measured where the condition $R_{gs} + R_{gd} << \frac{1}{g_{chi}}$ is full-filed. From the HEMT theory is also clear, that the conductivity of the channel g_{chi} is dependent on applied gate voltage V_{gs} what has to be considered by calculation.

The sheet carrier concentration of the channel n_s can be determined from the capacitance–voltage characteristic of the gate and then the 2DEG drift mobility is defined as:

$$\mu_n = g_{chi} \cdot \frac{L_g}{W_g} \cdot \frac{1}{q \cdot n_s} \tag{4.23}$$

4.2 Small-Signal Model

The small-signal model of HEMT allows us to evaluate parameters of the device which predict the small-signal behaviour by different frequencies. These parameters show us the possibility of the device to operate at high frequencies or with high switching speeds. To characterise the frequency behaviour two basic parameters are used in praxis: the current gain cut off frequency f_T and the maximum frequency of oscillations f_{max}.

The current gain cut off frequency is defined as a frequency at which the current gain in a common-source configuration becomes unity for short-circuit conditions at the output [19].

The maximum frequency of oscillation is defined as a frequency at which the unilateral power gain of the device goes to unity. A unilateral power gain is the gain from the device in an amplifier made using only non-lossy, passive, and reciprocal matching networks. The f_{max} is also the highest frequency at which an ideal oscillator made using this device

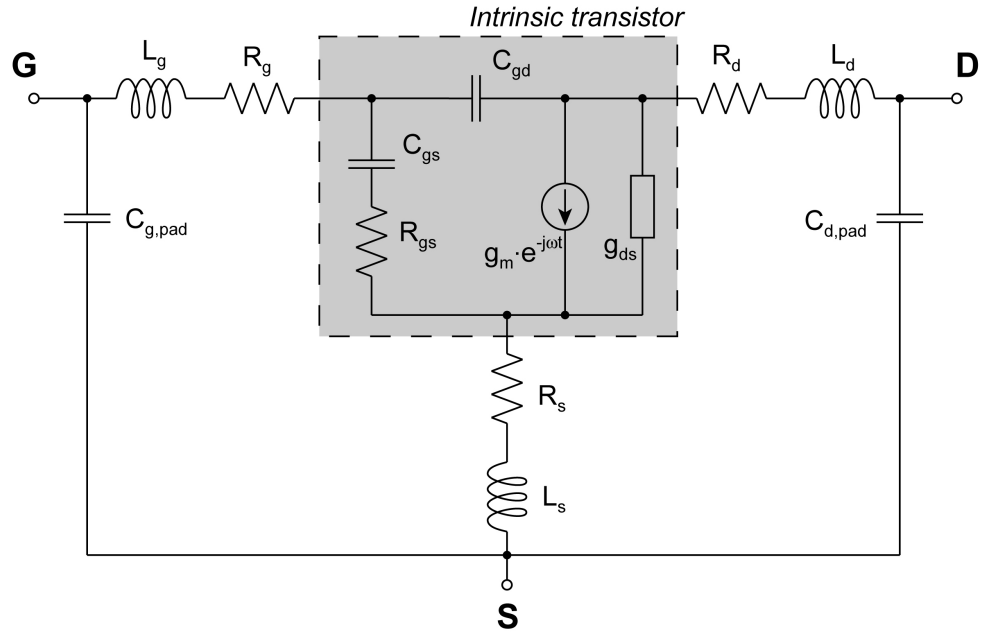


Figure 4.5: Small-signal model of HEMT.

will still be expected to operate.

The classical small-signal model of the HEMT shown in figure 4.5 consists of an intrinsic device where the influence of parasitic resistances (R_g, R_s, R_d), inductances (L_g, L_s, L_d), and capacitances ($C_{g,pad}$, $C_{d,pad}$) of pads are not included and the pads parasitic components.

One of the most important small-signal parameter is the transconductance and under the source-drain current saturation conditions it is defined as:

$$g_m = \left.\frac{dI_d^{sat}}{dV_{gs}}\right|_{V_{ds}=const.} \tag{4.24}$$

With the assumption that only the capacitive effect dominates, the small-signal model can be simplified and redrawn as shows figure 4.6. From this can be derived the radial frequency at which the current gain becomes unity:

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}} \tag{4.25}$$

and from this the unity current gain frequency:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{4.26}$$

If the full small-signal model is considered the approximated unity gain frequency can be expressed as [19]:

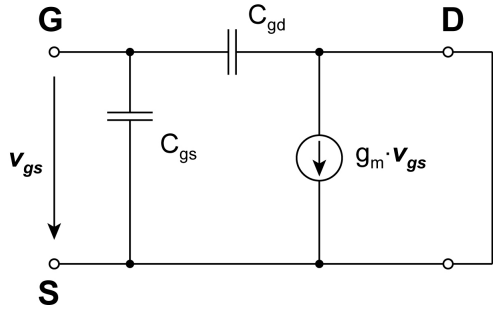


Figure 4.6: Simplified small-signal model of HEMT with dominating capacitive effect and shortcut at the output [19].

$$f_T = \frac{g_m}{2\pi}\left[(C_{gs}+C_{gd})\left(1+\frac{R_d+R_s}{R_{ds}}\right)+C_{gd}g_m(R_d+R_s)\right]^{-1} \tag{4.27}$$

The maximum frequency of oscillations is then [19]:

$$f_{max} = \frac{f_T}{\sqrt{4\cdot\frac{R_s+R_g+R_{gs}}{R_{ds}}+2\cdot\frac{C_{gd}}{C_{gs}}\left(\frac{C_{gd}}{C_{gs}}+g_m(R_s+R_{gs})\right)}} \tag{4.28}$$

From equations 4.26 and 4.27 is clear, that the parasitic parameters of the device degrade the current gain frequency of the transistor. Therefore is important to reduce the parasitics to reach higher frequencies.

4.3 Large-Signal Model

The large-signal model helps us to predict the behaviour of the device applying a large signal to the device (figure 4.7). The aim is to find a compromise between the working frequency (or the input Δf_{in} and output Δf_{out} frequency band width) and the maximum output power applicable to the device. Many factors have to be taken into account but the most important are the material layer structure and the geometry of the transistor that have the biggest influence on the parasitics of the device.

The maximum linear rf output power $P^{dc}_{out\,lin}$ that can be achieved from FET is estimated from the dc output characteristics and the optimal load line (see figure 4.8). If we consider a class A operation then the linear rf output power given by dc behaviour of the transistor is defined as [20]:

$$P^{dc}_{out\,lin} = \frac{I_d^{sat}(V_{br}-V_{knee})}{8} \tag{4.29}$$

In the region where the drain current is a squarewave and the output power saturates, the saturation output power is defined as [20]:

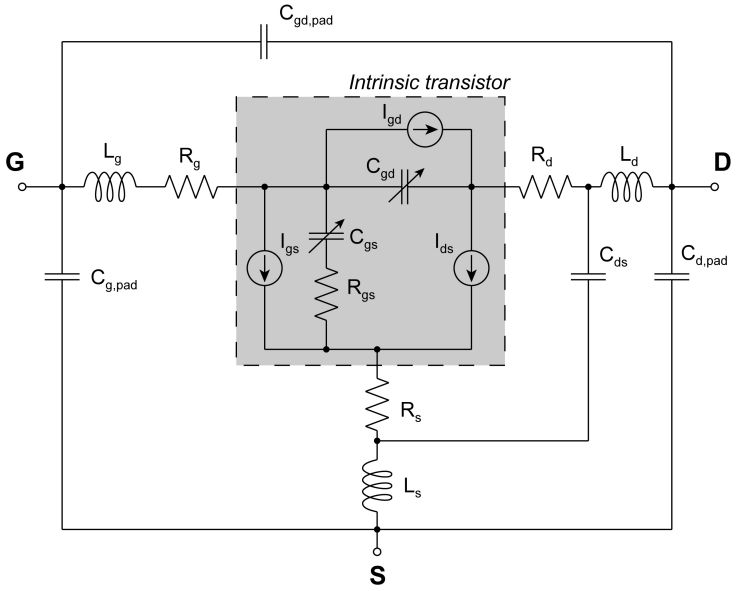


Figure 4.7: Large-signal model of HEMT.

$$P_{out\,sat}^{dc} = \frac{I_d^{sat}(V_{br} - V_{knee})}{8} \cdot \frac{16}{\pi^2} = P_{out\,lin}^{dc} \cdot \frac{16}{\pi^2} \tag{4.30}$$

Actually, the real rf output power P_{out} is often different (lower) from the $P_{out\,lin}^{dc}$ and $P_{out\,sat}^{dc}$. The origin of the difference is in the dc/rf dispersion effect where by dc measurements also surface states and traps in active and buffer layers contribute to the total current [69]. These contributions disappear by the rf power measurement because the traps are not able to follow a quick changes of applied field.

From the measurement point of view the matching of the input and the output circuit is important by the large-signal measurements. If the network is not fitted the reflections at the input or output of the device occur and the measured output power is not maximum. The field effect transistor in idealised matching network is depicted in figure 4.9. The matching inductances L_{in} and L_{out} by the frequency f_m are defined as [21]:

$$L_{in} = \frac{1}{(2\pi f_x)^2 C_{in}} \tag{4.31}$$

$$L_{out} = \frac{1}{(2\pi f_x)^2 C_{out}} \tag{4.32}$$

and the bias gain is equal to:

$$\frac{V_L}{V_S} = -n_{in} \cdot n_{out} \cdot g_m R_L \tag{4.33}$$

Then the power gain is defined as:

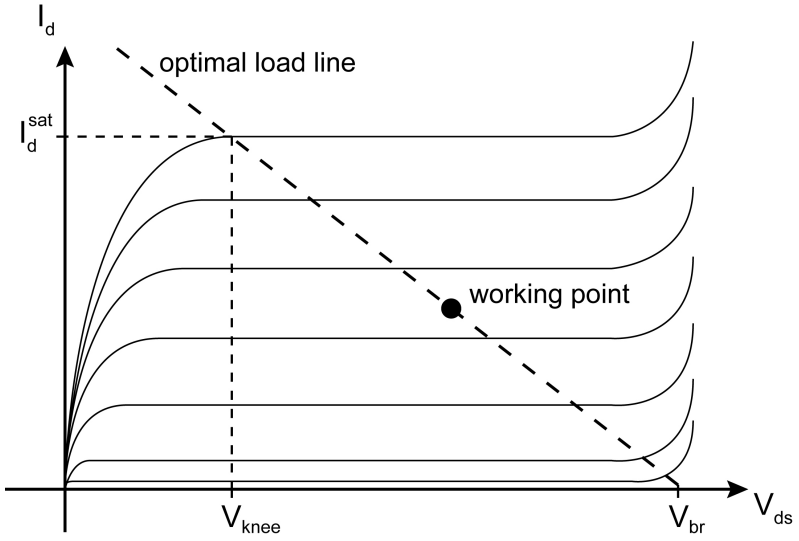


Figure 4.8: Optimal load line for maximum output power.

$$G_T = \left(2\frac{V_L}{V_S}\right)^2 \frac{R_S}{R_L} = (2 \cdot n_{in} \cdot n_{out} \cdot g_m)^2 R_S R_L \tag{4.34}$$

where n_{in} and n_{out} are the input and output transformational ratios of the matching tuners, respectively. If $R_S = R_L = R_0$ then:

$$G_T = (2 \cdot n_{in} \cdot n_{out} \cdot g_m \cdot R_0)^2 \tag{4.35}$$

From this equation follows, that the highest possible power gain can be reached when the transconductance of the transistor g_m is as high as possible. The second factor which influence the power gain is the breakdown voltage V_{br}. The working bias point of the device is in the middle, between V_{knee} and V_{br}, as figure 4.8 shows and therefore with increasing breakdown voltage the applicable range $(V_{br} - V_{knee})$ is wider, the working point moves to higher drain-source voltages, what allows us to reach higher output power.

After the network is fitted the Power Added Efficiency can be expressed as:

$$P.A.E. = \frac{P_{out} - P_{in}}{P_{out}^{dc}} \tag{4.36}$$

where P_{in} is the rf input power and P_{out} is the output power of transistor.

The frequency band width at input and output of the transistor can be determined from figure 4.9 and are defined as:

$$\Delta f_{in} = \frac{1}{2\pi n_{in}^2 R_S C_{in}} \tag{4.37}$$

and

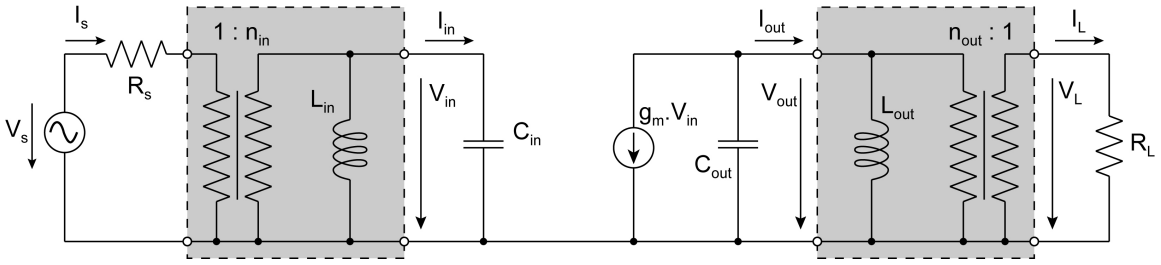


Figure 4.9: FET with idealised matching network.

$$\Delta f_{out} = \frac{1}{2\pi n_{out}^2 R_L C_{out}} \tag{4.38}$$

The aim is to reach the widest possible frequency ranges what is connected with an input and output capacitance of the device. With decrease of the parasitic capacitances the input C_{in} and output C_{out} capacitances also decrease what leads to an increase of Δf_{in} and Δf_{out}.

4.4 Thermal Effects in AlGaN/GaN HEMTs

In previous chapters the small-signal and large-signal models of HEMTs have been introduced but AlGaN/GaN heterostructure presents some specific behaviours that have not been noticed by another material systems. One of this behaviour is the thermal effect which deforms the dc characteristics of the real device and therefore must be included in the model of the HEMT on AlGaN/GaN material system.

The origin of this deformation is again in not thermally matched substrate (see table 3.1) what cause an increase of the channel temperature by higher applied drain-source voltages and hence a decrease of the drain saturation current I_d^{sat}. This effect is called self–heating effect and for its modelling was created an additional sub–circuit presented by Berroth *et al.* (figure 4.10) [22]. This circuit introduces an analogy between the electrical and thermal processes in the device. The thermal current source i_{th} represents the dissipating power and the voltage drop on the thermal resistance R_{th} gives the channel temperature rise defined as:

$$\Delta T = R_{th} i_{th} \tag{4.39}$$

Then the output dc characteristics of HEMTs fabricated on the AlGaN/GaN material system with the self–heating effect are depicted in figure 4.11. The determination of the channel temperature from the output dc characteristics for AlGaN/GaN HEMTs was already presented by Kuzmik *et al.* [33]. The author considers with three factors that

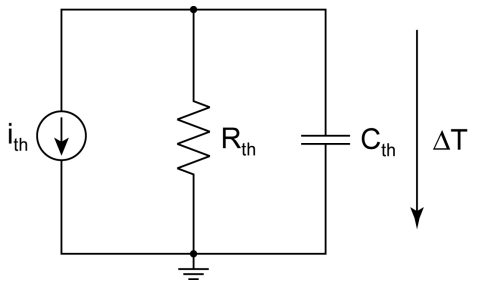


Figure 4.10: The thermal sub–circuit for modeling of the self–heating effect.

contribute to the reduction of the drain–source current:

1. The current reduction caused by a voltage drop on the source-gate resistance $R_s(T)$ which increases at elevated temperatures. The current reduction is then:

$$\Delta I_d^{sat} = I_d^{sat} g_m \Delta R_s \tag{4.40}$$

2. The current drop due to a decrease of the sheet carrier concentration in the channel and therefore the decrease of the threshold voltage V_{th} expressed as:

$$\Delta I_d^{sat} = g_m \Delta V_{th} \tag{4.41}$$

3. The current drop due to a change of the saturation velocity $\Delta\nu_{sat}$ in the channel expressed in respect to the reference value ν_{sat}:

$$\Delta I_d^{sat} = I_d^{sat} \frac{\Delta\nu_{sat}}{\nu_{sat}} \tag{4.42}$$

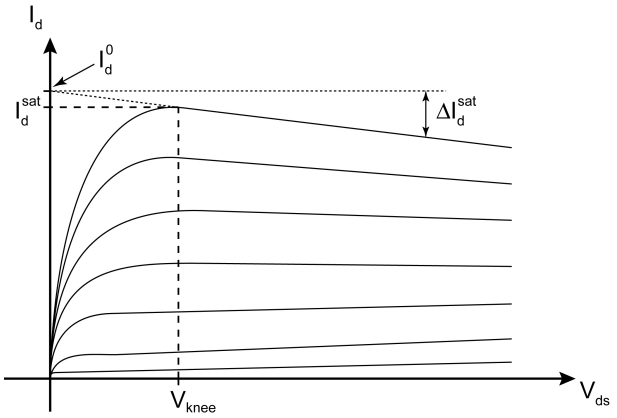


Figure 4.11: The influence of the self–heating effect on the output dc characteristics of HEMT.

The total reduction of the drain–source current is then the sum of these partial contributions and is equal to:

$$\Delta I_d^{sat} = -g_m(I_d^{sat} \cdot \Delta R_{gs} + \Delta V_{th}) + \frac{I_d^{sat} \cdot \Delta \nu_{sat}}{\nu_{sat}} + \frac{V_{ds}}{R_{sub}} \tag{4.43}$$

where V_{ds}/R_{sub} is the leakage current through the substrate. From this equation can be easily derived the channel temperature as a function of the dc dissipating power $T = f(P_{out\,lin}^{dc})$ after the temperature dependencies $V_{th}(T)$, $R_{gs}(T)$ are expressed.

Chapter 5

Determination of Heterostructure Parameters

Before the processing of the grown sample is started the layer structure must be tested for selected parameters to find out if it is suitable for the next treatment. Important parameters of a layer structure as the sheet carrier concentration in 2DEG n_s, the carrier mobility in 2DEG μ_n, the sheet resistance R_{sheet}, the specific resistance ρ_c, etc. are evaluated by different methods. These methods are introduced in this chapter.

5.1 Hall Effect Measurements

The Hall effect measurements allow us to determine independently the sheet resistance R_{sheet} of the layer structure and the 2DEG sheet carrier concentration n_s in the sample. If the current I is flowing through the sample and the magnetic field $\mathbf{B}$ perpendicular to the current flow is applied then the Hall voltage V_H is induced perpendicular to I and $\mathbf{B}$. This situation is depicted in figure 5.1. Each electron flowing in the x-direction with velocity v_x causes in the y-direction the Lorentz-force F_y which is compensated by the Hall voltage V_H. This can be applied just with the condition that no current is flowing in the y-direction. Then the Lorenz-force is expressed as [11]:

$$F_y = -q \cdot (v \times \mathbf{B})_y = q v_x B \tag{5.1}$$

As was mentioned the Lorentz-force must be compensated by the Hall field $\overline{E}_y = V_H/b$ and therefore:

$$F_y = q v_x B = q\overline{E}_y \tag{5.2}$$

With a consideration that the current is carried just by electrons the transport can be

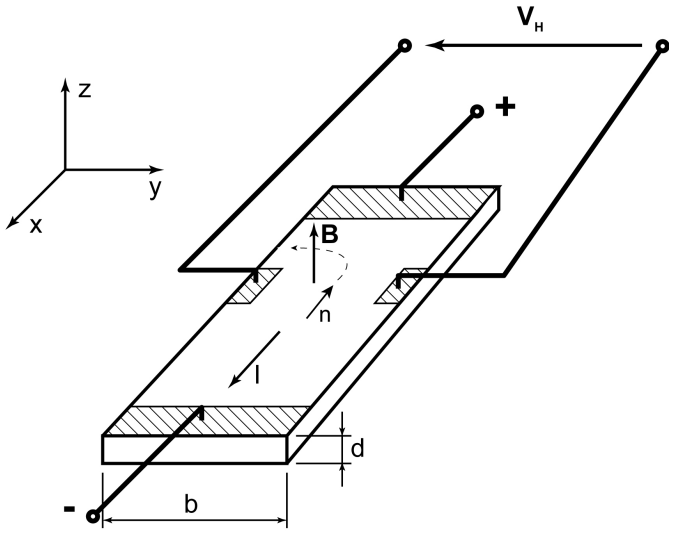


Figure 5.1: The principle of Hall effect measurement.

described as:

$$j_x = \frac{I}{bd} = -nqv_x \tag{5.3}$$

Then the Hall field can be derived from equations 5.2 and 5.3 as:

$$\overline{E}_y = \frac{V_H}{b} = -\frac{1}{nq} j_x B = -\frac{1}{nq}\frac{IB}{bd} \tag{5.4}$$

where $R_H = -(nq)^{-1}$ is the Hall constant. This constant is determined by the measurement and then the corresponding carrier concentration is:

$$n_s = n = -\frac{1}{qR_H} \tag{5.5}$$

In the case of the heterostructure the sheet carrier concentration in the 2DEG n_s is obtained by Hall effect measurement. If the sheet resistance R_{sheet} is known then the carrier mobility μ_n in the channel can be calculated:

$$\mu_n = \frac{1}{q \cdot R_{sheet} \cdot n_s} \tag{5.6}$$

5.2 Atomic Force Microscopy

The Atomic Force Microscopy (AFM) is the method through which the nanometre scale picture and topography information about the sample surface can be obtained. The base of the AFM is a sharp tip fixed on the cantilever which scans the surface of the sample (figure 5.2). The laser beam focused on the back side of the cantilever is reflected onto a

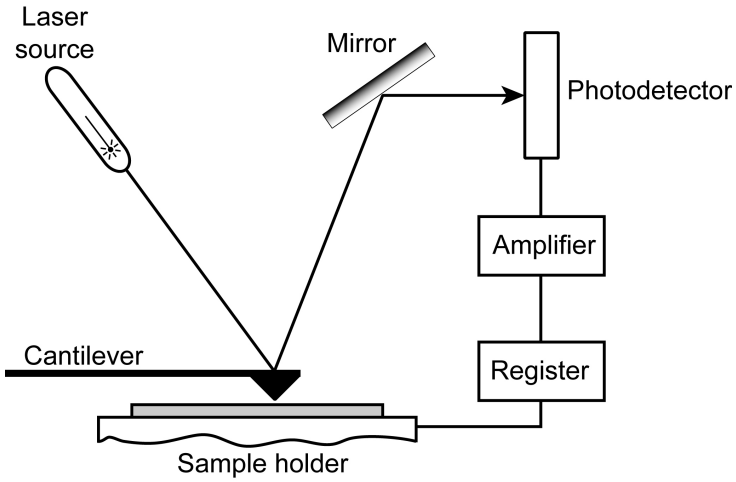


Figure 5.2: The schematic draw of the Atomic Force Microscopy.

position-sensitive photodetector. In this arrangement a small deflection of the cantilever will tilt the reflected beam and change the position of the beam on the photodetector.

The force between tip and the sample surface is very small, usually less than $10^{-9}N$. The feedback mechanisms enables the piezoelectric scanners to maintain the tip at a constant force (or height) above the surface. According to the interaction of the tip and the sample surface, the AFM can be classified as repulsive (contact mode), attractive (non-contact mode), or tapping mode. The mode must be chosen in view on the scanned surface and the required accuracy of the measurement.

In contact mode a high resolution can be provided but the electrostatic and tension surface forces pull the scanning tip toward the surface what can damage the sample and distort image data. On the other side the non-contact mode provides low resolution of the scan. The tapping mode was developed for scanning very soft and fragile samples without inducing destructive forces and reaching high resolution of the image.

The AFM allows us not just to see the sample surface, but also to evaluate the surface parameters as the root-mean-square roughness rms, the maximum peak hight R_{max}, the average peak height R_a, etc. and helps us to predicate a suitability of the sample for the next device processing.

5.3 Transmission Line Model (TLM)

The transmission line model is the commonly used model for the determination of the sheet resistance R_{sheet}, the contact resistance R_c, and the specific resistance ρ_c. The basic principle is in the precise measurement of the resistance R between two rectangular ohmic contacts with different distances in between them (see figure 5.3 a). After the measured resistance R over the distance between the contacts d is plotted, the measured points can

be fitted by the linear curve described with equation (figure 5.3 b) [40]:

$$R = 2 \cdot \frac{R_c}{W} + d \cdot \frac{R_{sheet}}{W} \tag{5.7}$$

where W is the width of contacts. From this equation can be easily derived the contact resistance R_c and the sheet resistance R_{sheet}. The specific resistance ρ_c is then expressed by [40]:

$$\rho_c = \frac{R_c^2}{R_{sheet}} \tag{5.8}$$

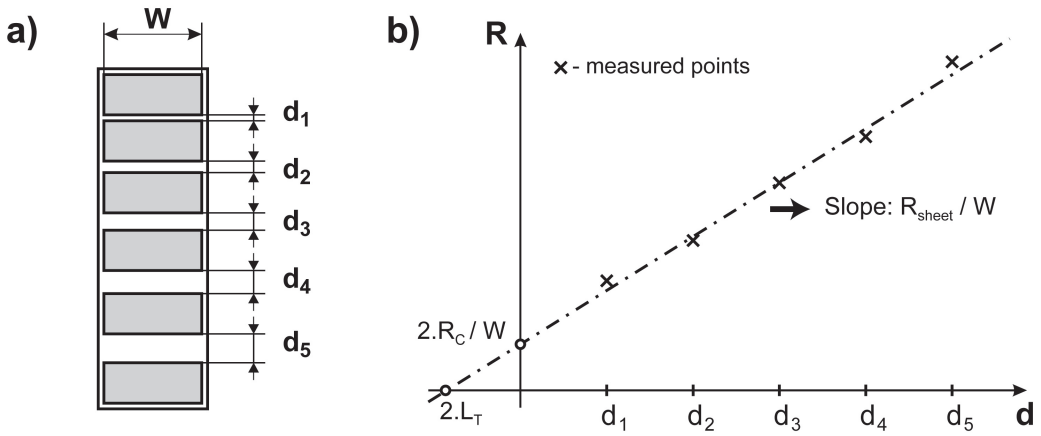


Figure 5.3: The shape of TLM structures (a) and evaluation of the contact R_c and sheet R_{sheet} resistance.

5.4 Capacitance-Voltage Measurements

The capacitance-voltage measurements (C-V measurements) are the final ones we use to determine the layer structure quality. These measurements show us if the 2DEG is formed in the structure and together with TLM measurements alow us to calculate the sheet carrier concentration in the 2DEG and the mobility in the channel. These results can be afterwards compared to the Hall effect measurements.

The C-V techniques are based on the fact that the depletion region width w of the reverse biased semiconductor junction depends on the reverse applied voltage. If we consider the Schottky contact (figure 5.4 a) where the dc reverse bias V_{dc} is applied, then the capacitance under the metal of the Schottky contact can be defined as [40]:

$$C = \frac{dQ_s}{dV_{dc}} \tag{5.9}$$

where Q_s is the semiconductor charge. The capacitance is determine by the superposing

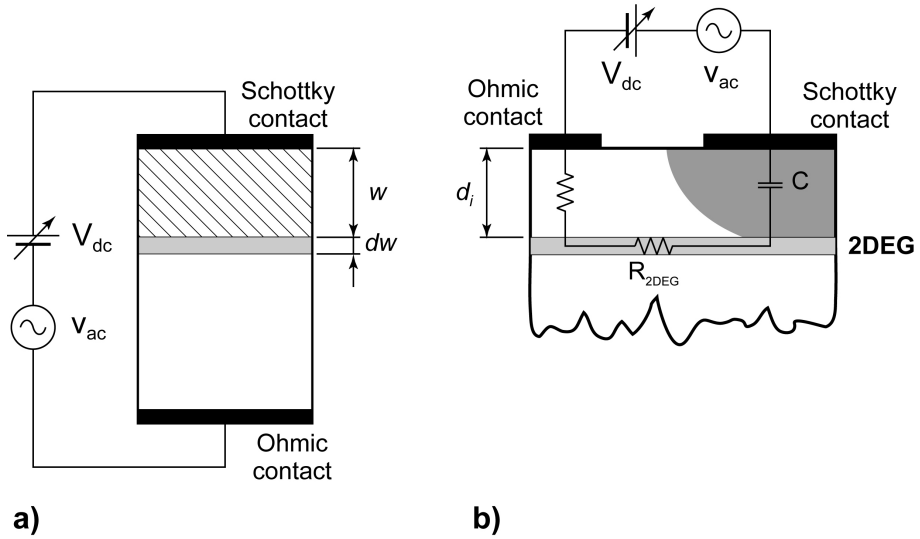


Figure 5.4: The analogy between a vertical (a) and a horizontal Schottky diode with 2DEG (b).

of a small amplitude ac voltage v_{ac} on the reverse dc voltage V_{dc}. The amplitude of the ac voltage is usually in the range of 10 to $20mV$ and the frequency is $1MHz$ [40]. Then the semiconductor charge increment dQ_s is given by:

$$dQ_s = -q \cdot A \cdot N_D(w) \cdot dw \tag{5.10}$$

where A is the area under the Schottky contact and N_D is the ionised donor density. The capacitance of the Schottky contact derived from equations 5.9 and 5.10 is:

$$C = \varepsilon \frac{A}{w} \tag{5.11}$$

As an analogy to the situation displayed in figure 5.4 a, the heterostructure with formed 2DEG and Schottky contact on the top can be used (figure 5.4 b). If the 2DEG is considered as a conductive plane connected to the ohmic contact, then the capacitance between the metallic Schottky contact and the 2DEG can be determine. After the zero bias is applied to the Schottky contact and we consider that the depletion region is in touch with 2DEG due to the built-in voltage V_{bi}, the capacitance can be calculated according equation 5.11 where the depletion region width w is substituted for the depth of the 2DEG d_i:

$$C = \varepsilon \frac{A}{d_i} \tag{5.12}$$

In ideal case the capacitance C is constant with decreasing reverse bias down to V_{th} where the depletion region starts to penetrate through the channel (figure 5.5). After the whole

channel is depleted (reverse bias $\geq V_{th}$) the final capacitance of the Schottky contact is the series combination of the depletion region capacitance C and the capacitance of the depleted 2DEG C_{2DEG}. Due to very small channel capacitance C_{2DEG} [41] in comparison to the depletion region capacitance C, an abrupt decrease in CV characteristics of the diode is observed (figure 5.5).

Then the sheet carrier concentration of the channel can be calculated using equation 5.10:

$$n_s = \frac{1}{q \cdot A} \int_{V_{th}}^{V_{bi}} C(V) \cdot dV \tag{5.13}$$

where

$$Q_s = \int_{V_{th}}^{V_{bi}} C(V) \cdot dV \tag{5.14}$$

If the sheet resistance R_s is determined from the TLM measurements, the carrier mobility in the channel can be obtained in the same way as by Hall effect measurements from equation 5.6.

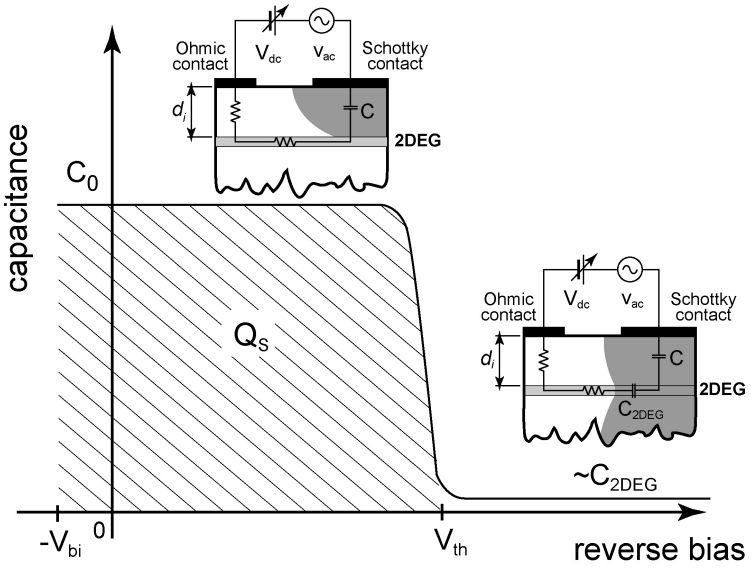


Figure 5.5: The ideal capacitance-voltage characteristic of the horizontal Schottky diode with 2DEG.

Chapter 6

Processing Technology

In recent years the processing technology of HEMTs based upon various material systems has been established in research and industrial institutions around the world as well as in our institute. Nevertheless, adaptation of the standard process to AlGaN/GaN material system was a crucial task yet to be accomplished. P. Javorka *et al.* began the process of HEMT technology adaptation to GaN–based systems in 1999 at our institute [10]. During his diploma and PhD studies the basic AlGaN/GaN HEMT technology process has been successfully developed for sapphire and silicon substrate.

Within the bounds of my PhD work the process technology was improved and modified to enable the fabrication of AlGaN/GaN HEMTs on SiC substrate and MOSHFETs[1]. Besides of this, additional technology steps were developed to improve dc, frequency, and power performances of the devices.

This chapter gives an insight into the standard AlGaN/GaN HEMT technology process (6.1), shows up the differences between standard and MOSHFET technology process (6.2), introduces the air bridge technology (6.3) and the application of passivation layers (6.4), gives an overview on the field plate technology (6.5) and describes the masks used for lithographical processes.

6.1 Standard AlGaN/GaN HEMT technology process

The process of classical HEMT fabrication consists of four steps, involving definition of mesa islands (mesa insulation), ohmic contacts fabrication (drain and source of HEMTs), Schottky contacts definition (gate electrodes), and contact pads fabrication.

A common approach in fabrication of semiconductor devices is to process many devices on the same wafer in parallel. The mesa insulation applies a technique to isolate the individual devices (transistors, diodes, MSM's, etc.) from each other in order to minimise

[1] Metal–Oxid–Semiconductor–Heterostructure–Field–Effect–Transistors

influences of devices in between. Isolation is reached by removing the conducting regions between the devices, i.e. the 2DEG must be removed to exclude conductive connections. The depth of the insulation etching in HEMTs depends on the depth of the AlGaN/GaN interface where the 2DEG is formed (cca. 20-50 nm for conventional layer structure). Afterwards, ohmic contacts are fabricated. They ensure best connection to 2DEG with the lowest possible resistance. Schottky contact is formed between source and drain ohmic contacts as the electrode which allows to control the drain current flow (see chapter 4). Finally, pads are introduced to give the possibility to measure the fabricated device with contact needles or bonding connections.

A picture of a HEMT fabricated in our labs taken by Secondary Electron Microscopy (SEM) with typical dimensions is shown in figure 6.1.

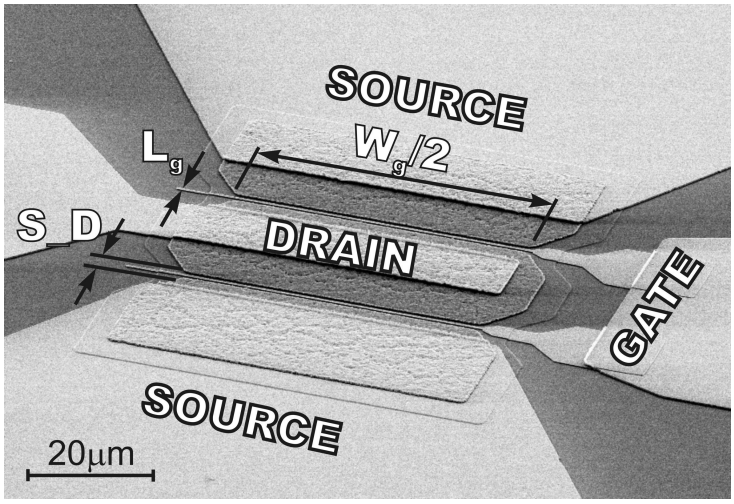


Figure 6.1: SEM picture of AlGaN/GaN HEMT with the gate width W_g of 200μm, the gate length L_g of 0.3μm, and the source–drain distance S_D of 3μm fabricated in our labs.

6.1.1 Definition of mesa islands

The definition of mesa islands in AlGaN/GaN layer systems necessitates the development of special processes due to the very strong bond energies in III–nitrides in comparison to other compound semiconductors. Often used wet chemical etching was found not to be suitable because of small etching rates (10nm/min), roughness surface, inhomogeneous depth and rough sidewalls with negative slope [10, 13]. Therefore, two dry etch processes; Electron Cyclotron Resonance Reactive Ion Etching (ECR RIE) and milling with Ar^+ ions (Ar^+ sputtering) were applied as suitable methods for etching GaN–based layer structures.

The ECR RIE technique applies a Cl_2–based inductively coupled plasma that has plasma density of two to four orders higher magnitude in comparison to conventional

RIE. The composition of gases Ar (5sccm) / CH_4 (5sccm) / H_2 (15sccm) / Cl_2 (2sccm) leads to relatively high etching rates of 70–100 nm/min. Cl_2–based RIE in combination with a lithography process using hardened resists results in suitable but rough edges (see figure 6.2 a).

Compared to Cl_2–based RIE the Ar^+ sputtering technology used in our lab yields even better results. This special type of Ion Beam Etching (IBE) etches the free surface of the sample by bias accelerated Ar^+ ions [10]. In our system we use an acceleration bias of 500 V and the density of ions is given by the current density of 0.5 mA/cm^2. These parameters result in an etching rate of 25–35nm/min depending on the composition of AlN in $Al_xGa_{1-x}N$ layer. The etched surface is shown in figure 6.2 b. Due to the very smooth, homogenous edges and not observable influences on the HEMTs electrical behaviour this technique was chosen as the standard etching technique. Suitable depths of the etched mesa profile reaches from 250 to 350 nm depending on the layer structure. Obtained results are consistent with results published in my diploma thesis [90].

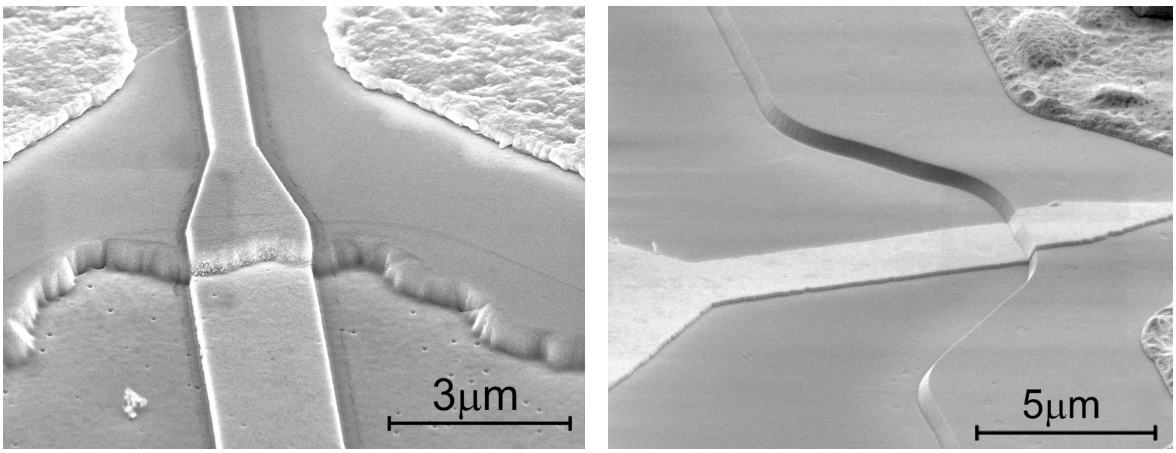


Figure 6.2: Comparison of AlGaN/GaN HEMTs etched by ECR RIE (a) and Ar^+ sputter (b) manufactured in our labs.

6.1.2 Ohmic contacts

Fabrication of ohmic contacts is the next important step which influences device properties. The contacts are applied by standard photolithography process followed by deposition of multilayered metals (for details see Appendix A). After the resist and the rests of metals have been removed by lift–off technique the contacts undergo a special annealing process. In order to reach ohmic behaviour annealing of the metallic layer in AlGaN/GaN systems requires a very high temperature, typically between 700°C and 900°C. The ohmic

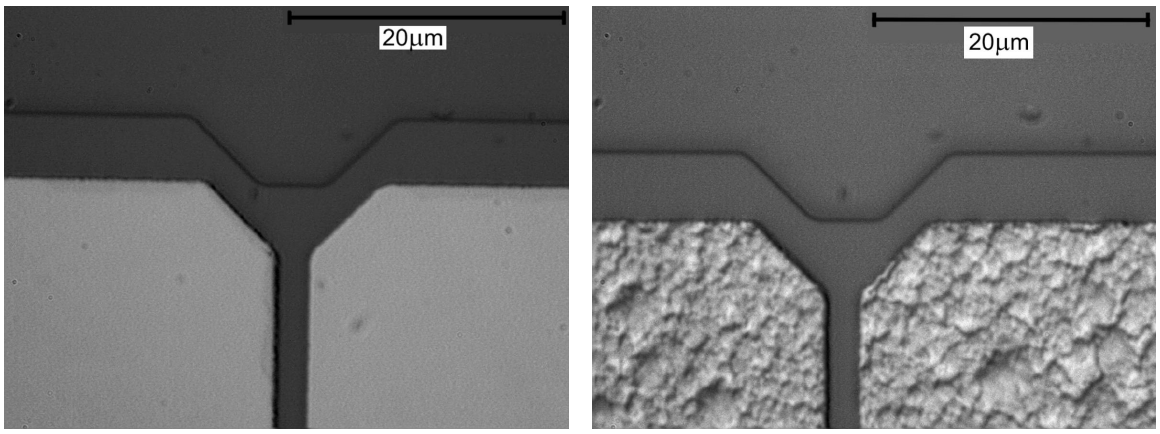


Figure 6.3: Ohmic contacts of AlGaN/GaN HEMT before (a) and after (b) annealing done in our labs.

contacts are visibly rougher after the annealing process. This result is typical for GaN–based materials and does not degrade the electrical behaviour of the device (see figure 6.3). The study of alternative ohmic contact types and a literature overview is to be found in my diploma thesis [90].

For fabrication of ohmic contacts we have used a Ti (35nm) / Al (200nm) / Ni (40nm) / Au (100nm) multilayer annealed at 850°C for 30 seconds in a N_2–rich atmosphere. The composition of metallic layers and annealing procedure was intensively studied at our institute by P. Javorka *et al.* and the results of this study are published in [10, 91]. The annealing process involves use of a computer controlled AET Addax Rapid Thermal Processing system. By means of the RTP system annealing temperature was well controllable over time, as illustrated by the temperature–time–function in figure 6.4[2]. Electrical parameters of ohmic contacts were evaluated by TLM measurements introduced in chapter 5 and are summarised in section *AlGaN/GaN layer structures* of chapter 7.

6.1.3 Schottky contacts

For manufacturing of suitable Schottky contacts on top of GaN (AlGaN) layer the appropriate metals must be chosen. It is important to create contacts with good rectifying behaviour of the metal–semiconductor interface, i.e. with a high Schottky barrier and low reverse (leakage) currents. Rectifying behaviour for n-GaN has been observed using Pt, Ni, Pd, Au, Co, Cu, and Ag contacts [13]. Some typical measured values of barrier heights for different metals and of the thermal stability, which is critical for real device operation, are collected in table 6.1.

[2]Used pyrometer is capable of measuring temperature above a 350°C.

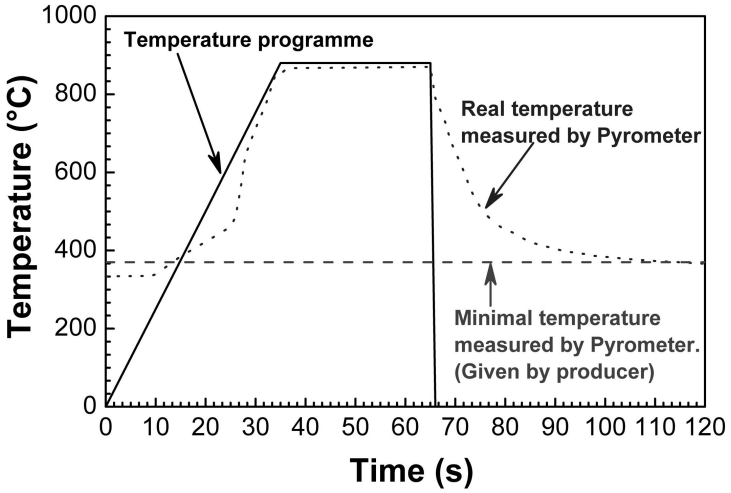


Figure 6.4: Temperature over time during the annealing process of ohmic contacts.

Metal	Barrier height	Thermal limits
Pt	1.00–1.10 eV	400 °C
Au	0.91–1.15 eV	575 °C
Ti	0.10–0.60 eV	–
Pd	0.94–0.95 eV	300 °C
Ni	0.66–0.99 eV	600 °C
Ag	0.90 eV	–
Ni/Au	1.04 eV	–

Table 6.1: Published heights of Schottky barriers and thermal limits on GaN [13, 38, 92].

There are two possibilities of Schottky contacts fabrication depending on the required pattern dimensions. The standard photolithography process is used for the fabrication of gate length longer as 1 μm. Gate lengths shorter than 1 μm are usually patterned by Electron Beam Lithography (E–beam) using a combination of PMMA resists (for details see Appendix A). The E–beam processing allows us to reach higher accuracy, better positioning, and higher resolution of patterned structures and was used as the standard technology step for definition of Schottky contacts. After pattern definition the Ni/Au metal layer is deposited. The detailed study of Schottky contacts on GaN–based structures and their behaviour was introduced in my diploma thesis [90].

6.1.4 Contact Pads

The final step in processing standard high electron mobility transistor is the fabrication of contact pads. The standard photolithography process followed by Ti/Au metallisation is used.

6.2 MOSHFET technology process

This section describes the MOSHFET fabrication technology process developed within the bounds of this work and shows up the differences to standard HEMT processing.

The major difference between HEMTs and MOSHFETs consists of a thin isolating layer that is placed in between semiconducting layer and metal electrode forming a MOS–structure. Figure 6.5 displays this characteristic difference. Strict requirements regarding the thickness of isolation layer are given for standard MOSFETs as well as for MOSHFETs. The thicknesses of this layer found in literature are beneath 15 nm but in general should be as thin as possible. SiO_2, Si_3N_4, $SiO_2/Si_3N_4/SiO_2$, and Al_2O_3 [93–96] layers were already presented as suitable solutions.

The fabrication process of MOSHFETs consists of five steps; definition of mesa islands, ohmic contacts fabrication, contact pads fabrication, deposition of isolation layer, and Schottky contacts definition.

The definition of mesa islands and fabrication of ohmic contacts is identical to standard HEMT processing. After these two steps have been performed contact pads are fabricated. It is important not depositing contact pads on top of the isolation layer. This might cause an additional parasitic capacitance due to relative large pad surface. After the contact pads have been applied the isolation layer is deposited. In our case a 10 nm thick SiO_2 layer deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) at 300 °C is used. The used deposition rate of 5.7 nm/min is the lowest possible rate of our PECVD machine. After the isolation layer has been deposited on the sample surface the contact pads need to be opened up again. This is done by means of Reactive Ion Etching (RIE) in O_2 plasma atmosphere (for details see Appendix B). Finally, the gate electrodes are processed by E–beam lithography as in standard HEMT process.

After processing the MOSHFET the thickness of the isolation layer is controlled by CV measurements on Schottky diodes and by ellipsometry.

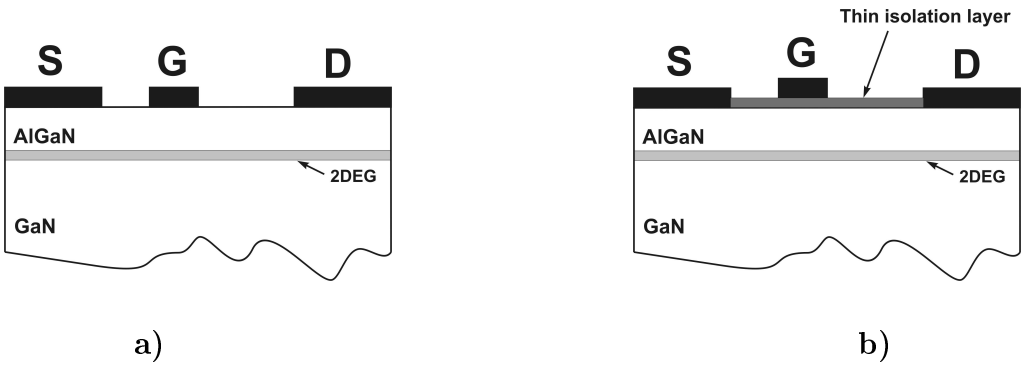
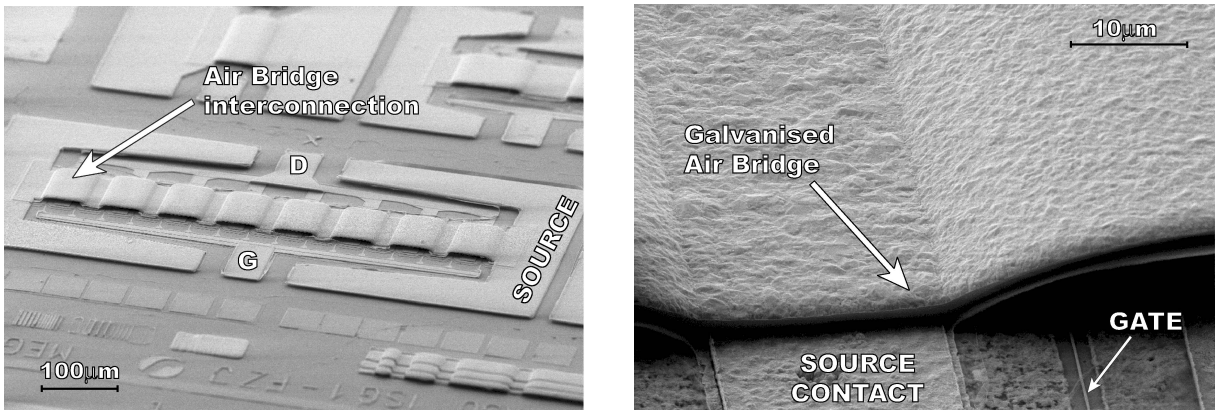


Figure 6.5: Differences between standard HEMT a) and MOSHFET b) structure.

6.3 Air Bridge technology

Air bridge technology is crucial to fabricate multiple finger devices with high power characteristics. It enables construction of conducting interconnections of source regions by bridging gate and drain regions. The fabrication of such a connection is challenging and therefore this technological step is used just when necessary.

The process developed at our institute has been already used a few years ago but, now for the first time it is adapted and applied to the AlGaN/GaN HEMTs. This process enables production of HEMTs with 4, 8, and 16 parallel gate fingers. Gate and drain electrodes are connected as in standard technology process while the source electrodes are connected using Air Bridge technology. Detailed description of the process is introduced in appendix C. A typical device using Air Bridge technology fabricated in our labs is shown in SEM picture 6.6.



a) b)

Figure 6.6: SEM picture of HEMT with Air Bridge technology fabricated in our labs (a); detailed view of the Air Bridge (b).

6.4 Passivation layers and materials

A passivation layer is a non–conductive layer deposited on the active area of a device. Usually the passivation layer protects the device from surrounding influences but this is not the only function by AlGaN/GaN heterostructures. As known, close to the AlGaN/GaN interface a polarisation induced charge (2DEG) is formed with very high electron density. It is not entirely clear until now what is the source of these electrons. A widely accepted explanation is that natural donor–like surface states are the source of the electrons [70] and due to this the change of the surface states are mirrored into the concentration of the 2DEG. The surface donor–like states can be easily affected by a

surface passivation layer and therefore in AlGaN/GaN heterostructures the sheet carrier concentration of 2DEG can be directly influenced by the passivation layer. Due to this reason it is very important to choose suitable passivation which does not degrade the device properties.

Many different types of surface passivation as Al_2O_3, Si_3N_4, SiO_2, Sc_2O_3 and MgO have been tested to reach the best device behaviours [61, 65–68, 77, 78, 103]. Influence of Si_3N_4 and SiO_2 passivation has been investigated in our laboratories. The passivation layer was deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) at temperatures from 150°C to 350°C. The measured thickness of layers was in the range from 10 nm to 150 nm. The thickness of the deposited layer was measured by ellipsometry.

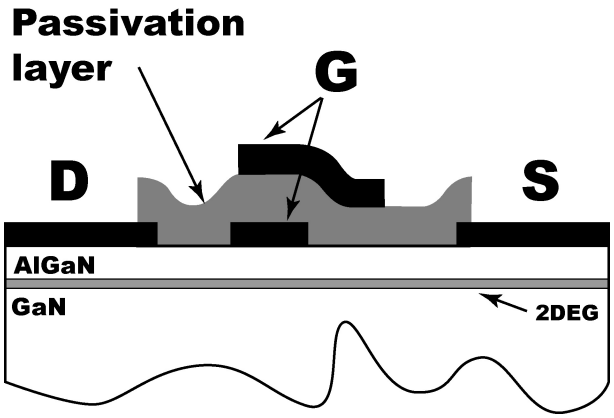
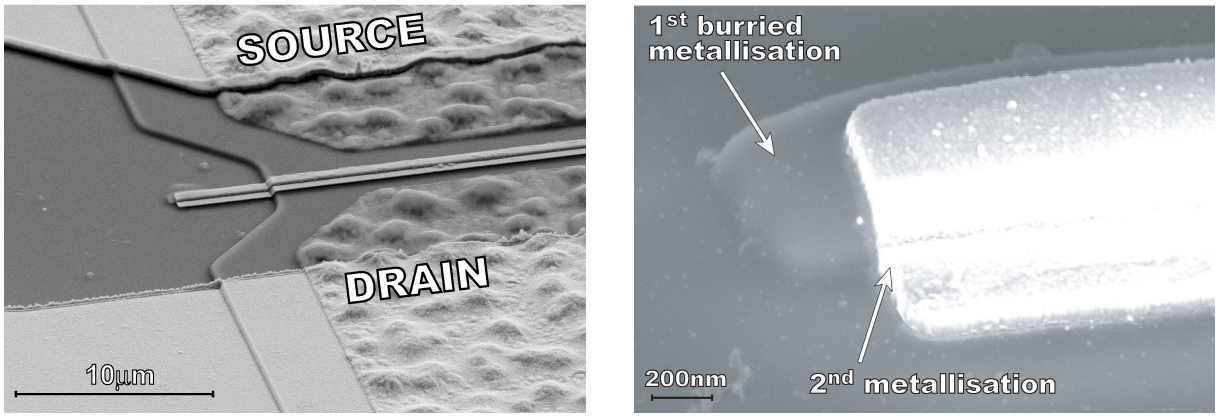


Figure 6.7: The principle of the field plate technology.

6.5 Field plate technology

Field plate technology is known since 1969 and is successfully used to increase the breakdown voltage of Field Effect Transistors (FETs). In AlGaN/GaN HEMT technology it is used since 2003 [87]. The field plate technology means fabrication of two gates, one above the other, separated by a passivation layer in between and connected by a pad (see figure 6.7). The passivation layer and the second gate electrode fabrication process is identical to standard process described above. It is important to place the second gate closer to the drain electrode which reduces the peak of electrical field under the first gate. The SEM pictures of a typical HEMT fabricated with field plate technology in our labs is shown in figure 6.8. The physical principle of this technology and the achieved results are described and simulated in chapter 10.



a) b)

Figure 6.8: SEM picture of AlGaN/GaN HEMT with field plate technology done in our labs a) and the detailed view of the field plated gate electrode b).

6.6 Masks

The description of the lithography mask is the final part which is needed to have a complete picture of the used technology process. Two mask sets have been used for fabrication of HEMTs in this work: "Mega HEMT" mask set and "Power2" mask set. The first set (Mega HEMT) was designed by M. Marso *et al.* and the second (Power2) was optimised for requirements within the bounds of this work.

An overview of "Mega HEMT" mask is to be found in figure 6.9. Each mask set consists of 4 basic fields which are repeated periodically. Fields 1, 2, and 4 are identical while field 3 contains Van der Pauw pattern instead of two MSM structures and FAT-FET devices. This design has been chosen to have the possibility to control the material properties of each sample by Hall effect measurements. HEMTs with gate width from 100 μm to 300 μm and gate length from 0.3 μm to 0.9 μm have been processed. The source–drain distance was designed from 2 μm to 5 μm for HEMTs and from 13 μm to 54 μm for FAT–FETs. The lateral Schottky diodes have a surface area of $25\times25\,\mu m^2$, $50\times50\,\mu m^2$, $100\times100\,\mu m^2$, and $200\times200\,\mu m^2$ with a 5 μm lateral distance from the ohmic contact.

The layout of the "Power2" mask set is shown in figure 6.11. Main difference between the "Power2" and "Mega HEMT" set is the introduction of the field plate technology in the "Power2" mask set and the eccentric positioning of the gate electrode (closer to the source contact) of the devices marked as Q, R, S, T U, V. Also the variation of the gate length and the source–drain distance was increased. The exact dimensions are documented in tables 6.2 and 6.3.

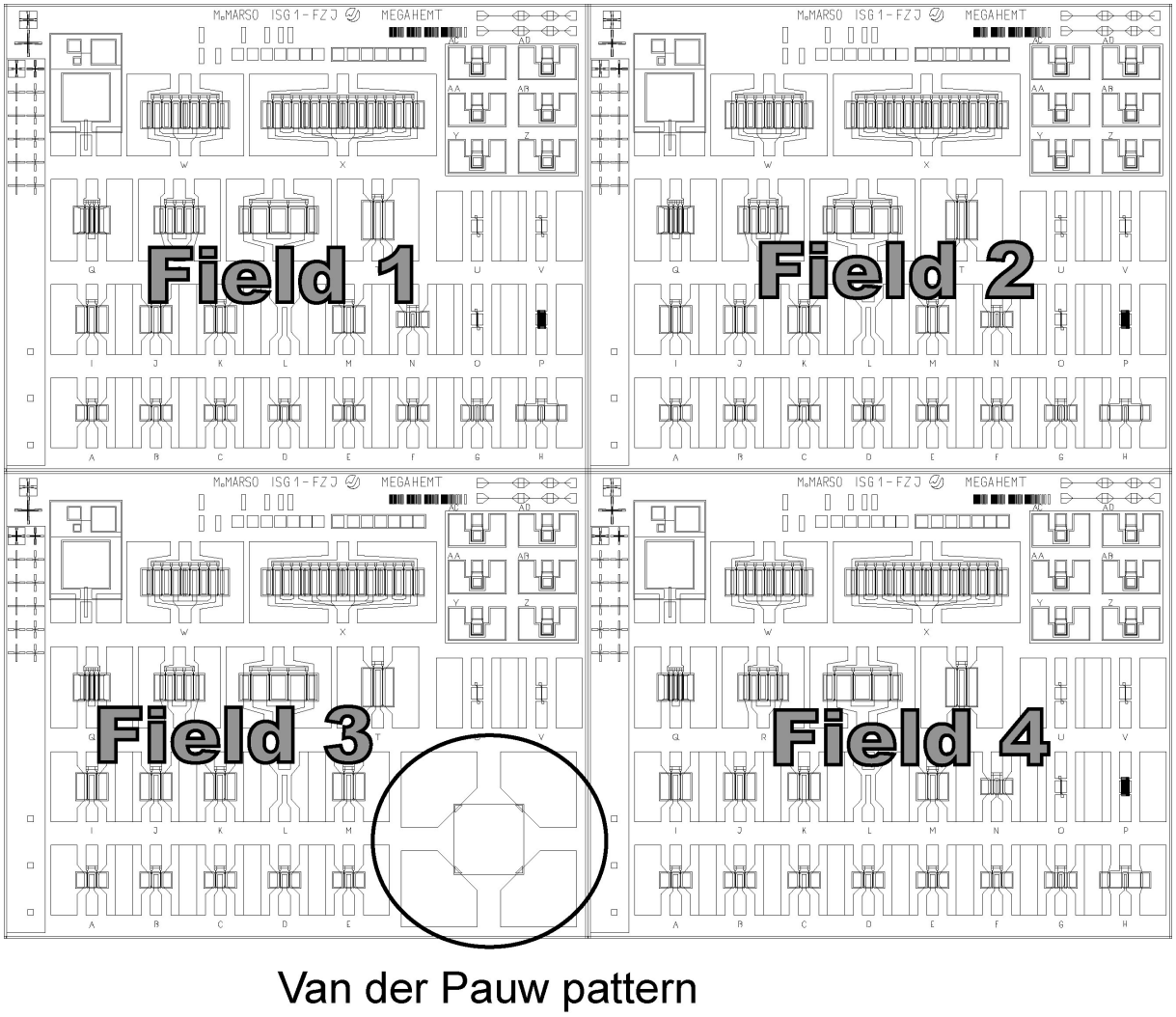


Figure 6.9: Overview of the 4 basic fields creating "Mega HEMT" mask set.

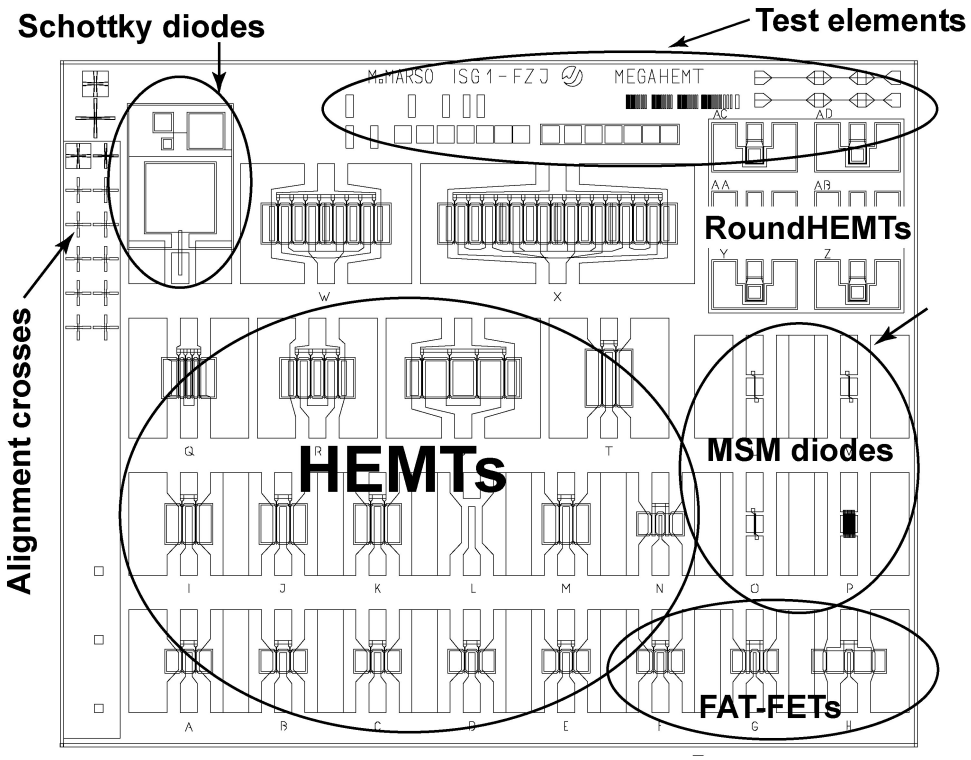


Figure 6.10: Description of the "Mega HEMT" mask field composition.

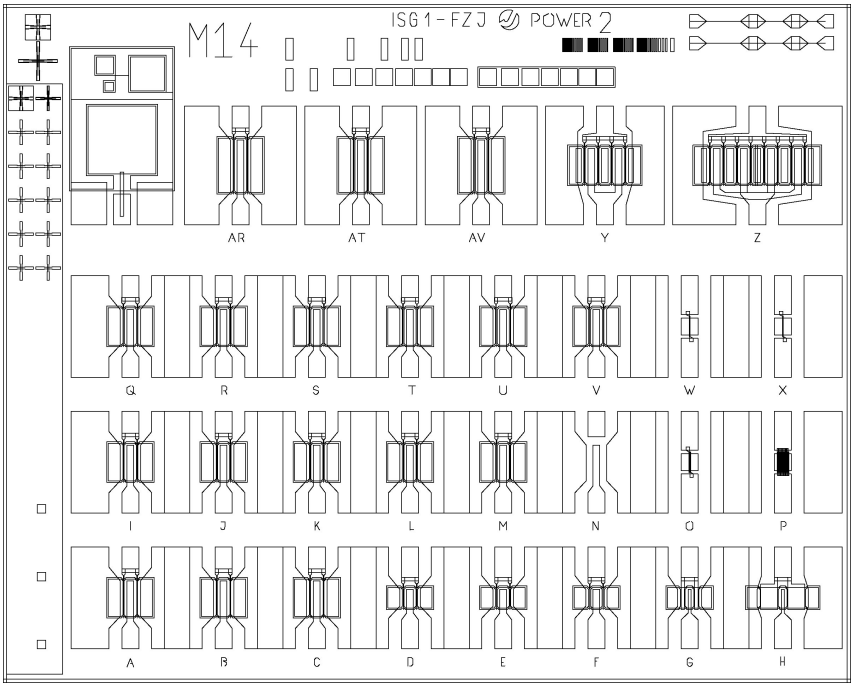


Figure 6.11: The layout of the "Power2" mask.

Device		**Gate Width** W_g (μm)	**Gate Length** L_g (μm)	**S_D distance** S_D (μm)
A, B, C	HEMT	2×50	0.3	3.0
D	HEMT	2×50	0.5	5.0
E	HEMT	2×50	0.7	5.0
F	FAT–FET	2×50	2.0	6.0
G	FAT–FET	2×50	10.0	14.0
H	FAT–FET	2×50	50.0	54.0
I	HEMT	2×100	0.3	3.0
J	HEMT	2×100	0.5	3.0
K	HEMT	2×100	0.7	3.0
L	TEST	2×100	N/A	N/A
M	HEMT	2×100	0.3	2.0
N	FAT–FET	2×100	10.0	14.0
O	MSM	1×50	2.0	1.0
P	MSM	9×50	1.0	1.0
Q, R, S	HEMT	4×100	0.3	3.0
T	HEMT	2×150	0.3	3.0
U	MSM	1×50	0.5	0.5
V	MSM	1×50	0.5	1.0
W	HEMT	8×100	0.3	3.0
X	HEMT	16×100	0.3	3.0
Y, Z	Round HEMT	150	0.7	5.0
AA, AB	Round HEMT	150	0.3	5.0
AC, AD	Round HEMT	150	0.3	3.0

Table 6.2: "Mega HEMT" mask set description.

Device		**Gate Width**	**Gate Length**	**Distances**		
		W_g (μm)	L_g (μm)	S_D (μm)	S_G (μm)	G_D (μm)
A	HEMT	2×100	0.3	2.0	0.85	
B	HEMT	2×100	0.5	2.0	0.75	
C	HEMT	2×100	0.7	2.0	0.65	
D	HEMT	2×100	0.5	4.0	1.75	
E	HEMT	2×100	0.7	4.0	1.65	
F	FAT–FET	2×100	2.0	5.0	1.50	
G	FAT–FET	2×100	10.0	13.0	1.50	
H	FAT–FET	2×100	50.0	54.0	2.00	
I	HEMT	2×100	0.7	2.5	0.90	
J	HEMT	2×100	0.7	3.0	1.15	
K	HEMT	2×100	0.9	3.0	1.05	
L	HEMT	2×100	0.9	3.5	1.30	
M	HEMT	2×100	0.9	4.0	1.55	
N	TEST	2×100	N/A	N/A	N/A	
O	MSM	1×50	2.0	1.0	N/A	
P	MSM	9×50	1.0	1.0	N/A	
Q	HEMT	2×100	0.5	3.0	1.0	1.5
R	HEMT	2×100	0.5	3.0	1.2	1.3
S	HEMT	2×100	0.5	3.5	1.0	2.0
T	HEMT	2×100	0.5	3.5	1.2	1.8
U	HEMT	2×100	0.7	4.0	1.0	2.3
V	HEMT	2×100	0.7	4.0	1.2	2.1
W	MSM	1×50	0.5	0.5	N/A	
X	MSM	1×50	0.5	1.0	N/A	
Y	HEMT	4×100	0.5	3.0	1.25	
Z	HEMT	8×100	0.5	3.0	1.25	
AR	HEMT	2×150	0.5	3.0	1.2	1.3
AT	HEMT	2×150	0.5	3.5	1.2	1.8
AV	HEMT	2×150	0.7	4.0	1.2	2.1

Table 6.3: "Power2" mask set description.

Chapter 7

AlGaN/GaN Layer Structures on SiC

The layer structure of AlGaN/GaN HEMTs is a frequently discussed topic. The layer composition and thickness has to be chosen with respect to the used substrate. We have investigated AlGaN/GaN HEMTs grown on SiC substrate what makes the task much easier compared to sapphire or Si substrates. This is due to the very small lattice mismatch of SiC to GaN and the very good thermal conductivity (see chapter 3 and table 3.1). This chapter describes the composition of layers, the simulation of band diagrams, and the characterisation of layer structures used in this work.

7.1 Composition of Layers

All layer structures grown on SiC substrate were produced by CREE Inc. (former ATMI Inc.) by Metal Organic Vapour Phase Epitaxy (MOVPE) according to our specifications. Generally, the used layer structures can be divided into four categories:

- non intentionally doped (n.i.d.),
- Si doped,
- with GaN cap layer,
- without GaN cap layer,

and combination of these four categories. An overview of processed samples and their layer structures is given in figure 7.1 and table 7.1.

From bottom to top the layers are as follows: On top of the SiC substrate a thin AlN layer is grown to reach Ga–face polarity of the n.i.d. 3 μm thick GaN layer. On top of this either a 30 nm thick n.i.d. $Al_{0.28}Ga_{0.72}N$ layer is grown for undoped samples or a stack of a 10 nm n.i.d. $Al_{0.28}Ga_{0.72}N$, a 10 nm Si doped $Al_{0.28}Ga_{0.72}N$, and a 5 nm n.i.d. $Al_{0.28}Ga_{0.72}N$ layers for the doped ones. Optionally, a 3 nm thin GaN cap layer is created on top, as on samples F1435, F1438, F1749, and F1750 (see table 7.1).

Sample	Substrate	Doping	GaN cap
S2661	SiC	n.i.d.	no
F1435	treated SiC	n.i.d.	yes
F1438	SiC	n.i.d.	yes
F1749	SiC	Si: 2×10^{18} cm^{-3}	yes
F1750	SiC	Si: 5×10^{18} cm^{-3}	yes

Table 7.1: Description of layer structures and differences in between.

The non intentionally doped (n.i.d.) GaN and AlGaN layers have the background n–type concentration of 1×10^{16} cm^{-3}, determined by producer. By means of Si dopant the n–type doping of specified AlGaN layers can be increased. Two of five layer structures used contain Si doping of 2×10^{18} cm^{-3} (F1749) and 5×10^{18} cm^{-3} (F1750). The structure compositions and thicknesses were chosen to yield the possibility to compare them with each other, i.e. n.i.d. samples can be compared with and without GaN cap layer (S2661 and F1438), the influence of the doping between n.i.d. sample, 2×10^{18}, and 5×10^{18} cm^{-3} doped samples (F1438, F1749, and F1750) can be investigated, and finally the influence of additional SiC substrate cleaning done by CREE Inc. (F1435 and F1438) can be examined.

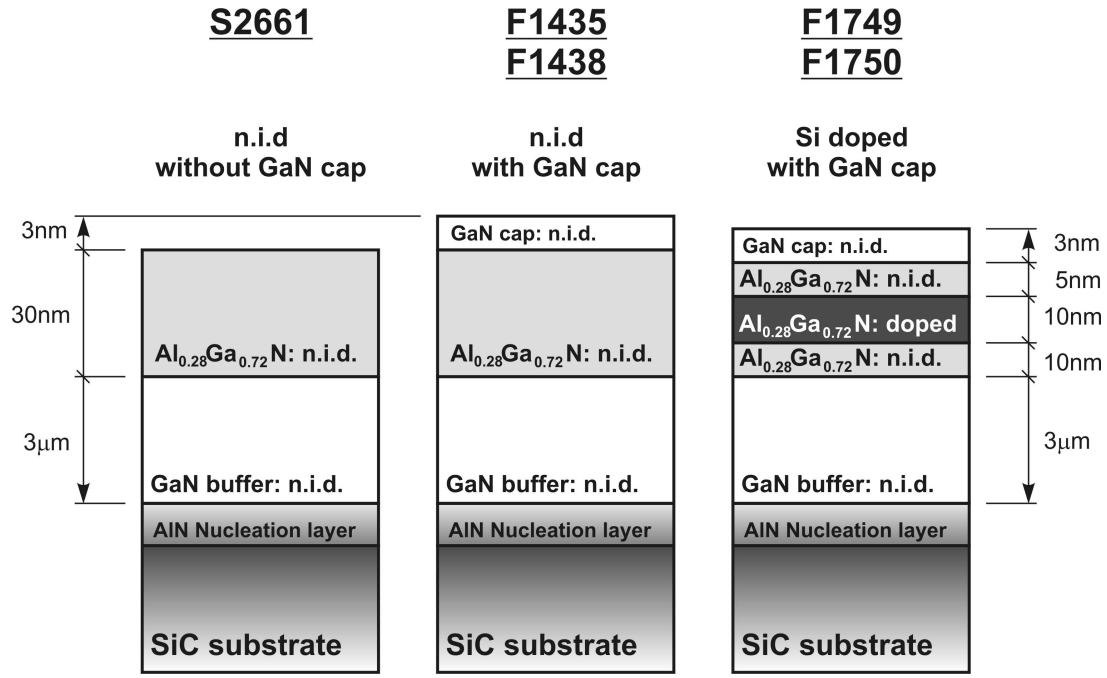


Figure 7.1: Overview of layer structures used.

7.2 Energy band diagram simulations

Simulation of the energy band diagram yields important information about the layer structure and the carrier concentrations which can help to prove suitability of the chosen layer structure for the fabrication of HEMTs. For this purpose we have used the WinGreen software package developed at our institute by K. M. Indlekofer and J. Malindretos [76]. The calculation of energy levels and charge distributions is based on realtime Green's functions and self–consistent solution of Schrödinger and Poisson equations.

The simulation of GaN–based heterojunctions requires knowledge of various constants. Besides the standard material parameters as the lattice constants, relative permittivity, band gap, and effective electron and whole masses also the polarisation induced charge density near the AlGaN/GaN interfaces is required. For simulation, this charge density is modelled as a fixed sheet charge (fully ionised donors and/or acceptors) near the interface. The vertical position of this charge density depends on the polarity conditions of layers to be simulated (see chapter 3). Due to Ga–faced structures to be simulated we have positioned the sheet polarisation induced charge density above the AlGaN/GaN interface (figure 3.4). The sheet carrier concentration calculated by Ambacher *et al.* [14, 15] of $1.63\times10^{13}\,\mathrm{cm}^{-2}$ and the GaN and AlGaN background concentration of $1.0\times10^{16}\,\mathrm{cm}^{-3}$ were used for modelling. The used material parameters are summarised in table 7.2. Figure 7.2 shows the simulated band diagrams and the charge densities for all layer structures using Fermi level pinning at the surface of 1.1 eV and zero buffer potential. The influence of the GaN cap layer is evident from this simulation: Besides a decrease of the sheet carrier concentration in 2DEG an additional barrier is formed near the surface (GaN cap/AlGaN interface) which is a crucial issue to reduce the gate leakage current. This is important especially for doped structures where higher gate leakage is expected due to additionally doped AlGaN layer. On the other side, an increase of the doping level increases the sheet carrier concentration of the 2DEG as can be seen from the simulation results of samples F1749 and F1750.

The simulated results will be compared with experimental results in section "Electrical characterisation of layer structures".

Parameter		**GaN (wurtzite)**	**AlN**
Relative permittivity	ε_r	9.5	8.5
Energy band gap	E_g (eV)	3.440	6.202
Effective electron mass	m_e	0.228 m_0	0.480 m_0
Effective hole mass	m_h	0.800 m_0	1.000 m_0

Table 7.2: Material parameters used for WinGreen simulation at room temperature (300 K).

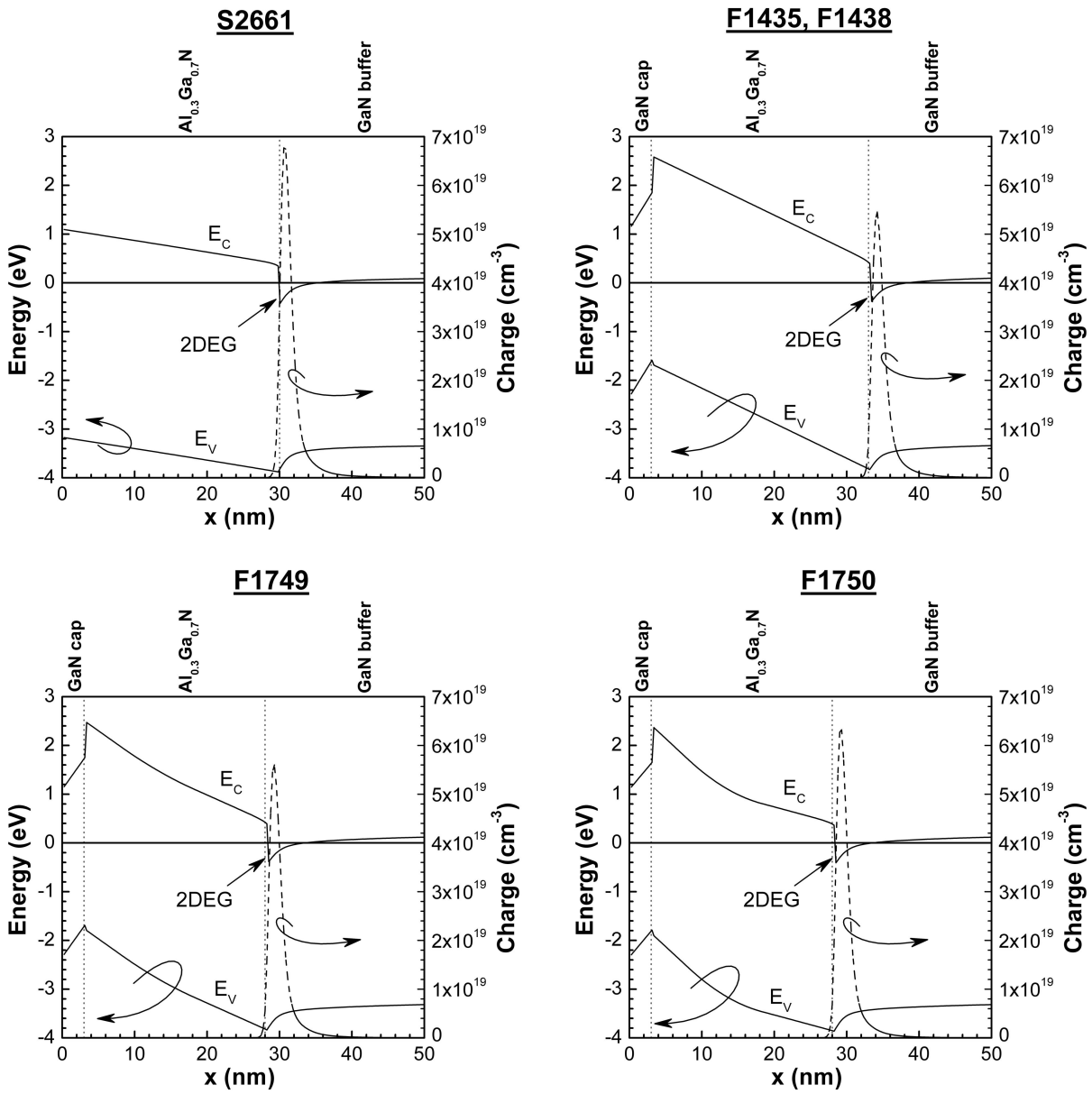


Figure 7.2: Simulation of energy bands and charge densities in used layer structures by means of WinGreen.

7.3 Atomic Force Microscopy (AFM)

Fabrication of HEMT devices depends on the technological process as well as on the quality of the semiconducting layers. One of the layer properties which has to be controlled properly by the growth process is the surface roughness. A frequently used method to determine the surface roughness is Atomic Force Microscopy (AFM). The principle of this method is described in chapter 5.

The surface roughness of all introduced samples has been controlled by AFM before

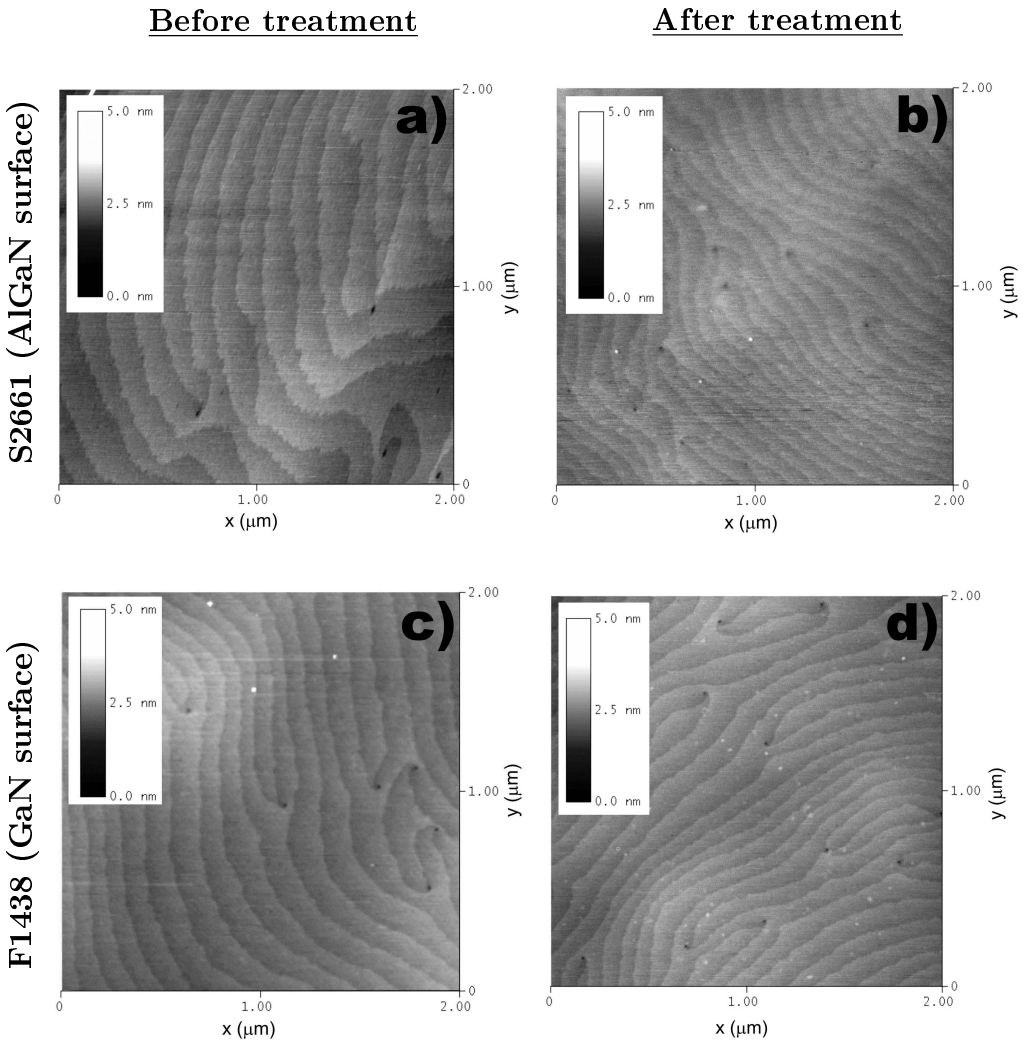


Figure 7.3: AFM scans of AlGaN (a and b) and GaN (c and d) surface before (left) and after (right) cleaning procedure.

processing. The root–mean–square roughness has been determined to be in the range of 0.12 nm – 0.22 nm for all probes. This is comparable with the best results published in literature [97, 98].

But also the processing technology, especially the surface cleaning and treatment in acids, can influence the roughness. Therefore we have made additional AFM scan in cooperation with Dr. T. Stoica before and after standard treatment to find out about the surface changes. The cleaning procedure consists of:

- Acetone & Propanol cleaning,
- HF(1) : H_2O(2) for 2 min,
- HCl(1) : H_2O(2) for 2 min,
- H_2O_2(1) : NH_3(2) for 10 min.

The AFM–scans before and after cleaning and the evaluation procedure of AFM–data have been done by Dr. T. Stoica and are shown in figure 7.3.

The scans have been analysed and the root–mean–square roughness (rms) has been calculated using Nanoscope III software package. Both, n.i.d. GaN and n.i.d. $Al_{0.28}Ga_{0.72}N$, surfaces typically show terraced–like shape. Important to note is the occurrence of deeper pits at the beginning and/or the end of some terraces which have been also taken into account in rms calculation.

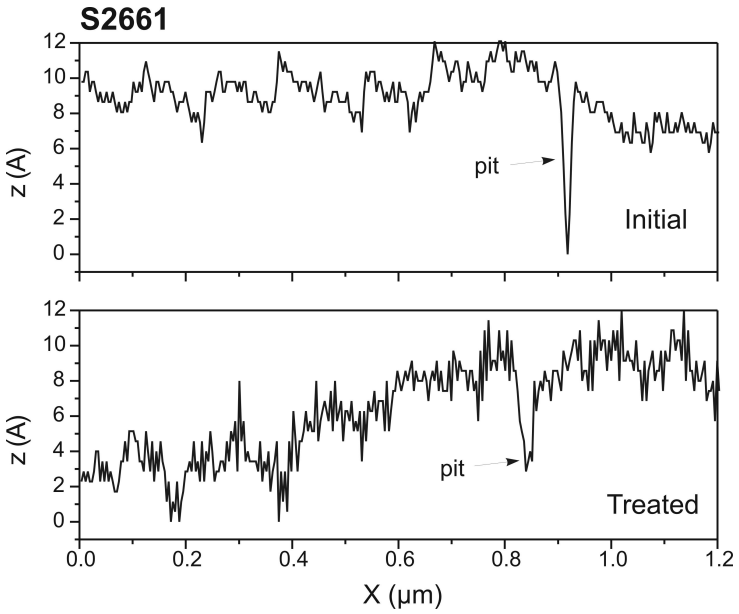


Figure 7.4: The cross section of the n.i.d. $Al_{0.28}Ga_{0.72}N$ surfaces used for device fabrication before and after surface treatment.

The AlGaN surface shows less defined steps and shallower pits after the treatment (see figure 7.4) and a small increase of the rms roughness from 0.13 nm to 0.16 nm before and after cleaning procedure, respectively. A $1 \times 1\,\mu m^2$ surface area has been measured including atomic steps.

The GaN surface, in contrast to the AlGaN surface, shows deeper pits and a decrease of rms from 0.14 nm to 0.12 nm after the treatment (also measured for a surface area of $1 \times 1\,\mu m^2$). The cross section of the analysed surface is illustrated in figure 7.5.

Summary, the results show very small surface roughness and insignificant surface changes after the treatment.

7.4 Electrical characterisation of layer structures

After the layer structures have been investigated by Atomic Force Microscopy electrical characterisation of layer structures is the second step needed to be done before

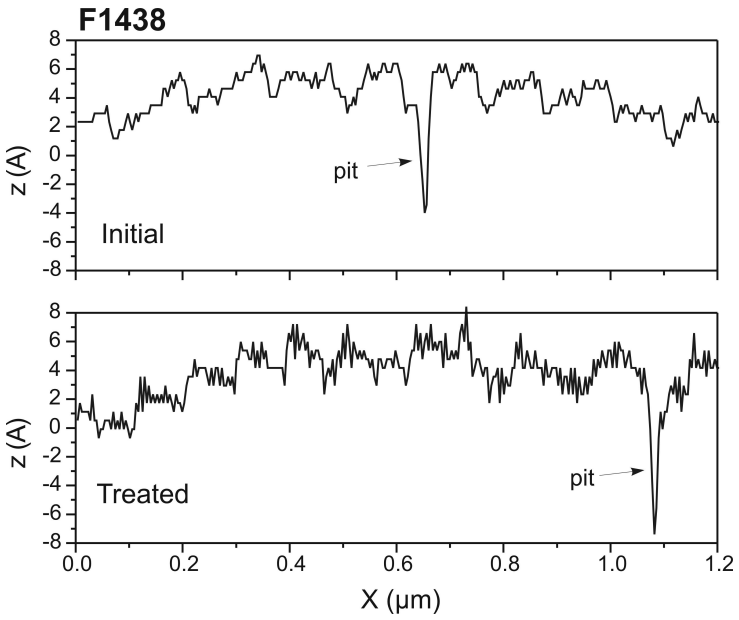


Figure 7.5: The cross section of the n.i.d. GaN surfaces used for device fabrication before and after surface treatment.

device processing. This characterisation consists of Hall effect, capacitance–voltage, and Transmission Line Model (TLM) measurements as theoretically introduced in chapter 5.

The Hall effect measurements have been performed using two types of Van der Pauw patterns. The first Van der Pauw pattern of $5 \times 5\,\mathrm{mm}^2$ area size was used for material characterisation at room temperature (300 K) and at 77 K. The aim was to confirm the 2DEG formation near the AlGaN/GaN interface. The second Van der Pauw pattern of $0.3 \times 0.3\,\mathrm{mm}^2$ area size was used for an exact material characterisation as close as possible to the fabricated devices and for investigation of passivation influences on the material properties at room temperature. Chapter 6 gives detailed introduction to the latter Van der Pauw pattern.

The capacitance–voltage (CV) measurements of Schottky diodes with different surface area were performed by means of Agilent 4294A parameter analyser at 1 MHz. From measurement data the sheet carrier concentration n_s can be derived using equations 5.9 and 5.10. In combination with sheet resistance R_{sheet} determined from TLM measurements the channel mobility μ_n can be calculated from equation 5.6. CV curves for all samples are documented in figure 7.6. Zero voltage capacitance c_0 corresponding to the distance between the Schottky interface and 2DEG ($d_i + \Delta d$) (eq. 4.3) is in a good agreement with layer structures. Also the threshold voltage V_{th} (where the capacitance decrease abruptly) well corresponds to the sheet carrier concentration of electrons in channel for each structure. Measured Hall effect results compared with results from capacitance–voltage and TLM measurements are summarised in table 7.3.

The sheet carrier concentration n_s and the mobility μ_n calculated from CV and TLM

measurements are in a good agreement with Hall effect measurements and WinGreen simulations. The sheet carrier concentration of the n.i.d. samples with GaN cap (F1435, F1438) is smaller in comparison to the n.i.d. sample without GaN cap (S2661). This can be explained as a consequence of the additional barrier at the GaN(cap)/AlGaN interface which rises up the conduction band relatively to the Fermi level in the quantum well area. The rise up of the conduction band of the samples with GaN cap explains the decrease of the sheet carrier concentration in the quantum well. With increased doping concentration of the AlGaN barrier layer the sheet carrier concentration of 2DEG increased from $\sim 7.5 \times 10^{12}\,\mathrm{cm}^{-2}$ for n.i.d. sample to $\sim 1 \times 10^{13}\,\mathrm{cm}^{-2}$ for $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped sample while the channel mobility slightly decreased from $\sim 1900\,\mathrm{cm}^2/\mathrm{Vs}$ to $\sim 1663\,\mathrm{cm}^2/\mathrm{Vs}$ for n.i.d and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped sample, respectively. The sheet resistance R_{sheet} decreased with increasing doping concentration. Very high mobility in the range of $3745 - 9755\,\mathrm{cm}^2/\mathrm{Vs}$ measured at 77 K confirmed the 2DEG formation.

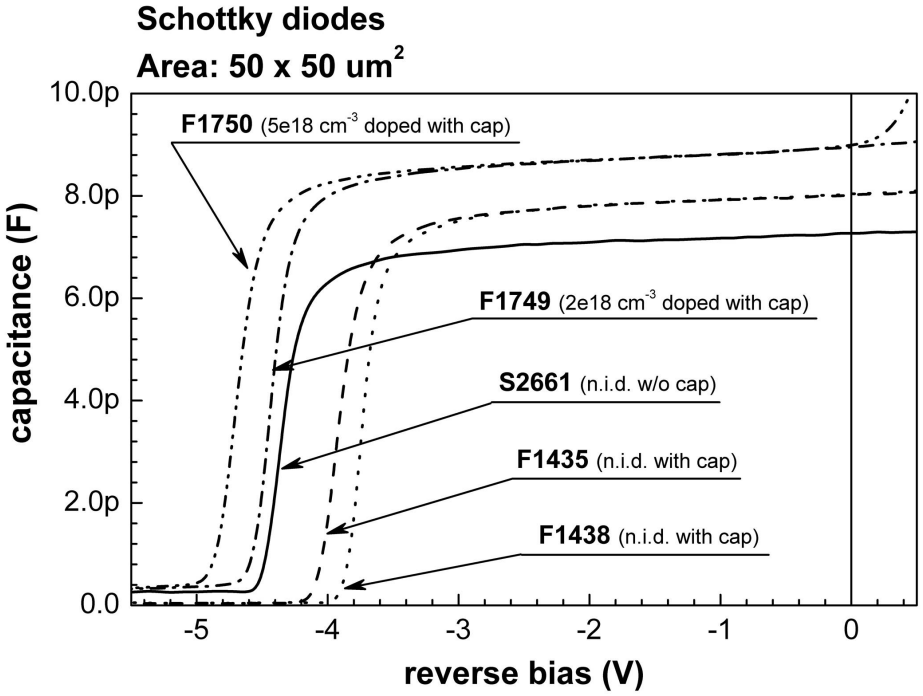


Figure 7.6: CV measurements of Schottky diodes on investigated layer structures

Sample		**S2661**	**F1435**	**F1438**	**F1749**	**F1750**
TLM	R_c $(\Omega \cdot mm)$	0.355	0.418	0.390	0.239	0.310
	R_{sheet} $(\Omega/square)$	549	438	414	354	308
	ρ_c $(\Omega \cdot mm)$	2.29×10^{-6}	3.99×10^{-6}	3.67×10^{-6}	1.61×10^{-6}	3.11×10^{-6}
	L (μm)	0.65	0.95	0.94	0.67	1.01
CV	n_s (cm^{-2})	7.74×10^{12}	7.37×10^{12}	6.93×10^{12}	9.35×10^{12}	10.7×10^{12}
	μ_n (cm^2/Vs)	1469	1933	2176	1886	1894
Hall effect	n_s (cm^{-2})	7.94×10^{12}	7.77×10^{12}	6.95×10^{12}	8.19×10^{12}	9.72×10^{12}
$(0.3 \times 0.3\text{mm}^2)$	R_{sheet} $(\Omega/square)$	464	423	466	428	387
300 K	μ_n (cm^2/Vs)	1695	1900	1930	1780	1663
Hall effect	n_s (cm^{-2})	5.17×10^{12}	7.58×10^{12}	7.53×10^{12}	9.52×10^{12}	10.8×10^{12}
$(5 \times 5\text{mm}^2)$	R_{sheet} $(\Omega/square)$	507	453	448	407	404
300 K	μ_n (cm^2/Vs)	2420	1823	1855	1618	1430
Hall effect	n_s (cm^{-2})	6.42×10^{12}	8.89×10^{12}	8.15×10^{12}	10.6×10^{12}	11.5×10^{12}
$(5 \times 5\text{mm}^2)$	R_{sheet} $(\Omega/square)$	263	88	78	89	97
77 K	μ_n (cm^2/Vs)	3745	8140	9755	6683	5595

Table 7.3: Electrical parameters of layer structures evaluated from CV, TLM, and Hall effect measurements.

Chapter 8

Unpassivated AlGaN/GaN HEMTs on SiC

After having characterised the semiconducting layers in the previous chapter the attention is now drawn towards the HEMT devices themselves. In particular, a static characterisation of the AlGaN/GaN HEMTs is performed followed by a discussion of the drift mobility issue which precedes the treatment of thermal effects. After these issues a rf characterisation and pulse measurements are performed. A consideration of output power performance concludes this chapter.

It has to be noted that this chapter exclusively treats unpassivated devices.

8.1 Static characterisation

Measurement of the output and the transfer characteristic is the basic method for HEMT characterisation, while breakdown measurements can be considered as an important method to gather information regarding limits of the device. Using these measurements the functionality of the device and the quality of the layer structure can be analysed.

All measurements are performed by means of Agilent E5270A semiconductor analyser controlled by a computer. The measurement system allows to measure in the bias range of -200 V to +200 V and the current range is up to 1 A with femto-amp accuracy. The gate-source and the drain-source biases are controlled simultaneously and the gate and drain currents are read subsequently. The schematic draw of the measurement system is shown in figure 8.1.

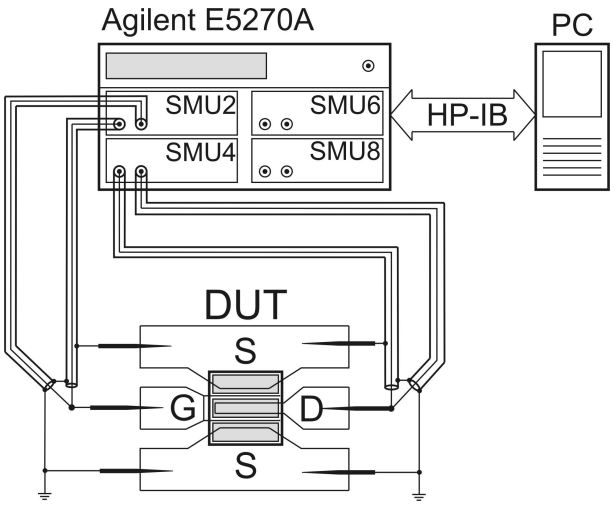


Figure 8.1: Measurement system used for dc characterisation of AlGaN/GaN HEMTs.

8.1.1 Static output and transfer characteristics

The measured output and transfer characteristics were used for evaluation of parameters as the maximum drain current I_d^{sat}, threshold voltage V_{th}, extrinsic transconductance g_m and leakage currents. The typical output and transfer characteristics measured for $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped sample are shown in figure 8.2. Well known AlGaN/GaN HEMT behaviour is observable by output characteristics, i.e. decreasing drain current with increasing drain-source bias in saturation region. This is caused by self heating effects and is dependent on the thermal conductivity of the used substrate.

A comparison of HEMT parameters fabricated using different layer structures can be found in figure 8.3 and important parameters are collected in table 8.1. Devices fabricated on doped layer structures exhibit better dc performances in comparison to undoped ones. The drain saturation current I_d^{sat} increases with increasing doping level while the threshold voltage is shifted to more negative values. This is in agreement with Hall measurements collected in table 7.3 where the doped samples exhibit higher sheet carrier concentrations in the 2DEG in comparison to undoped samples. Better performance of the doped samples can be explained as the doping of the buffer layer acts as an additional source of electrons for the 2DEG, increasing the sheet carrier concentration of the 2DEG. It is necessary to stress again, that until now it is not clear what the source of such a high sheet concentration of electrons in the 2DEG might be. An already mentioned and widely accepted explanation is that natural donor–like surface states are the source of electrons.

But doping of AlGaN/GaN HEMTs gives rise for negative influences as well. As is shown in table 8.3 and will be discussed in the next part, an increasing doping level increases the gate leakage current markedly from $\sim 2 \times 10^{-9}\,\mathrm{A/mm}$ to $1.5 \times 10^{-6}\,\mathrm{A/mm}$.

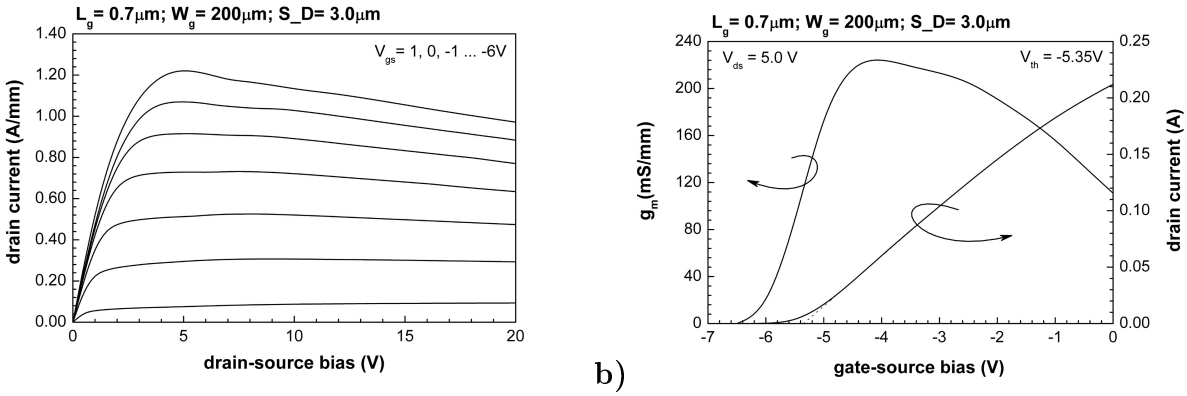


Figure 8.2: Typical output (a) and transfer (b) characteristics of 5×10^{18} doped HEMT.

Sample	**Doping** ($\mathbf{cm^{-3}}$)	**GaN cap**	I_d^{sat} (A/mm)	g_m (mS/mm)	V_{th} (V)	**gate leakage** (A/mm)
S2661	no	no	0.67	174	-3.48	2.30×10^{-9}
F1435	no	yes	0.69	180	-3.10	2.07×10^{-8}
F1438	no	yes	0.73	185	-3.32	4.65×10^{-9}
F1749	2×10^{18}	yes	1.06	214	-4.54	1.27×10^{-7}
F1750	5×10^{18}	yes	1.12	207	-5.18	1.51×10^{-6}

Table 8.1: Important parameters evaluated from dc measurements on fabricated HEMTs with $L_g = 0.9\mu m$ and $S_D = 4.0\mu m$. Leakage current was evaluated at $V_{gs} = -6V$ and $V_{ds} = 0V$.

This is directly connected to the breakdown voltage of the transistor which decreases with increasing doping level.

8.1.2 Breakdown voltage

Breakdown voltage and its relationship to leakage currents needs to be discussed because of its influence on output power. As was already shown in figure 4.8 and according to equation 4.30, the parameters which basically limit the output power are the drain saturation current I_d^{sat} and the breakdown voltage V_{br}. For maximum output power a maximum I_d^{sat} and V_{br} are needed. We have already shown the dependence and improvement of I_d^{sat} by additional doping of AlGaN buffer layer. This section will introduce a non-destructive Current-injection measurement technique for breakdown voltage determination. Possibilities to improve breakdown voltage will be discussed also.

The Current–injection technique is based on dc measurement under exact conditions where the source is grounded and a fixed predefined current is injected into the drain. The gate-source bias is ramped down from on–state to below threshold bias and the drain-source bias with the gate current are monitored [10, 105]. The drain-source breakdown

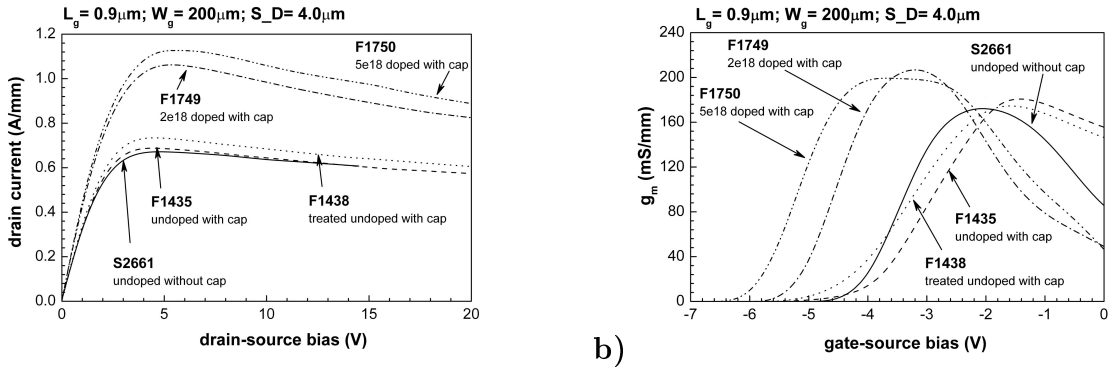


Figure 8.3: Comparison of output characteristics (a) and extrinsic transconductance (b) of all fabricated samples.

V_{br} is obtained as a maximum measured V_{ds} irrespective of V_{gs}. The gate-drain voltage dependence on V_{gs} can be expressed by equation:

$$V_{gd} = V_{ds} - V_{gs}, \tag{8.1}$$

where V_{gd} is the gate-drain bias. From this equation the gate-drain breakdown bias V_{br}^{gd} can be determined as a bias where the magnitude of the measured drain current is equal to gate current: $I_d = -I_g$ (see figure 8.4 a). Injected drain current for off–state breakdown condition depends on the drain leakage current and is typically $\sim 1 mA/mm$. In our case, an injected drain current was chosen to be of $25\, mA/mm$. Smaller injected currents could distort evaluation of the breakdown voltage due to very smooth knee of the current–voltage curve before breakdown.

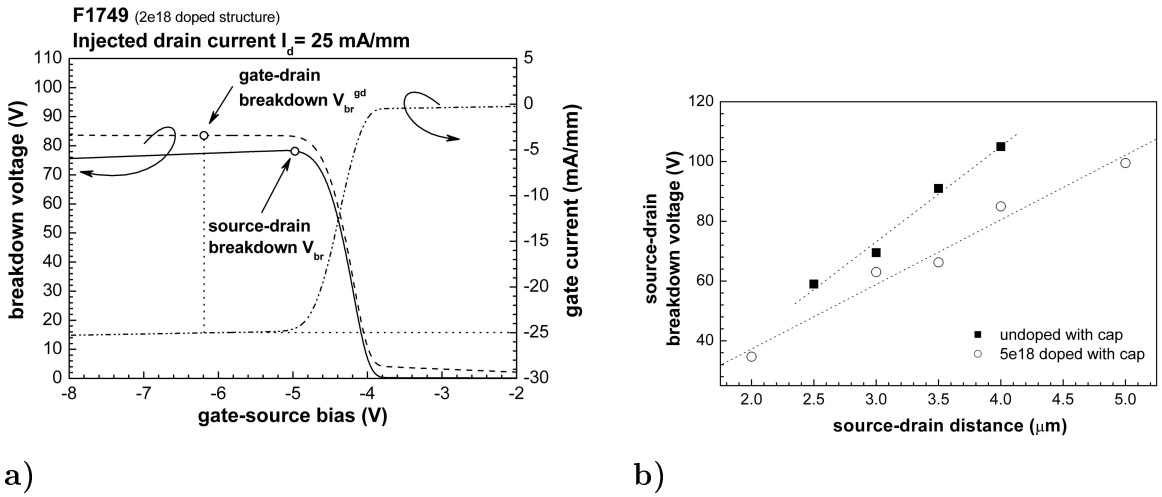


Figure 8.4: Principle of breakdown voltage evaluation (a) and measured drain-source breakdown voltage dependence on the source–drain distance for undoped and doped samples (b).

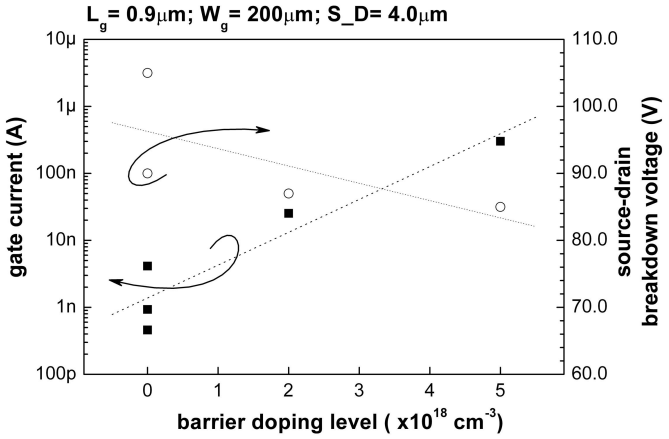
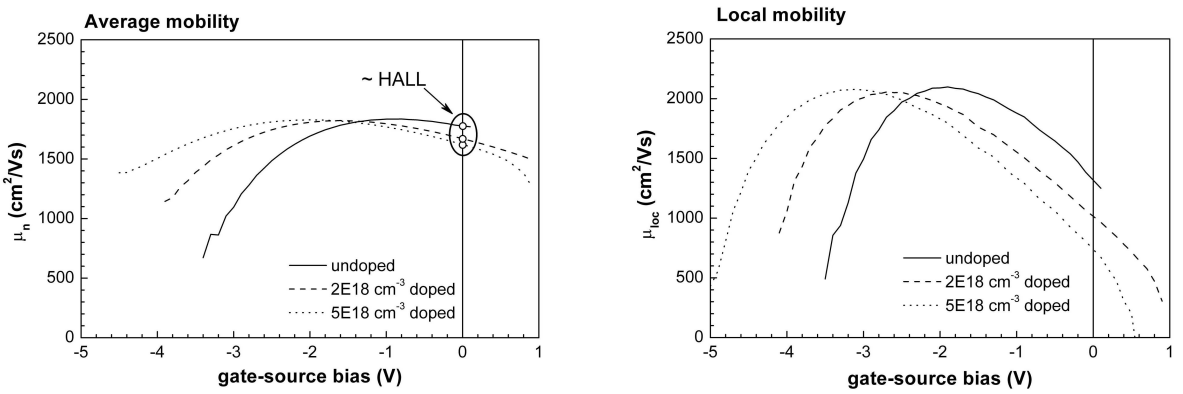


Figure 8.5: Dependence of the gate leakage current and the breakdown voltage on the barrier doping level.

The breakdown voltage was always derived statistically from measurements of various identical devices. All results published in this work are mean values from these measurements. The dependence of the source–drain breakdown voltage on the source–drain distance is shown in figure 8.4 b. With increasing S_D distance the breakdown voltage rises. Figure 8.4 b also introduces the comparison of undoped and intentionally doped sample. As was expected, the doped sample showed smaller breakdown voltages in comparison to undoped ones due to higher gate leakage currents. The correlation between gate leakage current and source–drain breakdown voltage for fabricated undoped and doped structures is shown in figure 8.5. With increasing gate leakage current the breakdown voltage decreases. It becomes clear, that reducing the gate leakage current by technological advances not only aims to reduce power consumptions but also tries to increase breakdown voltages.

8.2 Drift mobility of HEMTs

Until now the heterostructures used for device fabrication were characterised by standard Hall effect measurements. Hall characterisation shows the mean mobility of the carriers and does not allow us to determine the mobility distribution or existence of a parallel conductive layer. Mobility distribution can be determined by channel conductivity measurements on HEMTs with large gate length, in combination with capacitance measurements. The channel conductivity measurements were done at our institute by M. Marso *et al.* and aimed to compare non–intentionally doped, $2 \times 10^{18}\,\mathrm{cm}^{-3}$ doped, and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped samples with GaN cap with each other. Measured devices are named in the mask layout as FAT–FETs (see figure 6.2). To evaluate the drift mobility, the



a) b)

Figure 8.6: Dependence of the average (a) and local (b) mobility on doping concentration of the layer structure and the gate–source bias [30].

channel conductance g_{chi} has to be determined according to equation 4.20 and from linear region measurements of HEMT at drain–source biases of 0.1 to 0.3 V. The measured value of the channel conductance must be corrected for the series source and drain resistances. These were measured on HEMTs with $2\,\mu m$ gate length using the charge control model and were always less than 10% of the channel resistance of HEMTs with the gate length of $50\,\mu m$. The average drift mobility μ_n is then evaluated using equation 4.23 where a good agreement of the mobility obtained by Hall effect measurements and the average drift mobility by zero gate–source bias measured by channel conductance method is obtained (see table 8.2).

Additionally, the local mobility μ_{loc} defined as the mobility of carriers that are added into channel with gate voltage increase, expressed by [30, 109]:

$$\mu_{loc} = \frac{L_g^2 \cdot \Delta g_{chi}}{C_{gs} \cdot \Delta V_{gs}}, \tag{8.2}$$

was evaluated from measurements. Δg_{chi} represents the change of the channel conductance caused by the change of the gate–source bias ΔV_{gs}.

Sample	**Doping** ($\mathbf{cm^{-3}}$)	**Hall effect determ.** μ_n ($\mathbf{cm^2/Vs}$)	**Channel conductivity determ.** μ_n ($\mathbf{cm^2/Vs}$) **by** $V_{gs} = 0\,V$
F1438	n.i.d.	1930	1800
F1749	2×10^{18}	1780	1670
F1750	5×10^{18}	1663	1620

Table 8.2: Comparison of electron mobility and sheet carrier density of layer structures determined by Hall effect measurements and channel conductivity method.

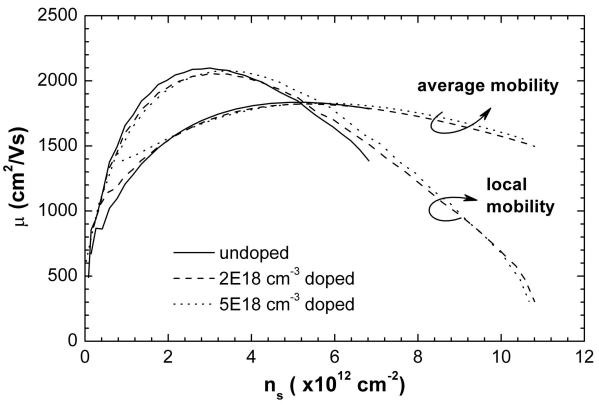


Figure 8.7: Dependence of the average and local mobility on the sheet carrier concentration for different doping level [106].

Peak average and local mobilities of $1825\,\mathrm{cm}^2/\mathrm{Vs}$ and $2100\,\mathrm{cm}^2/\mathrm{Vs}$ were measured, respectively, independent of the doping concentration of the supply layer (see figures 8.6 and 8.7). This confirms, that channel electron mobility is not influenced by the donor atoms in the AlGaN carrier supply layer. The maximum local mobility of $2100\,\mathrm{cm}^2/\mathrm{Vs}$ was determined by the sheet carrier concentration of $3 \times 10^{12}\,\mathrm{cm}^{-2}$. The activation of the parallel channel in the carrier supply layer was observed above $10^{13}\,\mathrm{cm}^{-2}$ (sharp drop of the local mobility). Similar results were published by Ridley *et al.* [110, 111], where the upper limit of AlGaN/GaN heterostructure of $2000\,\mathrm{cm}^2/\mathrm{Vs}$ by $2 \times 10^{12}\,\mathrm{cm}^{-2}$ is shown.

8.3 Thermal effects – Channel temperature

It is well known, that GaN–based materials are extremely stable at very high temperatures. For practical application, it is important to know about the behaviour of HEMTs for elevated temperatures and what is the maximum temperature for which devices are still working.

Therefore, we have investigated the dc behaviour of AlGaN/GaN HEMTs on SiC substrate at elevated temperatures. Obtained data were compared with those published on AlGaN/GaN HEMTs with sapphire and silicon substrates. Using thermal effects theory introduced in chapter 4 the channel temperature dependence on the dissipation power was calculated and compared with other used substrates.

Devices were characterised by Agilent E5270A semiconductor analyser using the same scheme as before. The wafer with fabricated HEMTs was placed in a cryostat with the tunable temperature from $77\,K$ to $540\,K$. The devices were tested for elevated temperatures in the range from $300\,K$ to $540\,K$. From the measured characteristics the

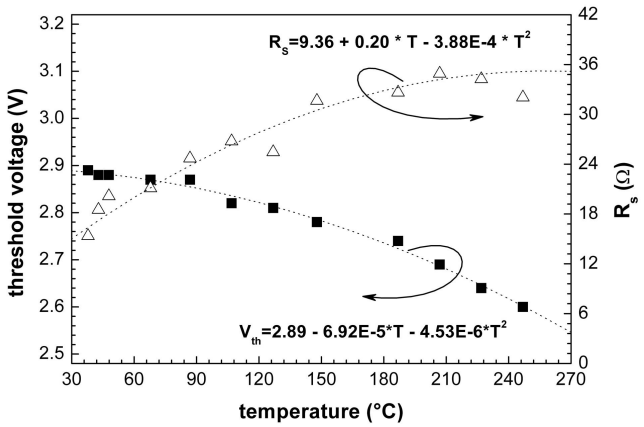


Figure 8.8: Temperature dependence of the serial resistance and the threshold voltage for the sample grown on SiC substrate.

temperature dependencies of the drain saturation current I_d^{sat} (figure 8.9 a), the threshold voltage V_{th}, and the serial resistance R_s (figure 8.8) were evaluated. The non–linear temperature dependencies of V_{th} and R_s were polynomially fitted and used for the channel temperature calculation according equation 4.43. The drain current dependence on the saturation velocity change $\Delta\nu_{sat}$ was assumed to be constant. This was done due to theoretical calculations which shows considerably smaller temperature sensitivity of ν_{sat} in GaN in comparison to other III–V material systems. Also strong polarisation fields in AlGaN/GaN quantum well further eliminate electron mobility dependence on temperature [33].

Figure 8.9 a shows much better dc performance of AlGaN/GaN HEMTs fabricated on SiC substrates at elevated temperatures in comparison to sapphire substrate where at $250°C$ the drain saturation current decreased to 73 % of its room temperature value on SiC contrary to 39 % on sapphire. This confirmed better thermal conductance of SiC substrate. The comparison of SiC and silicon substrates did not show any considerable difference in the change of the drain saturation current with the temperature. The channel temperature evaluated from temperature measurements on different substrates is shown in figure 8.9 b. The data for sapphire and silicon substrates were published in literature [33] while our measurements on SiC were added in advance. One can see that AlGaN/GaN HEMTs on SiC substrate exhibit markedly smaller channel temperatures in comparison to sapphire and Si substrates. Lower channel temperature of HEMTs on SiC substrate in comparison to Si substrate originates from smaller temperature dependence of the serial resistance and the threshold voltage. For the dissipation power of $6\,W/mm$ the channel temperature of $320°C$, $95°C$, and $62.2°C$ were examined for sapphire, silicon, and SiC, respectively. This indicates smaller temperature dependence, higher stability, and smaller

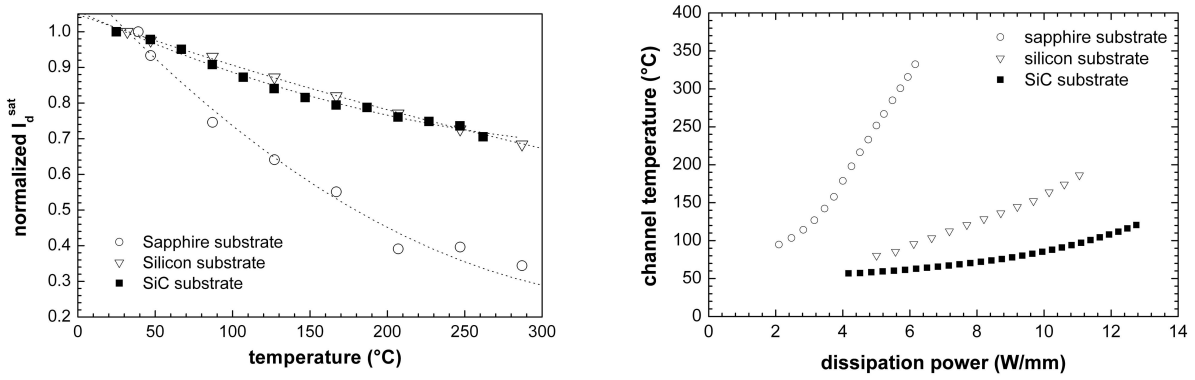


Figure 8.9: Normalised temperature dependence of the drain saturation current (a) and channel temperature dependence on the dissipation power (b) of AlGaN/GaN HEMTs with sapphire, silicon, and SiC substrates (values for sapphire and silicon substrates are from literature [33, 34]).

degradation of structures using SiC substrate. From these results we can expect better power performances without necessity of additional device cooling.

8.4 RF characterisation

Boundary frequencies are additional parameters investigated in our labs. As was introduced in the theoretical part, f_T and f_{max} frequencies define the frequency range where the HEMT shows amplifying behaviour. This is important information to be used for power measurements.

The boundary frequencies were evaluated from s–parameter measurements using forward current gain h_{21} and maximum unilateral transducer power gain Gu, defined as:

$$h_{21} = \frac{-s_{21}}{(1 - s_{11}) \cdot (1 + s_{22}) + s_{12} \cdot s_{21}} \tag{8.3}$$

$$Gu = \frac{|s_{21}|^2}{(1 - |s_{11}|^2) \cdot (1 - |s_{22}|^2)} \tag{8.4}$$

f_T is then determined as the frequency where $h_{21}^2 = 0$, and f_{max} is the frequency where $Gu = 0$ (see figure 8.10).

S–parameter measurements were done in a frequency range up to $110\,GHz$ using a HP 8510C Network Analyzer. Devices were measured for gate–source bias (V_{gs}) in the range from $+1\,V$ to V_{th} and drain–source bias (V_{ds}) in the range from 0 to $20\,V$. Afterwards, the peak cut–off frequency was evaluated. The gate–source bias, resulting in maximum

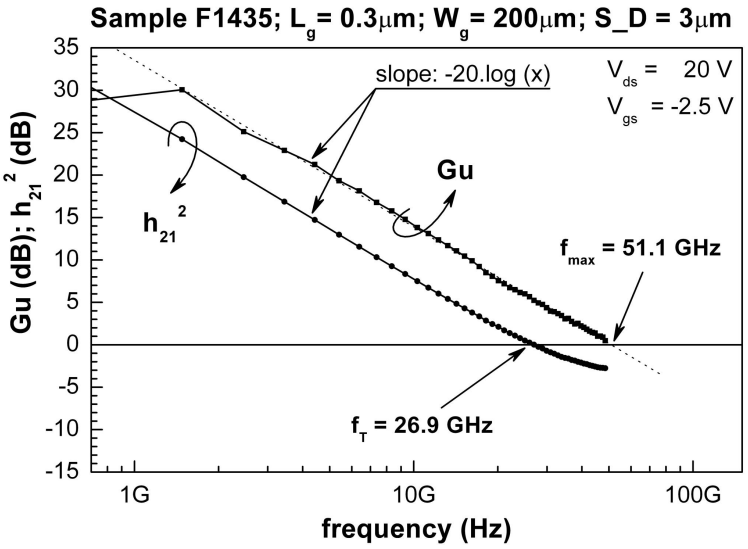
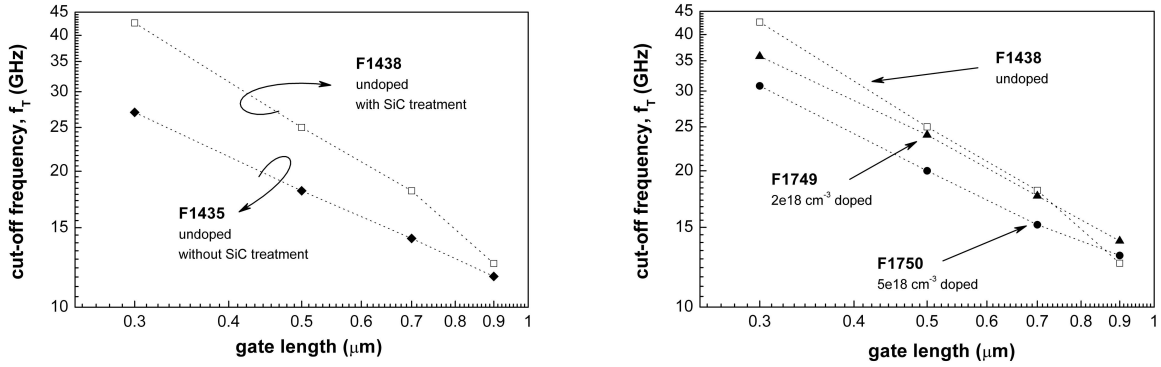


Figure 8.10: h_{21}^2 = f($frequency$) and Gu = f($frequency$) functions evaluated from s–parameter measurements of HEMT with $L_g = 0.3\mu m$ fabricated on undoped structure (F1435).

f_T from rf measurements, was in good agreement with the gate–source bias yielding peak extrinsic transconductance g_m evaluated from dc measurements. An example of evaluated f_T and f_{max} from s–parameter measurements on undoped sample for $V_{gs} = -2,5\,V$ and $V_{ds} = 20\,V$ is shown in figure 8.10.

RF measurements of fabricated samples show differences in cut–off frequencies between undoped samples F1435, F1438 and also between undoped and doped samples (see figure 8.11). Contrary to this, the drift–mobility results obtained in the previous section exhibit no influence of modulation doping on channel mobility and therefore similar rf behaviour for all samples was expected. Due to this discrepancy we assumed that additional effects have to be involved influencing rf behaviour. Therefore, we decided to investigate the gate-source capacitance C_{gs} and saturation velocity ν_{sat} of HEMTs with sub-micro gate length to determine the reason for such difference in f_T.

Gate–source capacitances were evaluated using the TOPAS software package developed by IMST GmbH. This package helps us to evaluate intrinsic parameters of HEMT from s–parameter measurements according to the small–signal model of HEMT introduced in figure 4.5. Evaluation resulted in more that two times higher gate–source capacitance of the F1435 sample in comparison to the other, undoped and doped structures, shown in figure 8.12 a. This explains difference in cut–off frequencies between the undoped samples F1435 and F1438 (see figure 8.11 a). The cut–off frequency of undoped samples is affected due to different C_{gs} according equation 4.26 and therefore the sample F1435 with higher gate–source capacitance exhibits smaller f_T in comparison to F1438 with consider-



a) b)

Figure 8.11: Cut–off frequency comparison of devices fabricated on differently treated SiC substrates (a) and undoped and doped layer structures (b).

ably smaller C_{gs}. The higher gate–source capacitance of sample F1435 can be explained by higher parasitic interface charge under the gate electrode which can be influenced by suitable technological process.

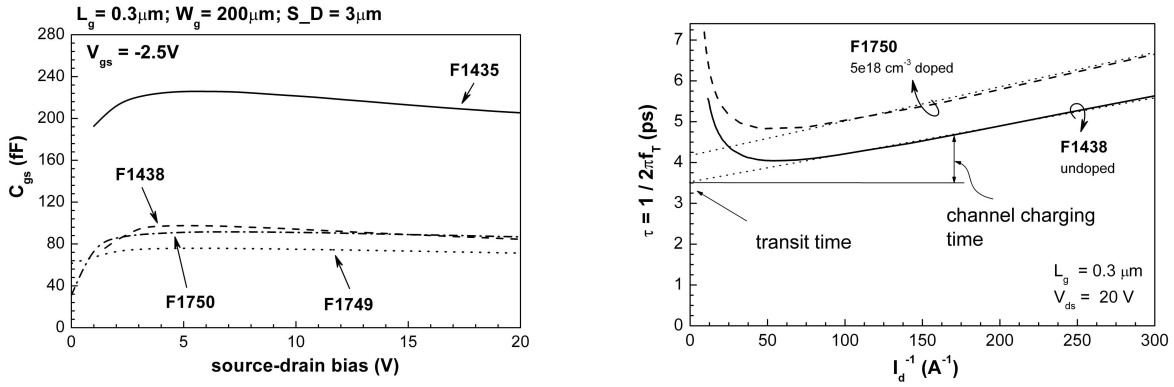
But the gate–source capacitance does not explain the rf differences between samples F1438 and F1750 which exhibit nearly the same C_{gs}. Therefore, an evaluation of the saturation velocity was done to identify if this could be the reason for different f_T.

To evaluate the saturation velocity ν_{sat} from rf measurements the total delay time $\tau = 1/2\pi f_T$ was plotted as a function of the inverse of the drain current $1/I_d$ at constant V_{ds} [106–108] (figure 8.12 b). The total delay time τ is defined as the sum of the transit time and the parasitic channel charging time. The parasitic channel charging time, which is proportional to the channel resistance, is inverse by proportional to the drain current I_d. Therefore, with increasing I_d the total delay time τ decreases linearly (true for low drain currents). Then the extrapolated intersect at $1/I_d = 0$ corresponds to the transit time $\tau_{transit}$ under the gate, defined as:

$$\tau_{transit} = \frac{L_g}{\nu_{sat}} \tag{8.5}$$

From evaluation of the transit time the 5×10^{18} cm^{-3} doped sample (F1750) shows reduced saturation velocity of 18 % in comparison to the undoped (F1438). We consider this as the reason for slightly dropped boundary frequencies of the doped sample F1750 where the doped barrier layer does not influence the electron mobility in 2DEG but reduces the saturation velocity.

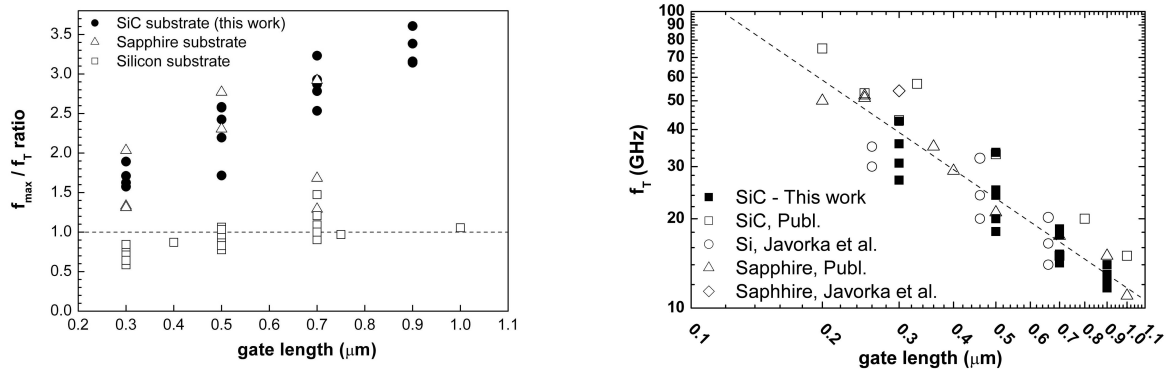
Finally, the f_{max}/f_T ratio of fabricated HEMTs on SiC substrate was evaluated. It is known from theory, that parasitic conduction of the substrate causes an abrupt decrease



a) b)

Figure 8.12: Gate-source capacitance of fabricated samples evaluated by Topas from s–parameter measurements (a) and the transit time of our HEMTs (b) [106].

of the f_{max} and also of the f_{max}/f_T ratio [10]. To show that SiC substrates yield HEMTs of better quality and higher resistance, we compared our results with HEMTs based on sapphire and silicon substrates that were either published in literature or fabricated in our labs (figure 8.13 a). Measurements showed comparable ratios of f_{max}/f_T of SiC and sapphire in the range of 1.7 to 3.5 depending on the gate length. Silicon substrate with its high parasitic conductance exhibits evidently smaller values of f_{max}/f_T of 0.7 to 1.1. Obtained rf results of our HEMTs fabricated on SiC substrate and published data are fully comparable, as shown in figure 8.13 b. This proves high quality and good functionality of our devices.



a) b)

Figure 8.13: f_{max}/f_T ratio (a) and f_T (b) of AlGaN/GaN HEMTs on SiC fabricated in our labs and published data on Si and sapphire substrates [10, 112].

8.5 Pulse measurements

Often discussed phenomenon in the context of AlGaN/GaN HEMTs is called current collapse or dc/rf dispersion: When applying higher frequencies (>100MHz) or stress[1] on HEMTs, the saturation drain current rapidly decreases. Recovery times for GaN–based devices were observed to be in the range of *ms* to *minutes*. By applying UV light the device can be fully recovered immediately [75]. Due to the slow parasitic transient, the current collapse can deteriorate significantly the rf behaviours and output power of HEMTs. Therefore, determination of the recovery time and the current collapse magnitude is very important for AlGaN/GaN heterostructures and was performed also in our labs.

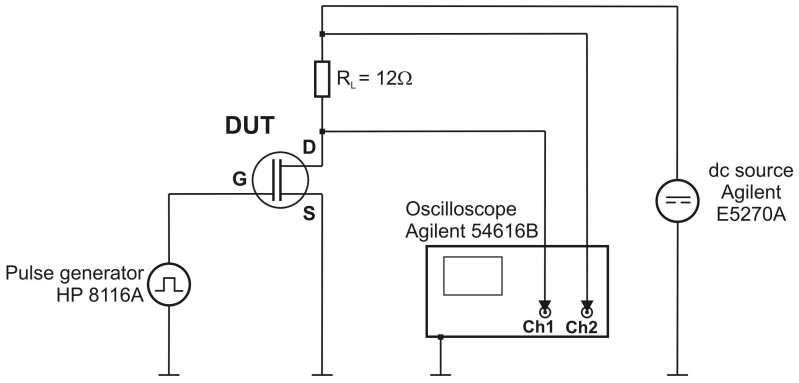


Figure 8.14: Scheme of pulse measurement system.

The current collapse was determined by gate lag measurements as the decrease of the pulsed drain current I_d^{pulse} in comparison to dc drain current I_d. The pulsed gate–source bias was generated by a HP 8116A pulse generator using frequencies of 0.2, 2.0, and 20 kHz. The utilised duty-cycle of 10 % resulted in pulse widths of t_p= 500, 50, and 5 μs and eliminated the self–heating effects at higher drain–source voltages. The drain–source bias was applied by Agilent E5270A Semiconductor Analyzer. A 12 Ω resistor was inserted in the drain circuit that was used for determination of the drain current by a two–channel digital oscilloscope Agilent 54616B. All devices were controlled by a computer. The principle scheme of our measurement system is shown in figure 8.14.

The measured dc and pulsed characteristics of a HEMT fabricated on an undoped sample without GaN cap is shown in figure 8.15 a. For better transparency, the pulsed output characteristics at $V_{gs} = +1V$ are only shown. One can see, that with increasing frequency (decreasing pulse width) a higher drain current collapse is observed. This causes a discrepancies between calculated dc output power $P_{out\,sat}^{dc}$ and measured rf power which decreases due to the decrease of the saturation drain current.

But our measurements indicate that the current collapse can be effectively diminished

[1] device is biased for e.g. 24 hours by $V_{gs} = V_{th}$ and $V_{ds} = 20V$

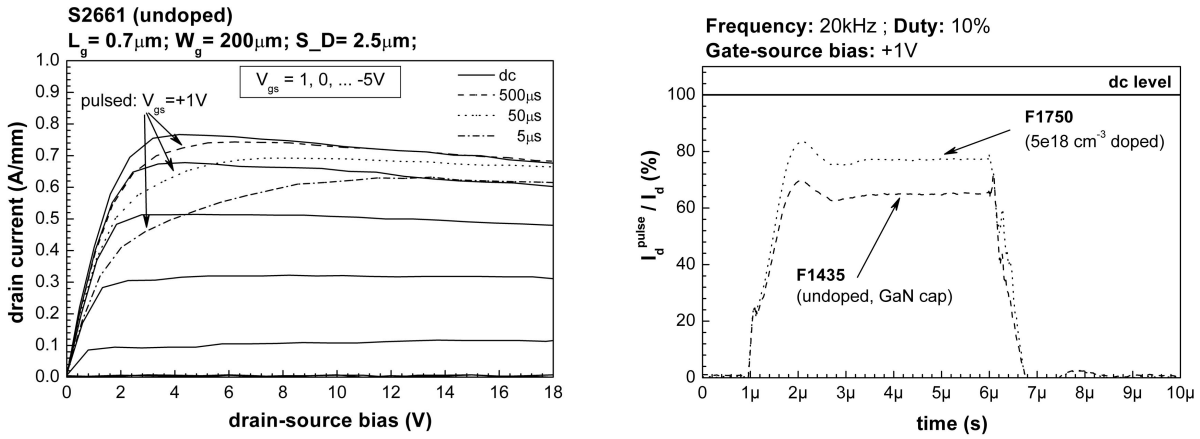


Figure 8.15: Output dc and pulsed characteristics of an undoped S2661 sample (a) and comparison of the normalised drain dc current with measured current pulses of undoped and doped samples (b).

by doping of the barrier layer. Figure 8.15 b shows, that the undoped sample exhibits a current collapse of 65 % at 5 μs pulse width contrary to 77 % current collapse measured on the $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped sample at the same pulse width. Despite of this success the current collapse in GHz range is still an obstacle which does not alow AlGaN/GaN HEMTs to be fully integrated in praxis. Furthermore, the doping of the barrier layer causes higher gate leakage currents, as was already discussed before (table 8.1). Many approaches were published in literature to explain the current collapse, as the virtual gate or various trapping effects [113–116]. They were mostly connected with the growth of the layer structure but until now a satisfying explanation for this phenomena was not found. Our further work was also focused on this problem and we have succeeded to eliminate the drain current collapse using modifications in our technology process. These results are introduced in chapter 11.

8.6 Output power

The final part of unpassivated AlGaN/GaN HEMTs characterisation consists of output power measurements. Here, the dependence of the output power P_{out} on the input power P_{in} is measured and subsequently the gain and the power added efficiency was evaluated. The devices were measured using a load–pull on–wafer measurement system developed by Focus Microwave (figure 8.16). Before the device is measured, it is important to calibrate the system and determine losses of each circuit part connected to the network what is likely to affect the accuracy of the whole system. After the device is connected and biased, the network was fit to 50 Ω resistance by means of computer controlled tuners. Then the

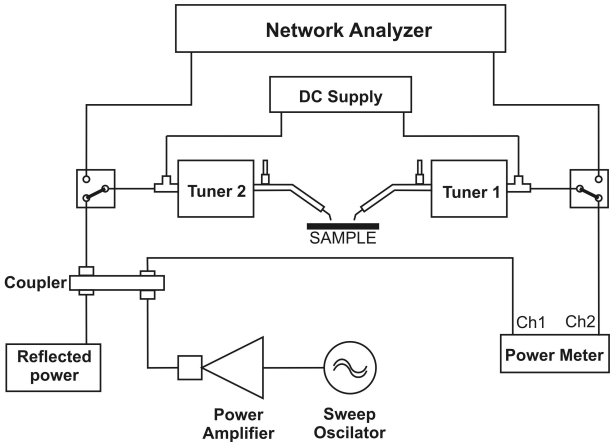


Figure 8.16: Principle scheme of the on–wafer load–pull measurement system used for output power determination.

device was measured in a defined input power frequency range.

The gate–source bias V_{gs} was chosen in correspondence to the peak extrinsic transconductance. The drain–source bias was varied up to a half of the breakdown voltage ($V_{ds}^{max} = V_{br}/2$). Measured output power, gain, and power added efficiency at 7GHz for $5 \times 10^{18}\text{cm}^{-3}$ doped sample with $L_g = 0.7\mu m$ is shown in figure 8.17. As expected, an increased drain–source bias lead to higher output power. Figure 8.18 a illustrates the dependence of the measured output power and power added efficiency (P.A.E.) on the doping of the barrier layer. As is shown, the output power increases with increased doping concentration. This corresponds to our pulse measurement results, where the structures with higher doping level exhibit smaller dc/rf dispersion (current collapse) and therefore higher output power was to be expected.

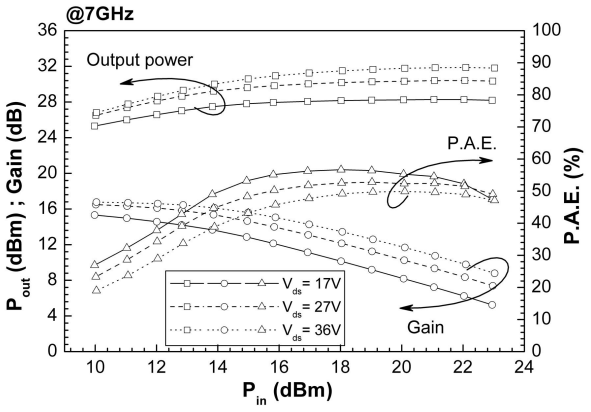


Figure 8.17: Output power measured on the $5 \times 10^{18}\text{cm}^{-3}$ doped sample with $L_g = 0.7\mu m$, $W_g = 200\mu m$, and $S\_D = 3\mu m$.

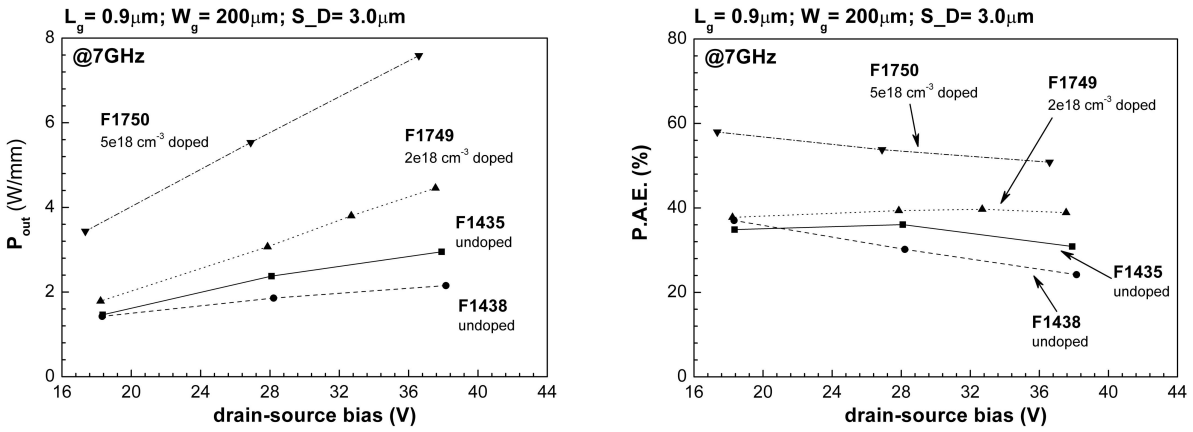


Figure 8.18: Dependence of the output power (a) and power added efficiency (b) on applied drain-source bias for undoped and doped samples.

The measured values of 2.95 W/mm (2.15 W/mm), 4.45 W/mm, and 7.58 W/mm for undoped (F1435, F1438), $2 \times 10^{18}\mathrm{cm}^{-3}$ doped (F1749), and $5 \times 10^{18}\mathrm{cm}^{-3}$ doped (F1750) samples, respectively, at 7 GHz are fully comparable with those published in literature [46, 47, 49, 51–55]. Output power exhibits also strong dependence on geometric dimensions of HEMTs. The best values of output power were measured on devices with a wide gate length ($0.9\,\mu m$) as well as small source–drain distances (in our case $3.0\,\mu m$, shown in figure 8.18). With decreasing gate length the output power decreased.

In spite of that, a saturation of output power was not observed in measured drain–source bias range what indicates higher possible power densities at higher drain–source biases. In our case the maximum V_{ds} is limited by the breakdown voltage of HEMTs. Although significantly lower measured output power in comparison to calculated values shows introduction of the current collapse (table 8.3). Therefore, the next technological steps will be focused on an increase of the breakdown voltage and thus on an increase of the output power and elimination of the current collapse.

Sample	I_d^{sat} **(A/mm)**	V_{knee} **(V)**	V_{br} **(V)**	$P_{out\,sat}^{dc}$ **calc. (W/mm)**	P_{out} **meas. (W/mm)**
F1435	0.76	4.0	69.5	10.10	2.95
F1438	0.81	4.0	71.5	11.09	2.15
F1749	1.06	5.0	–	–	4.45
F1750	1.22	5.0	49.4	10.99	7.58

Table 8.3: Comparison of calculated and measured output power.

Chapter 9

Influence of Surface Passivation on Device Performance

Natural donor–like surface states are supposed sources of electrons collected in 2DEG and need to be stabilised for proper function of devices. Surface passivation was found to be an effective method to make devices stable and to improve device properties. Nevertheless, not every passivation layer is suitable for GaN–based systems and leads to improved behaviour. Different passivation layers such as Al_2O_3, SiO_2, SiO, Sc_2O_3, Si_3N_4 and MgO have been already tested [61,65–68,77,78,103]. Published data differ not only in use of different passivation layer but are also controversial with regards to published improvement or degradation of HEMT behaviours. The influence of SiO_2 and Si_3N_4 passivation layers on AlGaN/GaN/Si heterostructure was tested [118–120, 126] and Si_3N_4 passivation found as favourable in comparison with SiO_2. Due to this reason, this chapter only introduces results obtained using Si_3N_4 passivated devices with SiC substrate fabricated in our labs.

9.1 Static and small-signal properties

Using device surface passivation improved stability, reliability, and device properties are expected. We investigated the influence of deposition temperature, thickness, and type of passivation layer (Si_3N_4 or SiO_2) on device properties in cooperation with the Slovak Academy of Science in Bratislava and the International Laser Centre in Bratislava. Experiments lead to a 150 nm thick Si_3N_4 passivation layer deposited by 300 °C with high quality deposition and best improvement of the device performance (published by D. Gregušova *et al.* [127]). At the beginning, I would like to stress that measurements before and after passivation were always done on exactly the same devices firstly measured as unpassivated, afterwards passivated, and again measured as passivated HEMTs. This method eliminates errors due to possible inhomogeneity of the layer structure.

Sample	**Doping** ($\mathbf{cm^{-3}}$)	**Passivation**	n_s ($\mathbf{cm^{-2}}$)	μ_n (cm^2/Vs)	R_s (Ω/sq)
S2661	n.i.d.	no	7.94×10^{12}	1695	464
		yes	10.1×10^{12}	1450	427
F1435	n.i.d.	no	7.77×10^{12}	1900	423
		yes	9.36×10^{12}	1725	387
F1438	n.i.d.	no	6.95×10^{12}	1930	466
		yes	8.21×10^{12}	1773	430
F1749	2×10^{18}	no	8.19×10^{12}	1780	428
		yes	9.77×10^{12}	1730	370
F1750	5×10^{18}	no	9.72×10^{12}	1663	387
		yes	11.6×10^{12}	1440	374

Table 9.1: Sheet carrier density, electron mobility, and sheet resistivity of AlGaN/GaN heterostructures on SiC substrates before and after passivation.

The first investigation we performed aimed at the influence of the passivation on 2DEG properties evaluated by Hall effect measurements on $0.3 \times 0.3\,\mu m^2$ Van der Pauw patterns fabricated simultaneously with the devices (see figure 6.9). The measured results collected in table 9.1 show an increase of the sheet carrier concentration in 2DEG after passivation and a slight decrease of the carrier mobility for all tested samples. Observable is also the influence of the doping concentration where the doped samples exhibit smaller passivation induced charge in comparison to undoped ones. These result are consistent with those measured on layer structures with Si substrate investigated in our labs (figure 9.1). Improvement of 2DEG properties after surface passivation supports the theory, that surface states can be the source of electrons collected in 2DEG where the passivation of surface traps change the surface state concentration resulting in a change of the 2DEG properties.

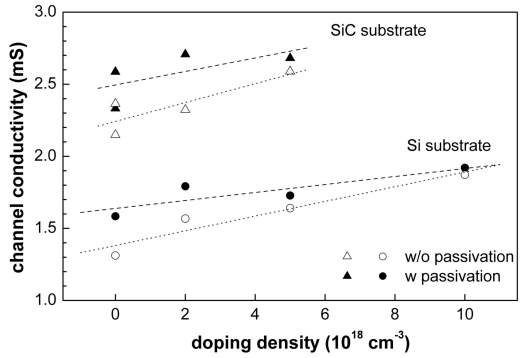


Figure 9.1: Influence of the SiN passivation on the channel conductivity of undoped and doped layer structures grown on Si and SiC substrates investigated on Van der Pauw patterns.

The smaller influence of the surface passivation on 2DEG using doped layer structure can be explained with the shielding of surface changes by an intentionally doped layer placed between the surface and the 2DEG. Increased doping density of the barrier layer makes the shielding effect more remarkable and therefore the change in 2DEG due to passivation is smaller (see figure 9.1). The improved properties of 2DEG after Si_3N_4 passivation resulted in improved dc HEMT properties shown in figures 9.2 and 9.3. The improvement was more pronounced for undoped samples as for doped ones, which is in a good agreement with Hall effect data (see table 9.2). The shift of the threshold voltage to more negative values observable on both undoped and doped structures after passivation points to an increased sheet carrier concentration in channel under the gate electrode.

The gate leakage currents and breakdown voltages investigated on passivated samples differed just slightly from those measured on unpassivated samples (see figure 9.4). Typically, higher gate leakage currents were measured for doped samples in comparison to undoped ones.

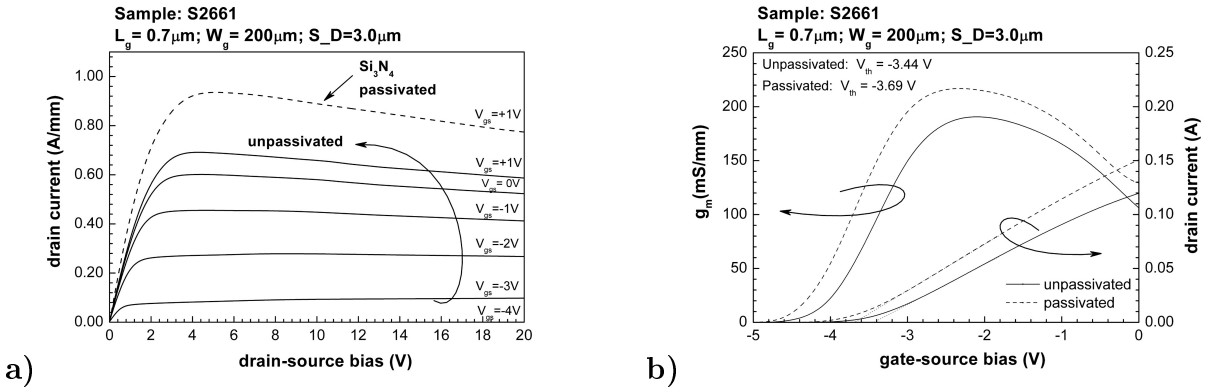


Figure 9.2: Comparison of output (a) and transfer (b) characteristics of undoped sample (S2661) before and after passivation.

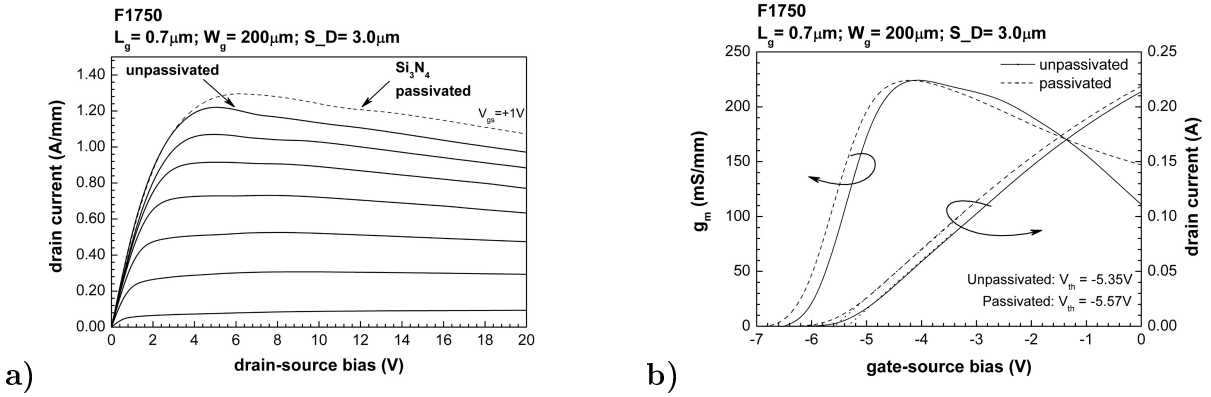


Figure 9.3: Comparison of output (a) and transfer (b) characteristics of $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped sample (F1750) before and after passivation.

Sample	**Doping** ($\mathbf{cm^{-3}}$)	**Passivation**	I_d^{sat} (A/mm)	g_m (mS/mm)	V_{th} (V)
S2661	n.i.d.	no	0.69	193	-3.47
		yes	0.93	219	-3.69
F1750	5×10^{18}	no	1.22	227	-5.35
		yes	1.30	226	-5.57

Table 9.2: Comparison of undoped and doped HEMT parameters before and after passivation ($L_g = 0.7\mu m$, $W_g = 200\mu m$, $S_D = 3.0\mu m$).

The rf measurements show just slight increase of the cut-off frequency f_T after passivation from 33.5 GHz to 35.0 GHz for $L_g = 0.5\mu m$ on undoped sample (S2661) and from 32.0 GHz to 35.3 GHz for 5×10^{18} doped sample (F1750) with the same L_g. The maximum frequency of oscillation f_{max} was unchanged for both, undoped and doped samples.

These results indicate markedly improved dc and slightly improved rf behaviours after Si_3N_4 passivation, which should lead to higher output power according to the already discussed equations 4.29 and 4.30. To confirm this hypothesis, gate lag and output power measurements are performed and evaluated in next sections.

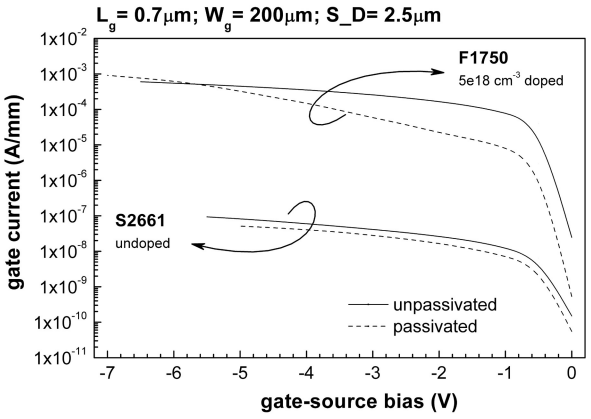


Figure 9.4: Comparison of the gate current before and after passivation for undoped and doped sample measured by $V_{ds} = 0V$.

9.2 Pulse measurements

The gate lag measurements (or pulse measurements) were done in the same way as described in chapter 8. The current collapse is evaluated as the decrease of pulsed drain current relative to its dc value. A frequency of 20 kHz with the pulse width of $5\mu s$ was applied and the pulsed drain current I_d^{pulse} was extracted $4\,\mu s$ after the lead edge of the

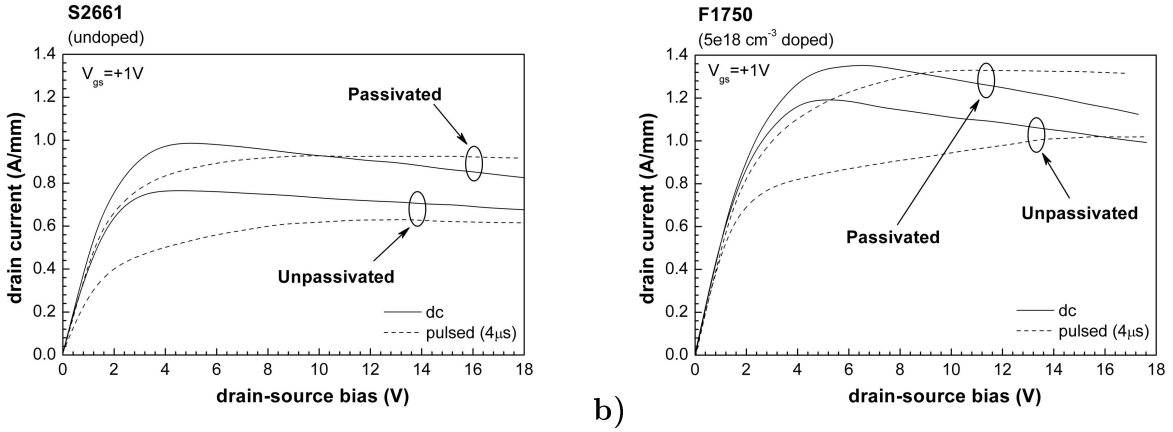


Figure 9.5: Static and pulsed output characteristics of undoped (a) and doped (b) sample by $V_{gs} = +1V$.

pulse. The dc and pulse output characteristics shown in figure 9.5 measured before and after passivation exhibit a decrease of the current collapse from 25 % to 14 % in undoped, and from 23 % to 11 % in the doped sample after the passivation (figure 9.6). Improvement of the dc behaviour and diminishing of the current collapse after surface passivation was observed on all AlGaN/GaN HEMTs fabricated in our labs independent of the doping level of the barrier layer or the introduction of the GaN cap. This remarkable improvement of AlGaN/GaN HEMT behaviour implies again the connection between surface states and current collapse and highlights that the under–gate and beside–gate regions of HEMTs play a significant role in the dispersion process. The responsibility of surface states for dispersion effects was published also by other groups [55, 117].

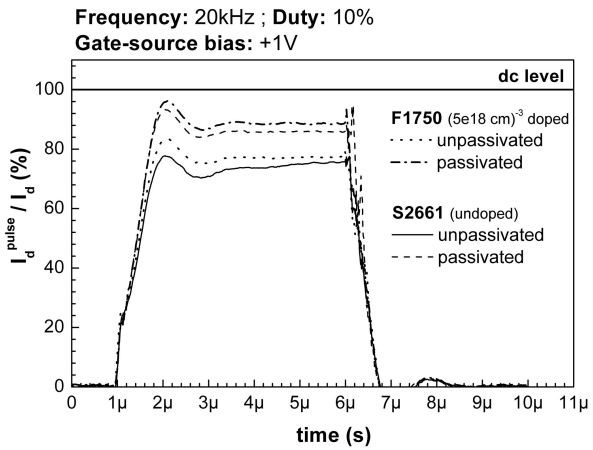


Figure 9.6: Comparison of normalised pulse to dc drain current measured on undoped and doped structures before and after passivation.

9.3 Output power

Output power measurement is the last characterisation method used for determination of the passivation influence on the AlGaN/GaN HEMT behaviour. Improved dc and pulsed properties using surface passivation lead to higher theoretically calculated dc power values $P^{dc}_{out\,sat}$. Due to this, we expected to measure higher real output power values of fabricated devices. Our expectations were confirmed by measurement shown in figure 9.7 a. The output power measured at $V_{ds} \cong 27V$ increased from 3.81 W/mm to 7.16 W/mm (88 % improvement) for undoped structure and from 4.70 W/mm to 6.94 W/mm (48 % improvement) for the $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped structure. This corresponds very well with improvement of dc behaviour of undoped sample after passivation in comparison to doped one (see table 9.2) and our investigations of AlGaN/GaN HEMTs on Si substrate done by P. Javorka *et al.* [10] which observed the same tendency. Measured output power value of 9.04 W/mm on passivated AlGaN/GaN/SiC HEMTs at 7 GHz is fully comparable with the best published results in the last few years (figure 9.7 b).

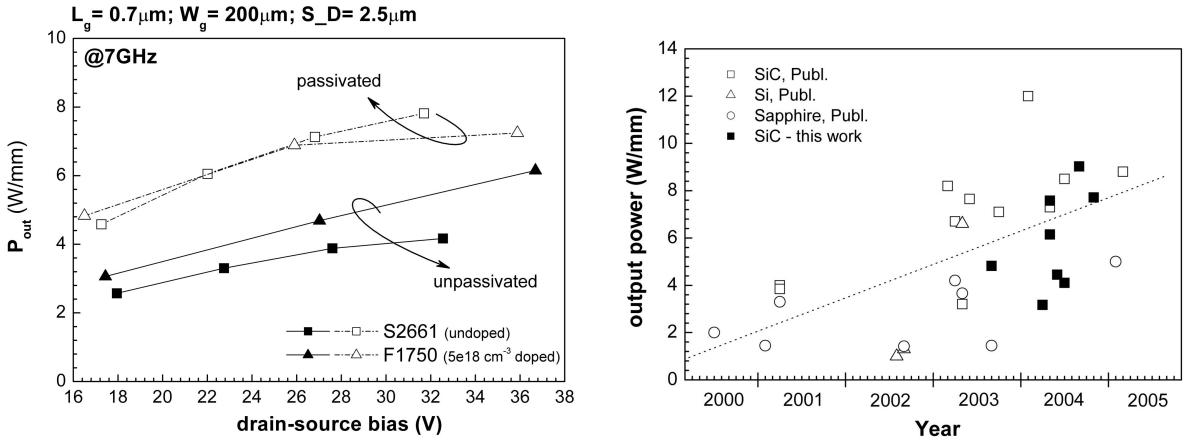


Figure 9.7: Output power measured on unpassivated and passivated samples ($L_g = 0.7\mu m$, $W_g = 200\mu m$, $S_D = 2.5\mu m$ (a) and output power trade line over years (b) [43–64] .

Improvement of AlGaN/GaN HEMT properties after surface passivation was published also by other groups [67, 68]. The increase of the drain current and the decrease of the current collapse using suitable surface passivation is not the only possibility for output power improvement. The next opportunity lies in the increase of the breakdown voltage which allows us to move the working point of the device to higher drain–source biases. Another big challenge is the elimination of the current collapse in AlGaN/GaN HEMTs and the explanation of the physical fundament. Both problems were intensively studied in our institute and our answers to these questions are introduced in the next chapters.

9.4 Modelling of surface passivation effects

To understand influence of the surface passivation on AlGaN/GaN heterostructure and high electron mobility transistor behaviour a model with possible physical explanation is described. This model is just phenomenological and is based on results of our institute research.

After appropriate passivation we observed two main influences on the HEMT structures: increase of the sheet carrier concentration in 2DEG, and decrease of the dc/rf dispersion. Figure 9.8 shows possible situation in unpassivated GaN cap/AlGaN/GaN heterostructure. In thermodynamical equilibrium the sheet carrier concentration of 2DEG n_s is proportional to concentration of surface states n_{ss}. The difference between n_s and n_{ss} are electrons in 2DEG originating from other sources as the Si doped AlGaN layer or background GaN buffer.

After applying drain–source bias some electrons from the gate are trapped at the surface states of unpassivated GaN and form virtual gate causing current collapse. Simultaneously, electrons from valence band at AlGaN/GaN cap interface are trapped through very thin GaN cap layer and fill empty surface states. Subsequently, the holes generated in valence band are neutralised by electrons in surface state.

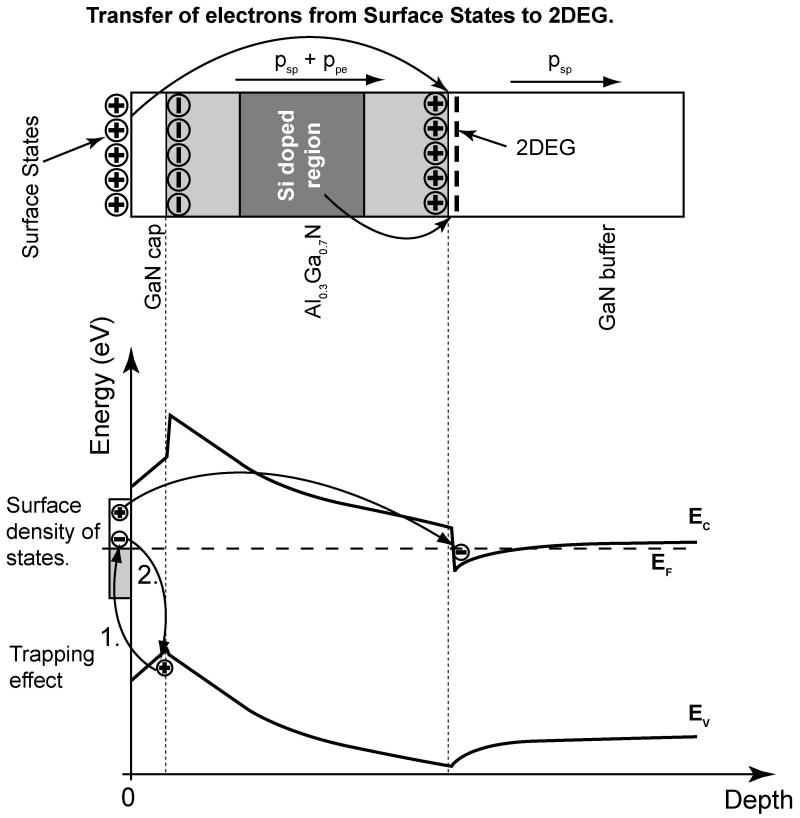


Figure 9.8: Model of possible trapping effect in HEMT.

Appropriate surface passivation builds additional positive charge formed at the GaN cap/Passivation layer interface which force additional electrons transfer from surface states to 2DEG and increases the sheet carrier concentration in channel after passivation. Furthermore, passivation of surface states prevent trapping of electrons from valence band through GaN cap to surface states and with it reduces the current collapse in HEMTs.

This explains an increase of the sheet carrier concentration in 2DEG and reduction of the dc/rf dispersion after adding passivation layer on top of AlGaN/GaN heterostructure.

Chapter 10

Field Plate Technology

The previous chapter presented improvements of dc and power properties using suitable surface passivation. Nevertheless, this is not the only possibility and further improvement regarding output power is feasible by extending the breakdown voltage. There are two possibilities of how to do it: Increase of the source–drain distance S_D or application of the field plate technology. Wider source–drain distances lead to a degradation of dc and transport properties and therefore are not frequently used. On the other side, field plate technology introduces an advantage of keeping small S_D and profiting from a change of the electric field distribution in the gate–drain region. Improvement of breakdown voltage using a field plated gate is known since 1969 [128] and is successfully exploited in Si– and GaAs–based materials. In AlGaN/GaN processing technology it was presented in the year 2003 for the first time and since that time it is used as a standard tool for breakdown voltage improvement.

10.1 Electric field simulations

Field plate technology means fabrication of a second wider gate electrode above the first one separated by a passivation layer (see chapter 6). The top gate electrode is extended to the drain contact and is electrically connected with the first gate on the pad. It is favourable to fabricate the first gate asymmetrically shifted in direction of the source contact what improves breakdown voltage and provides space for the top gate electrode (see figure 6.7). It is important to understand the electrical and physical influences of the field plate technology. Before the fabrication process was started, simulation of the influences of the second gate electrode were modelled. For this purpose, the commercially well known ATLAS simulation package from Silvaco International was used.

ATLAS simulation package allows to build up any layer structure using pre–defined material systems. Parameters of materials can be arbitrarily changed and subsequently

Parameter	**ATLAS parameter**	**Unit**	**GaN**	**AlGaN**
affinity	affinity	(eV)	–	3.82
E_g	eg300	(eV)	3.40	3.96
alignment	align		0.80	0.80
ε_r	permittivity		9.5	9.5
μ_n	mun	$(\mathrm{cm}^2/\mathrm{Vs})$	900	600
μ_p	mup	$(\mathrm{cm}^2/\mathrm{Vs})$	10	10
ν_{sat}	vsat	$(\mathrm{cm/s})$	2.0	–
N_C	nc300	(cm^{-3})	1.07	2.07
N_V	nv300	(cm^{-3})	1.16	1.16

Table 10.1: Material parameters used in ATLAS simulation [88].

simulated. In our case the two–dimensional AlGaN/GaN layer structure of the S2661 sample was modelled using material constants published in literature and summarised in table 10.1 [88]. The 2DEG was modelled as a sheet charge density collected near the AlGaN/GaN interface, similarly to WinGreen band structure modelling.

Three types of simulation were performed to see differences in electric field distribution under the gate electrode: simulation of standard HEMT, simulation of HEMT passivated with a 50 nm thick Si_3N_4 layer, and simulation of HEMT with applied field plate technology (figure 10.1). Using these structures, the electric field in between the source and drain electrodes at off–state conditions of HEMT ($V_{gs} = -2.8V$, $V_{ds} = 50V$) was calculated. As figure 10.2 shows, the most critical place with a peak electric field is on the drain side underneath the gate electrode highlighted with arrows. This peak is caused by very high potential difference between the gate and drain contact. Only a small 9 % decrease of the peak was calculated using passivation layer due to additional positive charge in passivation layer. A considerable peak decrease of 31 % and optimised electric field distribution was calculated using the second gate electrode (G_2) electrically connected with the first one (G_1). This allows us to apply higher drain–source biases and hereby to increase the output power without degradation of rf properties due to identical dimension of the active gate length.

10.2 Real structure measurements

Simulated data were used for fabrication of HEMTs with the field plate technology using S2661 (undoped) and F1750 ($5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped) layer structures. Devices Q, R, S, T, U, and V were designed for this purpose on the "Power 2" mask set. Fabrication process is described in chapter 6 and appendix A.

Using the field plate technology improvements of dc, rf, and pulsed properties identical

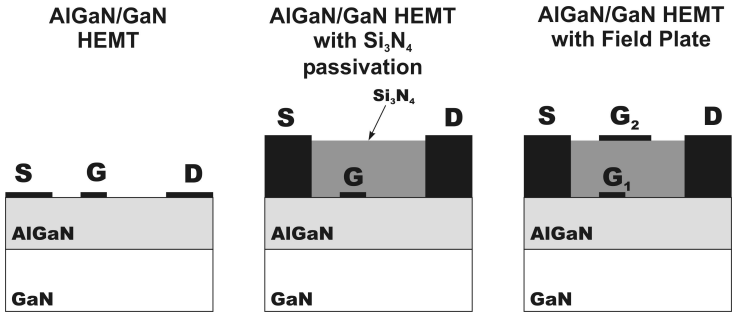


Figure 10.1: Overview of structures simulated by ATLAS.

to improvements after surface passivation introduced in chapter 9 have been determined. This is consistent with our expectations regarding the application of the same isolation layer (Si_3N_4) and having the same passivating influences on the surface. In the case of field plate technology, improvements of the breakdown voltage can not be determined using the Current–induction technique. This technique takes into account off–state changes of the drain–source leakage current while the on–state electric field distribution in undersurface region, which does not influence the off–state drain–source leakage, is not covered. Therefore, improvement of breakdown voltage was tested directly by output power measurement using higher drain–source biases.

The comparison of measured output power on undoped and doped sample is shown in figure 10.3 a. Positive influence of the field plate technology is proven by higher measured output power of 11.9 W/mm for undoped and 12.0 W/mm for the doped sample in comparison to 7.2 - 9.0 W/mm on passivated samples. The measured output power of HEMTs with the field plate technology was considerably higher also at devices with small gate lengths of 0.5 μm contrary to unpassivated HEMTs where the maximum output power exhibited devices with longer gate length.

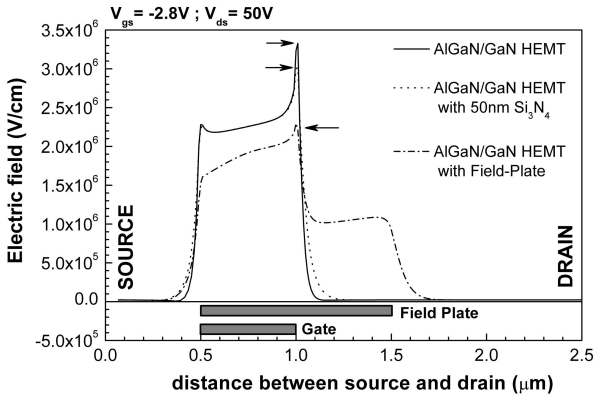


Figure 10.2: ATLAS simulation of electric field in AlGaN/GaN HEMT device under the gate electrode for different technological processes.

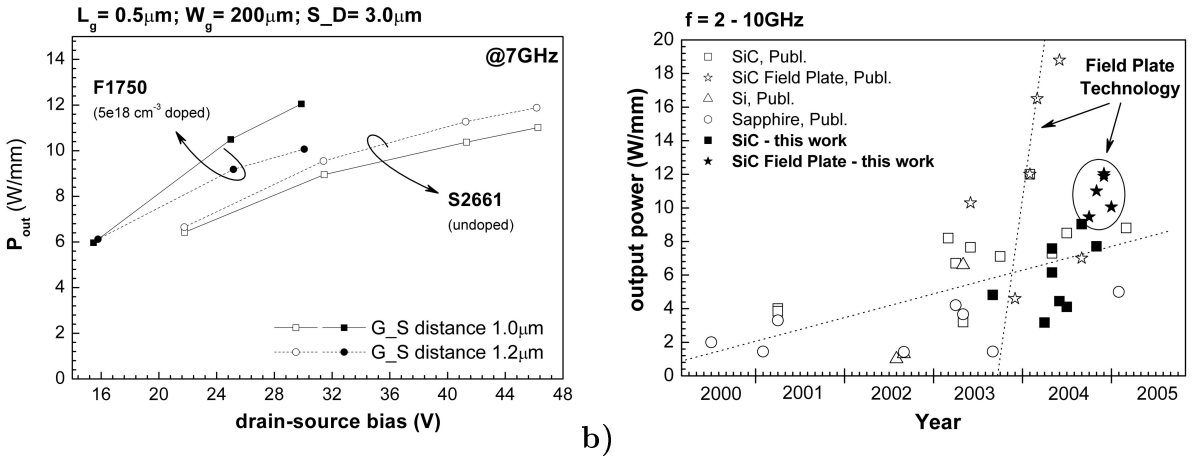


Figure 10.3: Output power measured on HEMTs with applied field plate technology (a) and comparison with results published in literature (b) [81–87].

Important is also the fact, that the doped sample reached an output power of 12 W/mm at the drain–source bias of 30 V contrary to 46 V for the undoped sample. Nevertheless, the doped sample suffers from markedly smaller breakdown voltage and can not reach drain–source bias higher than 37 V without breaking. The HEMTs manufactured on the undoped sample are able to work above $V_{ds} = 46\,V$ without breakdown, what was the top bias boundary of our measurement setup, and could possibly work at even higher drain–source biases that might result in higher measured output power values.

Finally, worldwide published results are compared to the output power measured on undoped and doped devices presented in this work. An overview is given in figure 10.3 b. Results are categorised according to the used substrate and field plate technology. It shows an extreme rise up after field plate technology introduction. This is in a agreement with our own output power data which can compete to the best published values.

Chapter 11

Influence of Technology Process on Current Collapse

The previous chapters demonstrated that HEMT properties can be improved considerably using surface passivation and field plate technology resulting in very high output performance power of 12 W/mm. Regardless these excellent results, all presented samples suffer from relatively high current collapse (or dc/rf dispersion) at high frequencies. The current collapse elimination leads to improved rf behaviour and reliability of HEMTs [72, 117]. Therefore, additional investigation regarding dc/rf dispersion elimination were performed and results are discussed in this chapter.

11.1 Elimination of current collapse

The effect of current collapse has been already introduced in chapters 8 and 9 and is the most discussed phenomena regarding GaN–based heterostructures. A many various observed trapping effects, especially trapping at the surface, in the access region between gate and drain, are considered to be primarily responsible for current collapse and high frequency dispersion [113, 114]. Another explanation of current collapse is based on charge trapping in the high-field region underneath the gate [115]. All these phenomena were investigated in our labs resulting in successful elimination of current collapse up to giga–hertz frequency range using the technological process described in this section.

HEMTs presented in the previous chapters exhibit high sensitivity on surface changes in between the drain and source region. However, only the free–standing surfaces beside the gate electrode was influenced using surface passivation until now. Passivated samples showed diminished dc/rf dispersion at $4\mu s$ pulses but the current collapse could not be completely eliminated (refer to chapter 9). Considering these findings, the additional possible source of instabilities in fabricated devices may be located underneath the gate

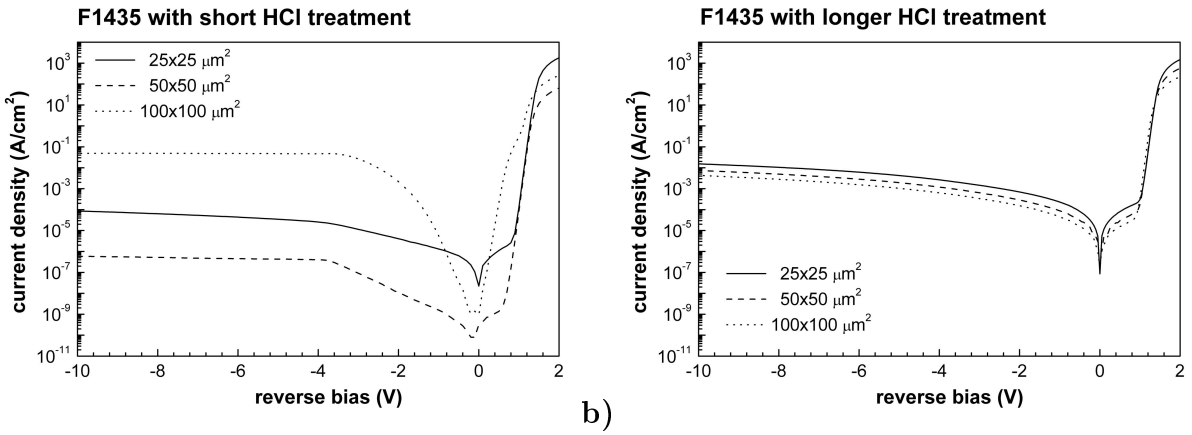


Figure 11.1: Comparison of current densities over applied bias on Schottky diodes fabricated using standard (a) and advanced (b) technology process .

region (metal–semiconductor interface) formed during the gate metal deposition process. Therefore, next investigation was focused on the gate (Schottky) metallisation process and treatment procedure prior to metallisation.

The standard technology process concerning gate electrode fabrication consists of 5 sec. pre–treatment using $HCl(1) : H_2O(2)$ solution (HCl dip) and standard Ni(25nm) / Au(100nm) metallisation. Pre–treatment removes native oxide from AlGaN(GaN) surface which is built up during the technological processes. The standard length of HCl dip was settled to be 5 sec. However, our further investigation using Schottky diodes, processed simultaneously with HEMTs, indicates that a very thin oxide layer is still present in between metal and semiconductor. IV measurements show that the current does not scale with the device area for samples with 5 sec. long HCl treatment. This is demonstrated in figure 11.1 a, in which the current density as a function of reverse bias is shown for three diodes with different contact area. The saturated reverse current density differs more than three orders of magnitude. This points to highly inhomogeneous current flow through the diode which might be due to a higher probability of leaks in the interfacial layer. Currents relatively well proportional to the diode area (figure 11.1 b) were achieved using longer, 15 sec., HCl treatment prior to gate metallisation indicating qualitatively better Schottky interfaces without leaks. A higher reverse current densities of diodes prepared using longer HCl treated can be due to the surface conduction mechanisms and/or the electron traps in GaN cap layer.

Additionally, the gate metallisation process was investigated and was found to influence significantly current collapse elimination. For metal deposition a conventional electron beam evaporation system was used. Electron beam evaporation is a well established technique extensively used both in industries and in research laboratories for the deposition of optical materials, metals and semiconductors. The use of multi–crucible

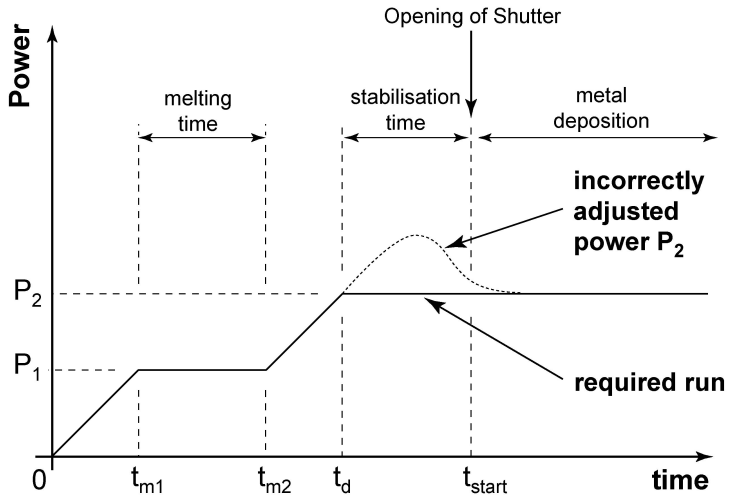


Figure 11.2: Overview of non–collapsed Schottky contact deposition over time.

electron beam sources allows the deposition of multilayers of up to four materials. A quartz crystal thickness controller is used for programming multilayers as well as for the automatic control of the thickness and of the deposition rate in each layer.

The most crucial process–phase is the first contact of evaporated metal atoms with the semiconductor surface during the evaporation process. It is important to reach smooth evaporation of the first atomic layers with the smallest deposition rate possible. Otherwise, the surface can be hit by high–energy atoms resulting to formation of defect donors [136]. Smooth deposition can be achieved using careful adjustment of the electron beam power prior to deposition (figure 11.2). P_1 is the power setting up the melting point of the metal to be evaporated. Between t_{m1} and t_{m2} the metal is melted in crucible. Melting time has to be long enough to clear away all impurities absorbed by the metal from chamber atmosphere. Afterwards, P_2 has to be adjusted to reach the required deposition rate. This is the most important step, since the run should not exceed the P_2 value. Exceeding P_2 leads to higher deposition rates of the first atomic layers producing donor defects at the Schottky interface. Also, the stabilisation time before shutter opening has to be long enough, usually up to a few minutes, to reach a constant deposition rate even for the first metal atomic layers and not to deposit rests of impurities usually collected on top of the melted metal.

11.2 Static and rf properties of non-collapsed HEMTs

The achieved improvements of technology process were utilised for fabrication of the second set of HEMTs using the wafers F1435, F1438, and F1750 as in chapters 8 and 9. The TLM measurements of the second set with longer HCl dip and adjusted metal de-

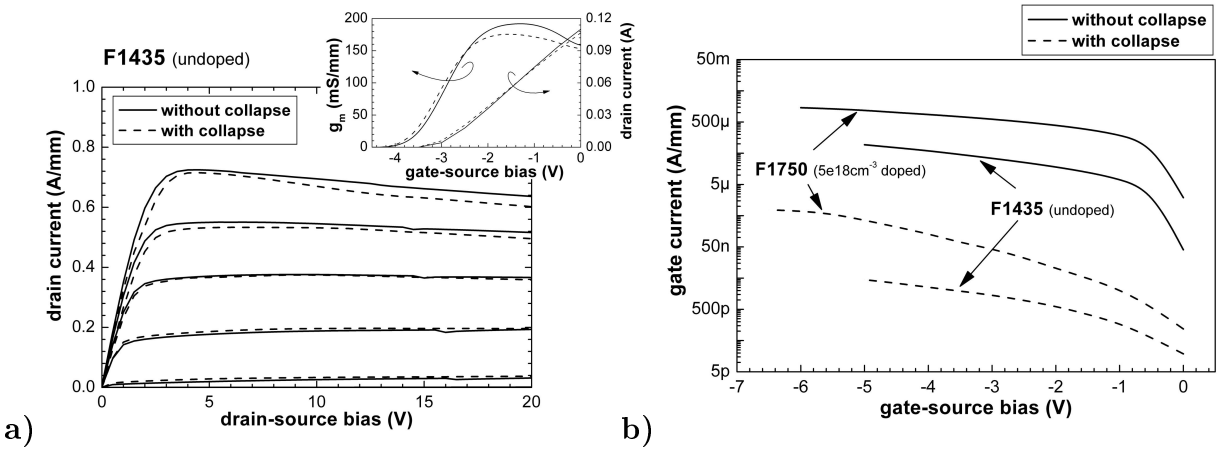


Figure 11.3: Comparison of output and transfer characteristics (a) and gate currents (b) of collapsed and non-collapsed unpassivated samples.

position yielded similar sheet resistance, contact resistance, and specific resistivity values compared to the first set. Considering this, the same ohmic contact behaviour of both sets is considered. I would like to stress, that all presented data in this section were measured on unpassivated samples.

Static measurements on GaN/AlGaN/GaN HEMTs with similar geometry from both sets showed nearly identical output and transfer characteristics. This is demonstrated in figure 11.3 a, in which typical IV and transconductance characteristics of undoped HEMTs with a gate length of $0.7\,\mu m$ are shown. The saturation drain current (at $V_{gs} = 1V$) and the peak extrinsic transconductance were 0.73 A/mm and 185 mS/mm, respectively. Devices on $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped heterostructure exhibited partially higher values, $I_d^{sat} = 1.3\,A/mm$ and $g_m = 255\,mS/mm$, which is in agreement with Hall effect data. The threshold voltage of devices prepared with longer dip was systematically slightly higher than for short-dip devices ($\Delta V_{th} = 0.25\,V$). Figure 11.3 b shows the two-terminal gate-source leakage currents typical for undoped and doped GaN/AlGaN/GaN HEMTs from both sets. Partially higher leakage currents for doped devices compared to undoped ones are observed. However, remarkable higher leakage currents (about four orders of magnitude) were measured on devices with longer surface treatment before the gate metal was deposited. This might indicate again, that an interfacial insulating oxide is still present in samples with short dip.

Small-signal microwave measurements yielded current-gain and power-gain cutoff frequencies (f_T and f_{max}, respectively) typical for AlGaN/GaN HEMTs. For example, $f_T = 20\,GHz$ and $f_{max} = 45\,GHz$ were measured on devices with a $0.7 \times 200\,\mu m^2$ gate. No significant difference was found between devices with different surface treatment.

Presented dc results show, that there is no possibility to determine the presence of current collapse in HEMTs from dc output and transfer characteristics or rf properties.

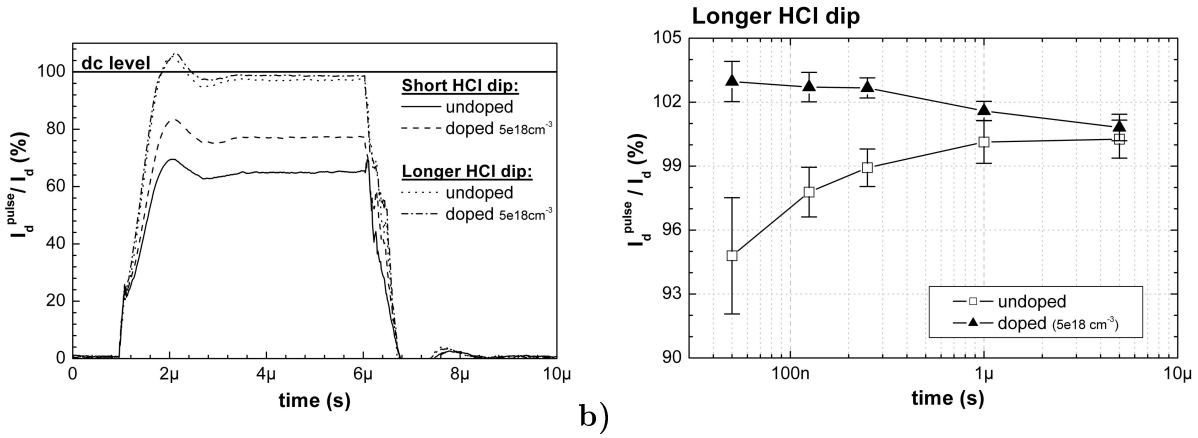


Figure 11.4: Gate lag measurements on unpassivated undoped ($V_{ds} = 6V$) and 5×10^{18} cm^{-3} doped ($V_{ds} = 8V$) sample with short and longer HCl dip applying $5\,\mu s$ gate–pulse width (a) and with longer HCl dip applying pulse width down to $50\,ns$.

The dc parameter which can indicate the presence of current collapse is the gate leakage current. This fact is supported with gate lag measurements presented in next section.

11.3 Pulse measurements

Gate lag measurements in gate turn–on pulsing mode were performed to investigate the current collapse. The gate–source voltage was pulsed from pinch–off to different on–state V_{gs} values and the pulse width was from $5\,\mu s$ down to $50\,ns$ (frequency range $0.2 - 20\,MHz$). Gate lag measurements in the nano–second range were done in co–operation with Prof. G. Meneghesso at the University of Padova in Italy and confirmed our gate lag measurements in micro–second range.

Significantly different behaviour between devices from the two sets was observed. For devices with short HCl treatment, the pulsed drain currents were much lower than corresponding static values. In contradiction to that, the devices with longer HCl treatment show negligible current collapse. This observation was similar for devices on doped and undoped structures. The obtained results are summarised in figure 11.4 a, in which recorded pulses of the drain current are normalised to its static value. The devices were switched from pinch–off state to $V_{gs} = 1V$. Significant collapse (35% for undoped and 23% for doped) was measured on devices with short surface treatment. In contradiction to that, devices with longer HCl treatment show only negligible, if any, current collapse. These longer–treated devices (undoped and doped) were also tested applying pulse widths down to $50\,ns$. The drain current collapse measured at $50\,ns$ turn–on gate voltage pulse, showed in figure 11.4 b, was less than 8% for undoped sample and the doped sample exhibits no collapse of the drain current. The drain current of the doped sample in pulsed mode

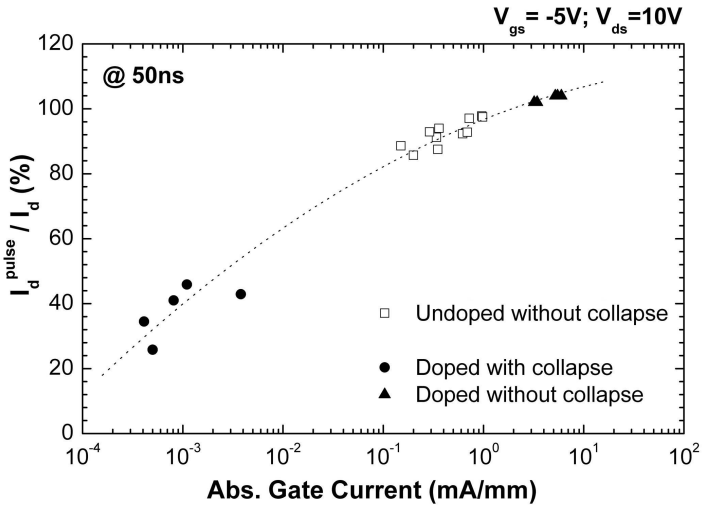


Figure 11.5: Dependence of the current collapse on gate leakage current.

was measured to be higher due to smaller self–heating in comparison to its static value resulting to I_d^{pulse}/I_d ratio over 100%. Error bars represent the results obtained from 10 measured devices with $L_g = 0.3\,\mu m$.

Measured dc/rf dispersion in undoped and doped samples depicted over the gate leakage current shows a clear dependence illustrated in figure 11.5. Here it is confirmed, that current collapse is directly dependent on the gate leakage current where with smaller dc/rf dispersion the gate leakage current is higher. This can be attributed to the presence of electron traps within the GaN cap layer and/or to surface conduction mechanisms. A higher conductivity between gate and drain/source contacts reflects into a large carrier population within the cap layer, hence faster surface charge modulation (i.e. smaller dispersion at a given pulse width) is observed. However, the reduction or elimination of the dc/rf dispersion at certain frequency does not mean reduction (or elimination) of the current collapse in the whole frequency range. It means a shift of a boundary frequency where the current collapse starts to be observable towards higher frequencies. Our aim is to move the boundary frequency of the current collapse above the work frequency range of the HEMT.

11.4 Stress measurements

In order to investigate the reliability of these low–dispersion devices, long–term bias stress measurements were performed. The output characteristics were measured by means of a HP4142B semiconductor parameter analyzer before and after stress. Devices were stressed for 12 hours at fully closed state of HEMTs (the gate–source bias was equal to

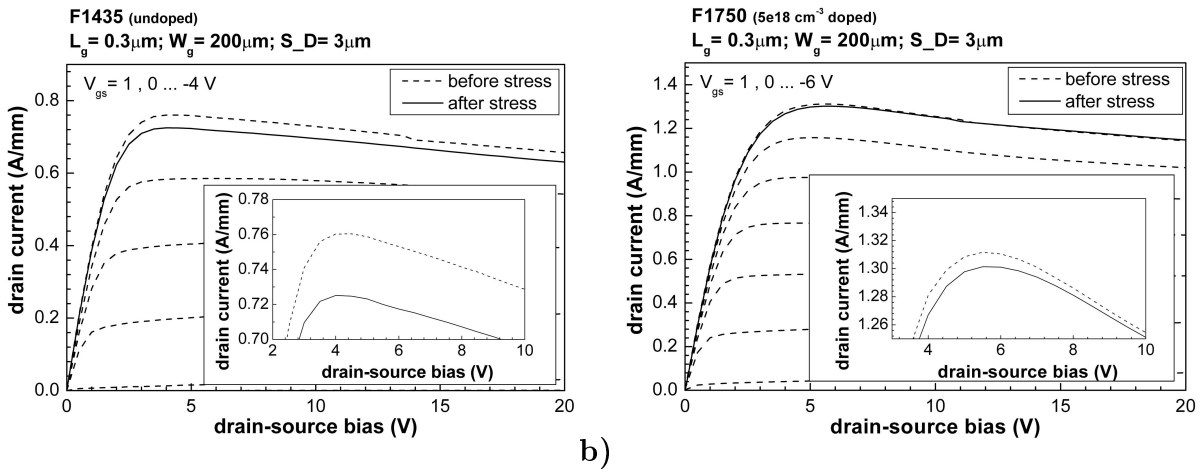


Figure 11.6: Static output characteristics of unpassivated undoped (a) and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped (b) samples before and after 12 h bias stress.

$V_{pinch-off}$), the drain-source bias was chosen to be $V_{ds} = 20V$. The maximum drain current value before/after stress was 0.76/0.73 A/mm and 1.31/1.30 A/mm for undoped and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped samples, respectively. This corresponds to a maximum decrease of 3.9% for undoped sample and of 1.2% for $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped samples (see figure 11.6). This is a significantly lower degradation compared to 37% decrease of maximum drain current published by H. Kim *et al.* on AlGaN/GaN/SiC HEMTs stressed for 12 h at the same bias conditions of $V_{ds} = 20V$ and $V_{gs} = -6V$ [117]. A decrease of the extrinsic transconductance of 4.9% and 2.3% (undoped and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped, respectively) after the stress confirms the results of drain current decrease. The rf and large signal performances of undoped samples were also investigated and show insignificant degradation of less than 5% after the stress.

In order to evaluate the drain current compression (CC), consecutive current sweeps before and after long–term stress were measured. Two dc sweeps, one directly after another, were measured before and after the stress was applied. Figure 11.7 shows the detailed view on sweeps measured at $V_{gs} = +1V$ before an after stress. The current compression was evaluated as the maximum percentage current decrease between two consecutive sweeps ($CC = (I_{d1}^{sat} - I_{d2}^{sat})/I_{d1}^{sat}$). A maximum drain-current decrease of 0.1-1.2% before and after stress, independently on the doping level, was measured. This is a one order of magnitude lower decrease in comparison to published data for MBE grown AlGaN/GaN/SiC HEMTs with a decrease of 1-41% after 16 h stress measured at $V_{ds} = 30V$ and $I_d = 200\,mA/mm$ [72].

The negligible degradation of static output and transfer characteristics after 12 hours of bias stress supports the thesis of performance improvements of devices with longer HCl treatment and using adjusted gate metal deposition. These results also demonstrate

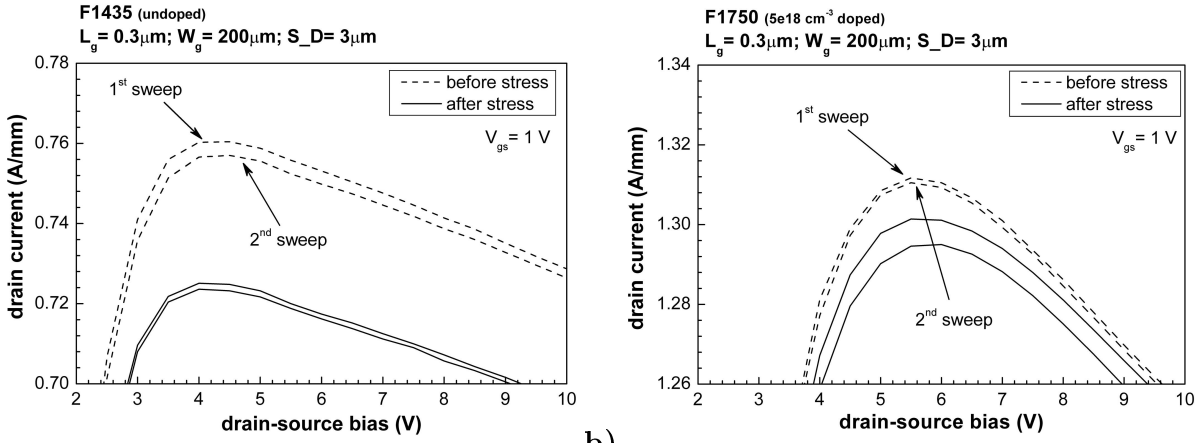


Figure 11.7: Drain current compression of unpassivated undoped (a) and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped (b) samples before and after 12 h bias stress.

that surface treatment under the Schottky contact is a crucial processing step in the preparation of reliable GaN-based HEMTs.

Properties of AlGaN(GaN) Schottky interfaces, applying different surface treatment before gate deposition have been reported also by other groups [129–133]. Various effects like an increase of surface Ga(Al)/N ratio, i.e. creation of N vacancies [129–131] or interface oxides [132, 133] and models like defect-assisted tunnelling [134], hopping conduction through threading dislocation [135] and field emission through thin surface barrier [131] are discussed as a possible current collapse reason. We believe that the existence of a thin interfacial oxide layer lowers the gate leakage but the trapping effects at the interface and/or within the GaN cap layer are responsible for larger current collapse. However, trapping effects and conduction mechanisms at the surface apart from the gate can play an additional role.

Chapter 12

Gate Leakage Current Reduction

The previous chapters showed considerable improvement of the static and output power properties using surface passivation, an increase of the breakdown voltage using field plate technology, and remarkable elimination of the current collapse by improvement of our technology process. Results showed, that with elimination of the current collapse the gate leakage current increases, which is contrary to our requirements of the smallest gate leakage possible (see chapter 11). A possible solution for the gate leakage current reduction is the fabrication of MISHFET devices using a thin insulation layer applied under the gate electrode. This layer acts as an additional barrier which decreases the leakage current and has also the function to passivate the surface. The thickness of this layer used to be less then $15\,nm$ not to loose the gate control function.

Within the bounds of this work a technology process was developed to fabricate MOSHFETs, which was presented in chapter 6. As an insulator, a $10\,nm$ thin SiO_2 layer was used deposited by PECVD on top of the undoped layer structure without GaN cap (S2661). HEMTs and MOSHFETs were fabricated simultaneously to have the possibility to compare them in between. The thickness of the oxide layer was evaluated using the measured CV characteristics shown in figure 12.1 and utilizing equation:

$$\frac{1}{C_{MOS}} = \frac{1}{C_{MS}} + \frac{1}{C_{OX}} \tag{12.1}$$

where C_{MOS} is the measured capacitance of the planar MOS diode at zero bias, C_{MS} is the measured capacitance of the planar Schottky diode at zero bias on the same layer structure, and C_{OX} is the oxide capacitance required for evaluation of the oxide thickness. Then the thickness of the oxide is given by:

$$d_{OX} = \frac{\varepsilon_{OX}}{C_{MOS}} \cdot A - \frac{\varepsilon_{OX}}{C_{MS}} \cdot A \tag{12.2}$$

for the Schottky diode with the surface area A. The calculated thicknesses of the AlGaN

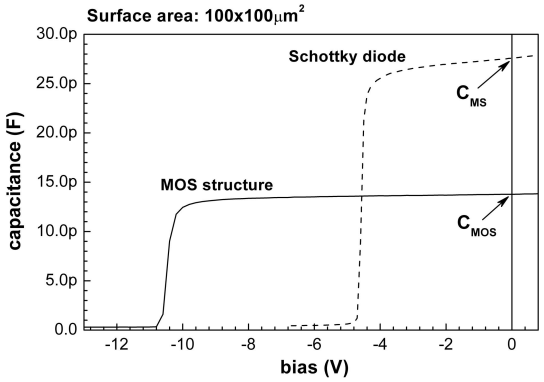


Figure 12.1: Comparison of CV characteristics measured on MOS structure and Schottky diode using the same layer structure.

buffer layer and the SiO_2 layer are $29.54\,nm$ and $11.62\,nm$, respectively, using relative permittivities of $\varepsilon_{AlGaN} = 9.2$ and $\varepsilon_{OX} = 3.9$ [103, 104]. This is in a good agreement with nominal values of $30\,nm$ and $10\,nm$ given for AlGaN buffer and SiO_2 layer, respectively.

The output characteristics of MOSHFETs showed 30 % increase of drain saturation current in comparison to HEMT structures (see figure 12.2). This is due to the influence of the SiO_2 insulation layer as a surface passivation confirmed also by Hall effect measurements where the MOS–structures exhibit an increase of $1.3 \times 10^{12}\,\mathrm{cm}^{-2}$ for the 2DEG sheet carrier concentration in comparison to unpassivated structures. Due to the considerable decrease of the gate capacitance (shown by CV measurements) and slightly decreased extrinsic transconductance, an increase of the cut–off frequency f_T is expected resulting from equation 4.26. The g_m parameter would be expected to decrease in MOSHFET rapidly, however the increased sheet carrier concentration in the channel and increased I_d^{sat} pushed the extrinsic transconductance up.

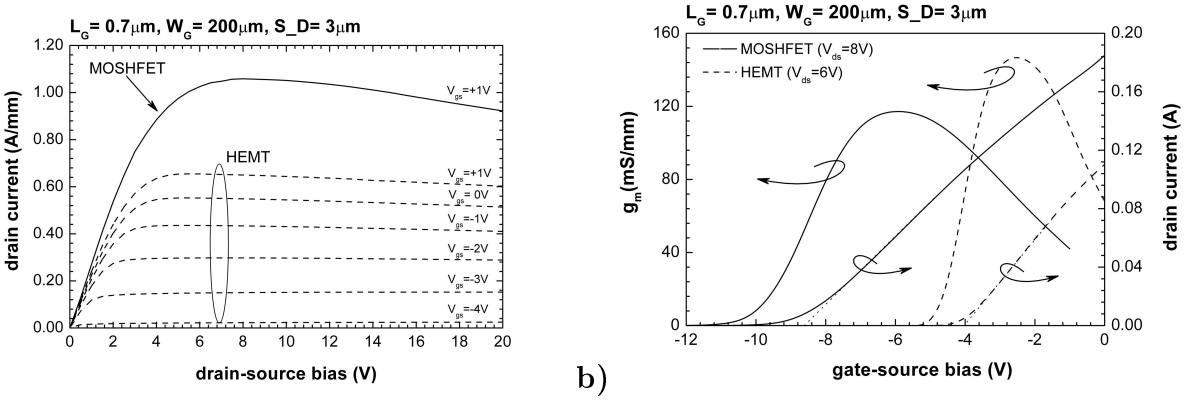


Figure 12.2: Comparison of output (a) and transfer (b) characteristics of MOSHFETs and HEMTs simultaneously fabricated on the same layer structure.

This was confirmed by rf measurements where the device with the gate length of $0.7\,\mu m$ and the source-drain distance of $3\,\mu m$ exhibits $f_T = 20.2\,GHz$ for MOSHFET in comparison to $15.2\,GHz$ for standard HEMT.

But the main reason for the MOSHFET development was a reduction of the gate leakage currents. Therefore, two terminal gate–source IV characteristics of MOSHFETs were measured and compared to the IV characteristics of HEMTs (shown in figure 12.3). Measurements showed a rapid decrease of the gate leakage current from 2.99×10^{-6} A/mm to 8.74×10^{-10} A/mm, measured at $V_{ds} = 0V$ and $V_{gs} = -5V$, using MOSHFET processing technology. Beside an increase of the drain saturation current and the current gain frequency this is the most important improvement of our device. But still, additional investigation is needed to improve the long–term reliability and to eliminate MOSHFETs degradation which involves the development of very thin high–κ insulators suitable for AlGaN/GaN heterostructures.

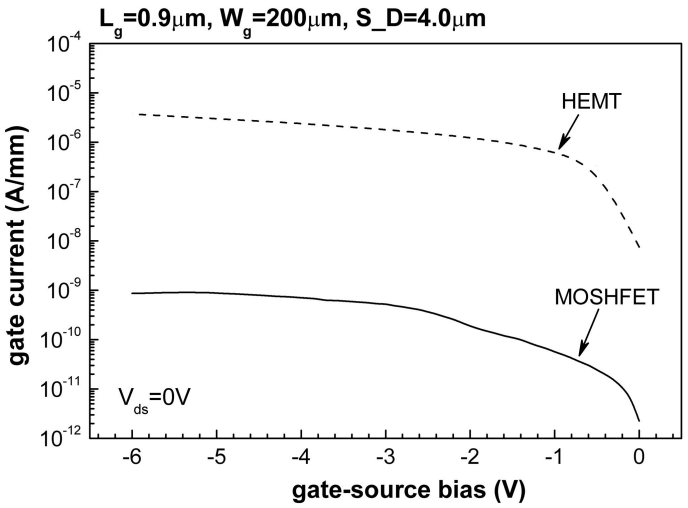


Figure 12.3: Two terminal gate–source IV characteristics of MOSHFET vs. HEMT.

Chapter 13

AlGaN/GaN HEMT "Made in Forschungszentrum Jülich"

An increasing interest in AlGaN/GaN heterostructures lead to an assembly of MOVPE grown GaN–based layer structures under leadership of Dr. H. Hardtdegen at our institute. During the last period, suitable AlGaN/GaN growth process was developed and improved. This resulted in the successful growth of GaN/AlGaN/GaN/Sapphire heterostructure [99, 100]. The grown layer structure consists of n.i.d. GaN buffer layer followed by a 30 nm thin n.i.d. $Al_{0.3}Ga_{0.7}N$ and covered by a 3 nm n.i.d. GaN cap. The sheet carrier concentration of $7.82 \times 10^{12}\,\mathrm{cm}^{-2}$ and the mobility of $1738\,\mathrm{cm}^2/\mathrm{Vs}$ were measured by room temperature using Van der Pauw patterns with area of $0.3 \times 0.3\,mm^2$. The sheet carrier concentration and mobility of $8.81 \times 10^{12}\,\mathrm{cm}^{-2}$ and $1753\,\mathrm{cm}^2/\mathrm{Vs}$, respectively, evaluated from CV and TLM measurements are in a good agreement with Hall effect measurements. The standard HEMT technology process described in appendix A was used for device fabrication. The ohmic contact resistance and the sheet resistance evaluated using TLM pattern yielded $5.89\,\Omega\,mm$ and $393\,\Omega/sq.$, respectively. All results showed very good homogeneity and planarity of the layer structure.

Output characteristics showed in figure 13.1 exhibit the saturation drain current of $0.77\,A/mm$, the extrinsic transconductance of $185\,mS/mm$, and the threshold voltage of $-4.5\,V$. These results are comparable with published results using AlGaN/GaN/Sapphire HEMTs where I_d^{sat} from $0.46\,A/mm$ to $0.95\,A/mm$ and g_m from $150\,mS/mm$ to $236\,mS/mm$ were published [10,61,62,101,102]. The gate leakage currents were measured to be $2.71 \times 10^{-5}\,mA/mm$ at $V_{gs} = -6\,V$ and $V_{ds} = 0\,V$, respectively. The dependence of the current gain frequency f_T and maximum frequency of oscillation f_{max} on the gate length of HEMTs is shown in figure 13.2. The device with the gate length of $L_g = 0.3\,\mu m$ showed a maximum cut–off frequency of $38.6\,GHz$.

These results show that we are able to produce GaN–based devices beginning with the

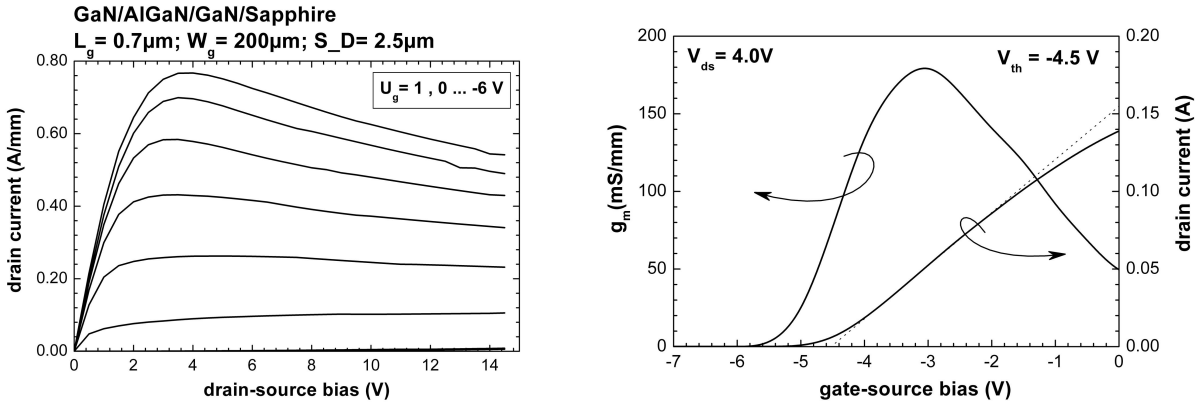


Figure 13.1: Output (a) and transfer (b) characteristics of HEMTs "Made in FZ-Juelich".

growth process, going on with the application of the device technology down to sub-micron dimensions, and ending with the device measurement and characterisation. Nowadays, the growing procedure of AlGaN/GaN heterostructures with alternative substrates is under development at our institute. HEMT and MOSHFET processing technology will be introduced using these structures with the aim to eliminate negative influences of the substrate mismatch.

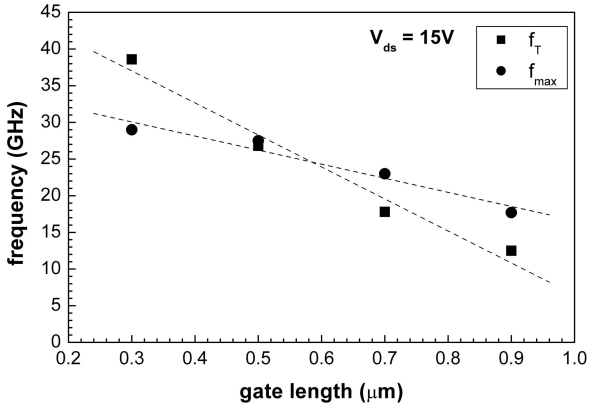


Figure 13.2: Current gain frequency and maximum frequency of oscillation dependency on the gate length.

Chapter 14

Conclusion

The III–Nitrides were intensively studied during the last few years due to its tunable band gap range from $0.7\,eV$ for InN to $6.2\,eV$ for AlN. In comparison to other systems III–Nitrides have a much smaller lattice constant and therefore are mechanically stable materials with high breakdown fields. Thanks to these properties are good candidates for possible applications in the field of high–temperature, –power and –frequency electronics.

Aim of this work was to investigate physical properties and technological parameters of AlGaN/GaN HEMTs on SiC substrate. By means of optimisation of the technology process and the geometry of devices the better static, small–signal, and large–signal properties should be reached. Characterisation of fabricated HEMTs required good knowledge of standard as well as novel measurement techniques adapted for AlGaN/GaN material system connected with the investigation of various effects, special for GaN–based heterostructures.

This work was divided into three parts. The first one contains an introduction followed by present status analysis and the definition of the main tasks to be accomplished. The second part covers the theory of gallium–nitrides, explains the formation of heterostructures using AlGaN/GaN, introduces the basic principles of high electron mobility transistors, followed by a discussion of special effects concerning the GaN–based material system. The final part consists of chapters 6 to 13 describing the technological processes and geometrical variations used for device fabrication, outlines the characterisation of fabricated HEMTs, and discusses the measured effects with respect to worldwide published data. This part is the most important part of the work. Finally, the work is closed with a conclusion.

The technological process developed in this work was derived from a HEMT fabrication process already established at our institute. After forming the mesa islands using Ar^+ sputtering the ohmic contacts were prepared by rapid-thermal annealing of Ti/Al/Ni/Au multilayer at $850\,°C$ for 30 s. The Ni/Au Schottky contacts were patterned by e-beam

lithography. Devices with a gate length of $0.3-0.9\,\mu m$ and a gate width of $50-300\,\mu m$ (two fingers) were prepared. Van der Pauw patterns with an active area of $0.3 \times 0.3\,mm^2$ were processed simultaneously with the HEMT devices. The standard process was improved within the bound of this work by additional processes containing MOSHFET processing, surface passivation, air bridge technology, and field plate processing. The mask layout called "Mega HEMT" was specially designed for the purposes of this work. Using this mask, HEMTs on undoped and doped layer structures were manufactured. Later, the new mask set with changed geometrical dimensions of HEMTs called "Power 2" was developed. This new layout enabled us to investigate the field plate technology resulting in higher output power of HEMTs.

The used layer structures were grown on SiC substrates using Metal Organic Vapour Phase Epitaxy (MOVPE) according to our specifications. Layer structures were divided into two main categories: non–intentionally doped (n.i.d. or undoped), and intentionally doped structures. The doping level of the doped structures was chosen to be $2 \times 10^{18}\,\mathrm{cm}^{-3}$ and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ using Si as N–type dopant. The layer structures were characterised using standard characterisation methods such as Hall effect, TLM, and CV measurements.

Improved properties of intentionally doped structures in comparison to undoped ones were observed using Hall effect measurements [118]. Increasing sheet carrier concentration in 2DEG of $\sim 7.0 \times 10^{12}\,\mathrm{cm}^{-2}$, $\sim 8.2 \times 10^{12}\,\mathrm{cm}^{-2}$, and $\sim 9.7 \times 10^{12}\,\mathrm{cm}^{-2}$ were measured for undoped, $2 \times 10^{18}\,\mathrm{cm}^{-3}$ doped, and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped samples, respectively. The mobility of electrons was determined to be $1930\,\mathrm{cm}^2/\mathrm{Vs}$, $1780\,\mathrm{cm}^2/\mathrm{Vs}$, and $1663\,\mathrm{cm}^2/\mathrm{Vs}$ for undoped, $2 \times 10^{18}\,\mathrm{cm}^{-3}$ doped, and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped samples, respectively. These results confirmed that layer structures were well grown with high mobility and high sheet carrier concentration in two–dimensional gas.

Static (dc) measurements on unpassivated devices exhibited improved properties of HEMTs fabricated on doped layer structure which is in agreement with Hall effect measurements [121]. Devices on undoped structure yielded values of $I_d^{sat} = 0.73\,A/mm$ and $g_m = 185\,mS/mm$. In comparison, $2 \times 10^{18}\,\mathrm{cm}^{-3}$ doped layer structures showed values of $I_d^{sat} = 1.06\,A/mm$ and $g_m = 214\,mS/mm$ and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped layer structures resulted in values of $I_d^{sat} = 1.12\,A/mm$ and $g_m = 207\,mS/mm$. On the other side, the doped structures exhibited lower breakdown voltage connected with higher gate leakage current.

The small–signal measurements showed advantageous behaviour of undoped layer structures. The HEMTs with the gate–length of $0.3\,\mu m$ ($W_g = 200\,\mu m$, $S\_D = 3\,\mu m$) fabricated on undoped layer structure exhibited a cut–off frequency of $42.6\,GHz$ in comparison to $35.8\,GHz$ and $30.8\,GHz$ measured on $2 \times 10^{18}\,\mathrm{cm}^{-3}$ doped and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped layer structures, respectively.

The current collapse phenomenon was investigated using gate lag measurements for undoped and doped samples. All unpassivated devices showed drain current collapse (or dc/rf dispersion) between 35 % and 23 % at 5 μs pulse width. The drain current in pulse mode was found to be dependent on the doping concentration of the barrier layer where with increased doping level the current collapse decreased. This collapsed behaviour was confirmed by output power measurements at 7 GHz where the output power of 2.95 W/mm, 4.45 W/mm, and 7.58 W/mm was measured on undoped, $2 \times 10^{18}\,\mathrm{cm}^{-3}$ doped, and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped layer structures, respectively. These values are far below the theoretically expected values of 12 W/mm calculated for AlGaN/GaN heterostructure.

Further improvement of static and large–signal properties was achieved using a 150 nm thick Si_3N_4 surface passivation layer. Hall effect measurements showed a higher sheet carrier concentration in the channel and a slightly lower decrease of electron mobility [118]. The increase of the product $n_s \times \mu_n$ in undoped layer structures was more pronounced (8.9 %) in comparison to doped layer structures (3.4 % for $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped structure). These results were in good agreement with the drain current increase and the shift of the threshold voltage to more negative values.

The positive influence on the surface states in between drain and source electrode using surface passivation resulted in a decrease of the current collapse at 5 μs pulse width to 14 % and 11 % for undoped and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped structure, respectively. An exact explanation of the phenomenon is not entirely clear until now but a widely accepted explanation is that natural donor–like surface states are the source of electrons collected in the 2DEG. Therefore, a change in surface states is mirrored into a change of the n_s in the 2DEG. Nevertheless, the non–collapsed samples suffered from high gate leakage currents. Developed MOSHFETs provided a suitable solution of this problem with better static and rf behaviour in comparison to HEMTs and four orders of magnitude lower gate leakage current in comparison to HEMTs [122]. However, further investigation is required for improved characterisation of MOSHFETs properties.

Improvement of the static and pulse behaviour resulted to remarkably improved output power. A 88 % increase of the output power for passivated undoped samples, and a 48 % increase for $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped samples was measured. This represents a maximum output power of $\sim 9\,W/mm$ measured on $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped sample. This value is fully comparable with worldwide published results.

Surface passivation was not the only investigated approach for improvements. A barrier to further output power increase is still the low breakdown voltage. Using the ATLAS simulation package the location of peak electric field in the under gate region was found and eliminated using field plate technology. A 31 % decrease of the electric field peak was

simulated and the breakdown voltage improvement in real HEMT was measured. This resulted in further output power increase with an excellent measured value of 12 W/mm in undoped and doped samples. This is an improvement of over 300 % for undoped and almost 60 % for $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped samples in comparison to unpassivated samples.

In spite of these remarkable results, current collapse was still present in measured samples. Detailed study of our technological process, specifically the gate contact processing and pre–deposition surface cleaning, were found to be crucial regarding the current collapse. An extended HCl treatment prior to metal deposition and adjusted metal deposition resulted to samples with negligible, if any, current collapse down to GHz frequency range (ns pulses) [121, 123]. The undoped samples exhibit a current collapse of under 8 % while the $5 \times 10^{18}\,\mathrm{cm}^{-3}$ doped sample have no current collapse at all at $50\,ns$ pulse width. Furthermore, a direct dependence of the gate leakage current on the current collapse was observed: With decreasing current collapse (better rf performances) the gate leakage current increased [125]. This can be attributed to the presence of electron traps within the GaN cap layer and/or to surface conduction mechanisms. A higher conductivity between gate and drain/source contacts reflects into a large carrier population within the cap layer, hence faster surface charge modulation (i.e. smaller dispersion at a given pulse width) is observed.

The long term reliability of the devices was also tested on non–collapsed samples. Negligible degradation below 3.9 % was measured after 12 hours off–state bias stress what was a one order of magnitude smaller degradation in comparison to data of recently published papers applying the same stress conditions [124].

Finally, the GaN–based research culminated in the fabrication of AlGaN/GaN HEMTs including MOVPE growth of undoped AlGaN/GaN heterostructure on sapphire substrate at our institute. The process consisted of the growth of layer structure, manufacturing of devices, and finally the electrical characterisation. Results showed fully comparable behaviour of these HEMTs with those worldwide published in literature.

Even though this work presents a major progress in GaN–based material system and processing there are still questions related especially to long term reliability (in months and years) which have to be answered. The reliability also seems to be the last barrier before industrial production of AlGaN/GaN HEMTs. By now, industrial companies announced wholesale production for the year 2006 what presents the AlGaN/GaN material system as a future candidate for research and industry.

Chapter 15

Zusammenfassung

Gruppe III-Nitride sind in der letzten Zeit besonders untersucht worden wegen ihres einstellbaren Bandabstandes von $0,7\,eV$ für InN bis $6,2\,eV$ für AlN. Im Vergleich zu anderen Systemen haben Gruppe III-Nitride einen deutlich kleineren Gitterabstand, und darum sind sie mechanisch stabiler und haben höhere Durchbruchfelder. Aus diesen Grund sind Gruppe III-Nitride geeignete Kandidaten für Hochtemperatur-, Leistungs-, und Frequenz-Anwendungen.

Das Ziel dieser Arbeit ist die Untersuchung von bauelementphysikalischen und prozesstechnologischen Parametern von AlGaN/GaN-„High Electron Mobility" Transistoren (HEMTs) auf SiC-Substraten. Durch eine Optimierung des Technologie Prozesses und der Geometrie der Bauelemente sollen damit das elektrische (dc), das Klein-Signal-Verhalten und die Groß-Signal Eigenschafen verbessert werden. Messung und Charakterisierung der Parameter der hergestellten Transistoren erfordern gute Kenntnisse von etablierten und von neuen, auf das AlGaN/GaN Materialsystem angepassten Messtechniken. Damit ist es möglich, unterschiedliche Effekte, die speziell bei GaN-basierte Heterostrukturen auftreten, zu untersuchen.

Die Arbeit besteht aus drei Hauptteilen. Der erster Teil umfasst die Einleitung, die Analyse des derzeitigen Status der Forschung und stellt die Ziele der Arbeit vor. Der zweite Teil beschreibt theoretisch Gallium-Nitrid (GaN), die Entstehung des Zweidimensionalen Gases (2DEG) in AlGaN/GaN Heterostrukturen und das Grundprinzip von „High Electron Mobility" Transistoren. Diskutiert werden auch Effekte, die speziell bei GaN-basierten Materialsystemen auftreten. Der letzter Teil stellt die Technologie Prozesse und die einzelnen Transistoren vor, beschreibt die Messungen und diskutiert die ermittelten Daten. Diese werden im Anschluss mit Daten aus der internationalen Fachliteratur verglichen. Eine Zusammenfassung beschließt die Arbeit.

Die Prozesstechnologie, die im Rahmen dieser Arbeit entwickelt wurde, ist von der in unserem Institut etablierten Standard-HEMT-Prozesstechnologie abgeleitet. Die Mesa–

Inseln wurden mittels Ar^+ Sputtern definiert, gefolgt von der Einlegierung der Ohmschen Kontakten aus Ti/Al/Ni/Au bei $850\,°C$ für 30 s. Schottky Kontakte (Ni/Au) wurden mit Hilfe der Elektronenstrahl Lithographie definiert. Auf diese Weise wurden Gate–Längen von $0,3 - 0,9\,\mu m$ und Gate–Breiten von $50 - 300\,\mu m$ (zwei Finger) hergestellt. Van der Pauw Muster mit einer aktiven Fläche von $0,3 \times 0,3\,mm^2$ wurden zusammen mit den HEMT-Bauelementen produziert. Diese Standard-Prozesstechnologie wurde später um die MOSHFET[1] Prozesstechnologie, Oberflächen-Passivierungsprozesse, Luftbrücken-Technologie und „Field plate"-Prozesstechnologie erweitert. Um die Prozesstechnologie durchzuführen, war eine Maskensatz für optische und Elektronenstrahl Lithographie notwendig. Der Maskensatz „MegaHEMT" ist speziell für diese Arbeit entwickelt und für die Herstellung von nicht-dotierten und dotierten HEMT genutzt worden. Später wurde ein neuer, optimierter Maskensatz „Power 2" entwickelt, mit dessen Hilfe die HEMT-Eigenschaften verbessert und die Realisierung der „Field plate"-Technologie ermöglicht wurde.

Wie schon erwähnt wurde, für die Herstellung und die Experimente wurden nicht-dotierte und dotierte Strukturen benutzt. Die von uns definierten AlGaN/GaN Schichten wurden auf SiC-Substraten durch die ATMI Inc. mittels MOVPE[2] Epitaxie epitaktisch deponiert. Hierbei ist eine Dotierung mit Silizium als n-Dotierungstyp von $2 \times 10^{18}\,\mathrm{cm}^{-3}$ und $5 \times 10^{18}\,\mathrm{cm}^{-3}$ gewählt worden.

Die epitaktisch deponierten Schichtstrukturen wurden mit Hall Messungen, TLM-[3] und CV-[4]Messungen charakterisiert. Die Hall-Effekt-Meßergebnisse wiesen auf verbesserte Eigenschaften der dotierten Strukturen im Vergleich zu nicht-dotierten hin [118]. Die gemessene Elektronendichte im 2DEG war $\sim 7,0 \times 10^{12}\,\mathrm{cm}^{-2}$ für nicht-dotierte, $\sim 8,2 \times 10^{12}\,\mathrm{cm}^{-2}$ für $2 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierte, und $\sim 9,7 \times 10^{12}\,\mathrm{cm}^{-2}$ für $5 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierte Proben. Die Beweglichkeit der Elektronen im Kanal war $1930\,\mathrm{cm}^2/\mathrm{Vs}$ für nicht-dotierte, $1780\,\mathrm{cm}^2/\mathrm{Vs}$ für $2 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierte, und $1663\,\mathrm{cm}^2/\mathrm{Vs}$ für $5 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierte Strukturen. Eine hohe Elektronendichte und hohe Beweglichkeit im Kanal bestätigten die gute Qualität der Proben.

Gleichstrom-Untersuchungen der nicht-passivierten Transistoren haben bestätigt, dass dotierte Proben im Vergleich zu nicht-dotierten bessere Eigenschaften aufweisen [121]. Bei nicht-dotierten Strukturen wurde $I_d^{sat} = 0,73\,A/mm$ und $g_m = 185\,mS/mm$ gemessen, im Vergleich zu $2 \times 10^{18}\,\mathrm{cm}^{-3}$ und $5 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierten Strukturen, wo bessere Gleichstromwerte $I_d^{sat} = 1,06\,A/mm$, $g_m = 214\,mS/mm$ und $I_d^{sat} = 1,12\,A/mm$, $g_m = 207\,mS/mm$ gemessen wurden. Gleichwohl wurden niedrigere Durchbruchspannungen und höhere „Gate Leakage" Ströme für dotierte Strukturen beobachtet, was die Eigen-

[1]HEMT mit MOS gate
[2]Metal Organic Vapour Phase Epitaxy
[3]Transmission Line Model
[4]Kapazität–Spannung

schaften verschlechtert.

Bei den Kleinsignal Messungen konnten höhere „cut-off" Frequenzen für nicht-dotierte Proben nachgewiesen werden. $42,6\,GHz$ wurde für nicht-dotierte Proben mit $L_g = 0.3\,\mu m$, $W_g = 200\,\mu m$, $S\_D = 3\,\mu m$ gemessen, im Vergleich dazu wurden $35,8\,GHz$ und $30,8\,GHz$ für $2 \times 10^{18}\,\mathrm{cm}^{-3}$ und $5 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierte Proben gemessen.

Das unerwünschte Kollabieren des Drain Stromes, typisch für AlGaN/GaN-Heterostrukturen, wurde mit der „Gate lag" Messmethode untersucht. Nicht passivierte Proben zeigten einen Kollaps zwischen 35 % und 23 % für $5\,\mu s$ lange Pulse. Es konnte gezeigt werden, dass der Kollaps abhängig von der Dotierung der Barrierenschicht ist. Mit erhöhter Dotierung der Barrierenschicht sinkt der Kollaps, was auch durch Leistungs-Messungen bestätigt werden konnte. Die Leistung bei 7 GHz war $2,95\,W/mm$ für nicht-dotierte, $4,45\,W/mm$ für $2 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierte, und $7,58\,W/mm$ für $5 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierte Strukturen. Dennoch lagen die gemessenen Leistungen tief unter dem theoretisch zu erwartete den Wert von $12\,W/mm$.

Eine weitere Verbesserung der Gleichstrom- und Leistungs-Kennzahlen konnte durch die Passivierung der Oberflächen mit einer $150\,nm$ dicken Si_3N_4 Passivierungsschichte erreicht werden. Die Hall-Effekt-Messungen wiesen eine höhere Konzentration von Ladungsträgern im Kanal und nur eine kleine Senkung der Elektronen-Mobilität nach [118]. Das Produkt $n_s \times \mu_n$ war deutlich um 8,9 % in nicht-dotierte Strukturen verbessert, im Vergleich zur Verbesserung um 3,4 % in $5 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierten Strukturen. Diese Ergebnisse stimmen mit der Vergrößerung des Drain-Stromes und der Verschiebung den Schwellenspannung überein.

Die Oberflächenpassivierung beeinflusst die Oberflächenzuständen und führt zur Senkung des Stromkollapses bei $5\,\mu s$ Pulsen auf 14 % für nicht-dotierte und auf 11 % für $5 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierte Strukturen. Eine exakte Erklärung des Phänomens ist derzeit auch in einschlägiger Literatur nicht zu finden. Wir denken, dass Änderungen der Oberflächenzustände sich in Änderungen der Konzentrationsdichte von Elektronen im Kanal wiederspiegeln. Dies stimmt mit der breit akzeptierten Erklärung überein, dass Donator-Zustände an der Oberfläche die Quelle von Kanalelektronen sind. Auf der anderen Seite weisen Bauelemente mit kleinem Stromkollaps höhere Gate-Ströme auf. Die untersuchten MOSHFET-Strukturen wiesen bessere Gleichstrom- und Hochfrequenz-Eigenschaften auf im Vergleich zu normalen HEMTs. Der Gate-Strom von MOSHFET-Strukturen war vier Größenordnungen kleiner als der von normalen HEMTs [122]. Aber die vollständige Charakterisierung von MOSHFETs ist noch nicht beendet und erfordert weitere Untersuchungen.

Eine Verbesserung von Gleichstrom- und Puls-Eigenschaften führt zur Verbesserung der Leistungseigenschaften um 88 % in der nicht-dotierten Proben und um 48 % in der

$5 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierten Proben. In absoluten Zahlen bedeutet dies $9\,W/mm$ für die $5 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierten Proben. Den Wert ist vergleichbar mit weltweit veröffentlichten Leistungen.

Die Oberflächenpassivierung ist nicht der einzige Ansatz, der untersucht wurde. Ein weiteres Hindernis für eine verbesserte Ausgangs-Leistung ist die immer noch relativ kleine Durchbruchspannung. Mit dem ATLAS-Simulationsprogramm konnten die Maxima des elektrischen Feldes, die den Durchbruch verursachen, in der Region unter dem Gate lokalisiert und mit der „field plate"-Prozesstechnologie eliminiert werden. Die Maxima des elektrischen Feldes sind laut Simulation um 31 % gesunken und damit konnte die Durchbruchspannung erhöht werden. In der folge sind die exzellenten Werte von 12 W/mm Ausgang–Leistungen bei nicht-dotierten und dotierten Proben erreicht worden. Das bedeutet eine Verbesserung von 300 % bei nicht-dotierten und fast 60 % bei dotierten Proben im Vergleich zu nicht passivierten Bauelementen.

Trotz der vorgestellten, positiven Ergebnisse zur Minimierung des Stromkollaps, war er immer noch in den Strukturen vorhanden. Unsere detaillierten Untersuchungen zielten daher auf eine weitere Verbesserung des Technologieprozesses, speziell der Aufdampfung des Gate-Kontaktes und der Reinigungsprozedur der Oberfläche vor der Aufdampfung. Eine längere Behandlung in Salzsäure kurz vor der Aufdampfung des Metalls führt zu Transistoren mit vernachlässigbar kleinem oder gar keinem Strom-Kollaps bis in den GHz Frequenzbereichs (ns Pulses) [121, 123]. Bei undotierten Proben wurde ein Kollaps von 8 % nachgewiesen, und bei $5 \times 10^{18}\,\mathrm{cm}^{-3}$ dotierten Proben konnte kein Kollaps bei $50\,ns$ Pulsbreite beobachtet werden. Darüber hinaus wurde folgende Abhängigkeit des Strom-Kollapses von den Gate Strömen beobachtet: mit sinkendem Kollaps (bessere rf Eigenschaften) sind die Gate-Ströme gestiegen [125]. Das kann durch Defekte in der „GaN Cap" Schicht und/oder durch Leitungsmechanismen an der Oberfläche verursacht worden sein. Eine höhere Leitfähigkeit zwischen Gate- und Source/Drain-Elektroden führt zu einer schnelleren Besetzung der Zustände innerhalb der „Cap"-Schichten und damit zu einer schnelleren Ladungsmodulation (kleinere „Dispersion").

Die Zuverlässigkeit der hergestellten Bauelemente über längere Zeiträume wurde an Proben ohne Kollaps getestet. Die Strukturen wurden für 12 Stunden bei „Pinch-off" Bedingungen unter Spannung gesetzt. Nach dem Zyklus konnten für die HEMTs nur eine geringe Degradierung unter 3,9 % nachgewiesen werden. Das ist eine um eine Größenordnung kleinere Degradierung als bei veröffentlichten Daten mit den selben Stress Bedingungen [124].

Das ganze auf AlGaN/GaN/Saphire Heterostrukturen basierte Bauelement kann an unserem Institut hergestellt werden. Der Prozess umfasst das AlGaN/GaN Wachstum,

die Herstellung von HEMTs und die elektrischen Charakterisierung. Die gemessenen Ergebnisse sind in jeder Beziehung mit veröffentlichten Daten vergleichbar, was auf die gute Qualität des gesamten Prozesses hindeutet.

Diese Arbeit präsentiert wichtige neue Entwicklungsschritte in GaN-basierten Prozessen und Technologien für die HEMT-Herstellung. Jedoch gibt es noch offene Fragen, speziell zur Langfrist–Zuverlässigkeit, die beantwortet werden müssen. Die Langfrist–Zuverlässigkeit scheint die letzte Barriere zu sein für die industrielle Produktion von AlGaN/GaN HEMTs. Jetzt schon kündigt die Industrie die Produktion für 2006 an, damit bleibt das AlGaN/GaN Material System ein guter Kandidat für zukünftige Produktionstechniken.

Appendix A

Standard HEMT Processing

A.1 Mesa etching

1. Sample Drying (Plate, Temperature: 180°C)
2. Photo-resist Deposition
   (a) Resist: AZ5214, 4000rev./min
   (b) Harden: 90°C, Time: 5min
3. Removing of the Side Resist
   (a) Exposure
   (b) Development: $AZ400K(1) : H_2O(4)$
4. Mesa definition
   (a) Exposure
   (b) Development: $AZ400K(1) : H_2O(4)$
   (c) Resist hardening
5. Etching: Ar^+ (Bias: 500V, Current density: 0.5mA/mm^2)

A.2 Ohmic Contacts Fabrication

1. Sample Cleaning (Acetone+Propanol, Oxygen Plasma, HF solution, HCl solution, NH_3
2. Photo-resist Deposition
3. Removing of the Side Resist
4. Ohmic Contacts Definition

   (a) Exposure
   (b) Development: $AZ400K(1) : H_2O(4)$

5. HCl Dip
6. Metallisation: Ti(35nm) / Al(200nm) / Ni (40nm) / Au (100nm)
7. Lift-off
8. Thermal Annealing (Temperature: 900°C, Time: 30sec, Atmosphere: N_2)

A.3 Schottky Contact Fabrication

1. Resist Deposition
   (a) Resist: PMMA 600
   (b) Resist: PMMA 200
   (c) Resist: PMMA 600
2. E-Beam Photo-Lithography
3. E-Beam development
4. HCl Dip
5. Metallisation: Ni(25nm) / Au(100nm)
6. Lift-off

A.4 Pads Fabrication

1. Photo-resist Deposition
2. Removing of the Side Resist
3. Pads Definition
4. Metallisation: Ti(50nm) / Au(300nm)
5. Lift-off

Appendix B

MOSHFET Processing

B.1 Mesa etching

B.2 Ohmic Contacts Fabrication

B.3 Pads Fabrication

B.4 Deposition of isolation layer

1. PECVD deposition of the SiO_2 (10 nm, 300°)
2. Photo-resist Deposition
3. Removing of the Side Resist
4. Definition of the Windows to be Open
5. RIE in O_2 plasma
6. Removing of the resist (Acetone & Propanol)

B.5 Schottky Contact Fabrication

Appendix C

Air Bridge Technology

1. First Photo-resist Deposition (AZ4562, 5000rev./min) and Harden (90°C)
2. Removing of the Side Resist
3. First Resist Layer Pattern (Mask Air-Bridge 1):
   (a) Exposure
   (b) Development: $AZ400K(1) : H_2O(4)$
4. Harden: 120°C
5. Metallisation: Au(100nm) / Ti(20nm)
6. Second Photo-resist Deposition (AZ4562)
7. Removing of the Side Resist
8. Second Resist Layer Pattern (Mask Air-Bridge 2)
9. Harden: 110°C
10. Removing of the Ti Layer: $HF(1) : H_2O(2)$
11. Galvanisation (I=25mA, T=60°C, t=25min)
12. Removing of the Second Resist (AZ100 remover)
13. Removing of the 100nm thin Au layer
14. Removing of the First Resist (AZ100 remover)

Appendix D

ATLAS Simulation Programmes

D.1 AlGaN/GaN HEMT simulation

```
go atlas
#
# AlGaN/GaN HEMT
#
# SECTION 1:  Mesh input
#
mesh
x.mesh loc=0.0 spac=0.5
x.mesh loc=4.0 spac=0.01
x.mesh loc=5.5 spac=0.01
x.mesh loc=10 spac=0.5
#
y.mesh loc=0.0 spac=0.05
y.mesh loc=0.030 spac=0.0001
y.mesh loc=0.1 spac=0.05
#
# SECTION 2:  Structure Specification
#
region num=1 material=GaN y.min=0.03
region num=2 material=AlGaN y.max=0.03 x.comp=0.3
#
elec num=1 name=source x.min=0.0 x.max=3 y.min=0.0 y.max=0.0
elec num=2 name=gate x.min=4 x.max=4.5 y.min=0.0 y.max=0.0
```

```
elec num=3 name=drain x.min=7 x.max=10 y.min=0.0 y.max=0.0
#
doping region=1 uniform n.type conc=1.0e15
doping region=2 uniform n.type conc=1.0e16
#
interface charge=-1.00e13 s.s y.min=0.030
#
# SECTION 3:  Material Models
#
material material=AlGaN align=0.8
material material=GaN align=0.8
#
material material=AlGaN affinity=3.82 eg300=3.96 permittivity=9.5 mun=600 mup=10
nc300=2.07e18 nv300=1.16e19
material material=GaN eg300=3.40 permittivity=9.5 mun=900 mup=10 nc300=1.07e18
nv300=1.16e19 vsat=2e7
#
models fixed.fermi calc.fermi
#
contact name=gate workfunction=4.5
#
# SECTION 4:  Initial solution
#
solve init
#
# SECTION 3:  Bias gate, drain
#
method gummel newton block
output e.field val.band con.band
solve vgate=-2.8 vdrain=50.0
save outf=hemt-2deg.str
tonyplot hemt-2deg.str
#
quit
```

D.2 Simulation of AlGaN/GaN HEMT with 50 nm Si_3N_4 passivation layer

```
go atlas
#
# Si3N4 passivated AlGaN/GaN HEMT
#
# SECTION 1:  Mesh input
#
mesh
x.mesh loc=0.0 spac=0.5
x.mesh loc=4.0 spac=0.01
x.mesh loc=5.5 spac=0.01
x.mesh loc=10 spac=0.5
#
y.mesh loc=-0.05 spac=0.05
y.mesh loc=0.0 spac=0.05
y.mesh loc=0.030 spac=0.0001
y.mesh loc=0.1 spac=0.05
#
# SECTION 2:  Structure Specification
#
region num=1 material=GaN y.min=0.03
region num=2 material=AlGaN y.max=0.03 x.comp=0.3
region num=3 material=Si3N4 y.min=-0.05 y.max=0.0
#
elec num=1 name=source x.min=0.0 x.max=3 y.min=-0.05 y.max=0.0
elec num=2 name=gate x.min=4 x.max=4.5 y.min=0.0 y.max=0.0
elec num=3 name=drain x.min=7 x.max=10 y.min=-0.05 y.max=0.0
#
doping region=1 uniform n.type conc=1.0e15
doping region=2 uniform n.type conc=1.0e16
#
interface charge=-1.00e13 s.s y.min=0.030
#
# SECTION 3:  Material Models
#
```

```
material material=AlGaN align=0.8
material material=GaN align=0.8
#
material material=AlGaN affinity=3.82 eg300=3.96 permittivity=9.5 mun=600 mup=10
nc300=2.07e18 nv300=1.16e19
material material=GaN eg300=3.40 permittivity=9.5 mun=900 mup=10 nc300=1.07e18
nv300=1.16e19 vsat=2e7
#
models fixed.fermi calc.fermi
#
contact name=gate workfunction=4.5
#
# SECTION 4:  Initial solution
#
solve init
#
# SECTION 3:  Bias gate, drain
#
method gummel newton block
output e.field val.band con.band
solve vgate=-2.8 vdrain=50.0
save outf=hemt-2deg-SiN50.str
tonyplot hemt-2deg-SiN50.str
#
quit
```

D.3 Simulation of AlGaN/GaN HEMT with Field–Plate Technology

```
go atlas
#
# AlGaN/GaN HEMT, Field-Plate
#
# SECTION 1:  Mesh input
#
mesh
x.mesh loc=0.0 spac=0.5
x.mesh loc=4.0 spac=0.01
x.mesh loc=5.5 spac=0.01
x.mesh loc=10 spac=0.5
#
y.mesh loc=-0.05 spac=0.05
y.mesh loc=0.0 spac=0.05
y.mesh loc=0.030 spac=0.0001
y.mesh loc=0.1 spac=0.05
#
# SECTION 2:  Structure Specification
#
region num=1 material=GaN y.min=0.03
region num=2 material=AlGaN y.max=0.03 x.comp=0.3
region num=3 material=Si3N4 y.min=-0.05 y.max=0.0
#
elec num=1 name=source x.min=0.0 x.max=3 y.min=-0.05 y.max=0.0
elec num=2 name=gate1 x.min=4 x.max=4.5 y.min=0.0 y.max=0.0
elec num=3 name=gate2 x.min=4 x.max=5.0 y.min=-0.05 y.max=-0.05
elec num=4 name=drain x.min=7 x.max=10 y.min=-0.05 y.max=0.0
#
doping region=1 uniform n.type conc=1.0e15
doping region=2 uniform n.type conc=1.0e16
#
interface charge=-1.00e13 s.s y.min=0.030
#
contact name=gate2 common=gate1
```

```
#
# SECTION 3:  Material Models
#
material material=AlGaN align=0.8
material material=GaN align=0.8
#
material material=AlGaN affinity=3.82 eg300=3.96 permittivity=9.5 mun=600 mup=10
nc300=2.07e18 nv300=1.16e19
material material=GaN eg300=3.40 permittivity=9.5 mun=900 mup=10 nc300=1.07e18
nv300=1.16e19 vsat=2e7
#
models fixed.fermi calc.fermi
#
contact name=gate workfunction=4.5
#
# SECTION 4:  Initial solution
#
solve init
#
# SECTION 3:  Bias gate, drain
#
method gummel newton block
output e.field val.band con.band
solve vgate=-2.8 vdrain=50.0
save outf=hemt-2deg-FP50.str
tonyplot hemt-2deg-FP50.str
#
quit
```

Appendix E

List of Symbols

Symbol	Description	Unit
a	Lattice constance (x-axis)	Å
c	Lattice constance (z-axis)	Å
C	Capacitance	F
c_0	Capacitance per unit area	F/m^2
E	Energy	eV
E_F	Fermi energy level	eV
E_C	Bottom of conduction band	eV
E_V	Top of valence band	eV
E_g	Energy band gap	eV
E_{vac}	Vacuum energy level	eV
L	Thickness of quantum well	Å
Λ	Correlation length	Å
T	Absolute temperature	K
f	Occupancy number	
m_e	Effective electron mass	m_0
m_h	Effective hole mass	m_0
μ_n	Electron mobility	cm^2/Vs
μ_p	Hole mobility	cm^2/Vs
μ_0	Low-field electron mobility	cm^2/Vs
n	Density of free electrons	m^{-3}
n_s	Sheet density of electrons	m^{-2}
N_D	Ionised donor density	m^{-3}
N_{dis}	Dislocation density	m^{-2}

Symbol	Description	Unit
L_g	Gate length of HEMT	μm
L_{gs}	Gate-source distance	μm
L_{gd}	Gate-drain distance	μm
W_g	Gate width of HEMT	μm
S_D	Source-drain distance of HEMT	μm
V	Voltage	V
V_{gs}	Gate-source voltage	V
V_{ds}	Drain-source voltage	V
V_{th}	Threshold voltage	V
V_{bi}	Built-in voltage	V
V_p	Pinch-off voltage	V
V_{br}	Breakdown voltage	V
V_{knee}	Knee voltage	V
V_H	Hall voltage	V
V_{dc}	dc voltage	V
v_{ac}	ac voltage	V
q	Magnitude of electronic charge	C
ε	Permittivity ($\varepsilon_0 \cdot \varepsilon_r$)	F/m
ε_0	Permittivity in vacuum	F/m
ε_r	Relative permittivity	
d_i	Thickness of wide band gap semiconductor	μm
Δd	Effective thickness of 2DEG	μm
g_{ch}	Extrinsic conductivity of 2DEG	S
g_{chi}	Intrinsic conductivity of 2DEG	S
ρ_c	Specific resistance	$\Omega \cdot mm$
R	Resistance	Ω
R_s	Source resistance	Ω
R_d	Drain resistance	Ω
R_g	Gate resistance	Ω
R_c	Contact resistance	$\Omega \cdot mm$
R_{ds}	Drain-source resistance	Ω
R_{sheet}	Sheet resistivity	$\Omega \cdot square$
R_{th}	Thermal resistance	Ω
R_{sub}	Substrate resistance	Ω

Symbol	Description	Unit
L_s	Drain inductance	nH
L_d	Source inductance	nH
L_g	Gate inductance	nH
$C_{g,pad}$	Gate pad capacitance	pF
$C_{d,pad}$	Drain pad capacitance	pF
C_{gs}	Gate-source intrinsic capacitance	pF
C_{gd}	Gate-drain intrinsic capacitance	pF
C_{2DEG}	2DEG capacitance	pF
ν	Carrier velocity	cm/s
ν_{sat}	Saturation carrier velocity	cm/s
E	Electric field	V/cm
E_y	Hall field	V/cm
E_c	Critical electric field	V/cm
I	Current	A
I_d	Drain-source current	A
I_d^{sat}	Saturation drain-source current	A
J	Current density	A/m^2
f_T	Current gain cut off frequency	Hz
f_{max}	maximum frequency of oscillations	Hz
g_m	Transconductance	mS
ω_T	Current gain radial frequency	Hz
P_{outlin}^{dc}	linear rf output power	W
P_{outsat}^{dc}	saturation output power	W
P_{out}	rf output power	W
$P.A.E.$	Power added Efficiency	%
$\mathbf{B}$	Magnetic field	T
F_y	Lorenz-force	N
L_T	Effective length of ohmic contact	μm
Q	Electric charge	C
Q_s	Semiconductor charge	C
A	Cross section	m^2
w	Depletion depth	μm

Appendix F

Physical Constants

Quantity	**Symbol/Unit**	**Value**
Angstrom unit	Å	1Å$= 10^{-1}nm = 10^{-10}m$
Avogadro constant	N_{avo}	$6.02204 \times 10^{23} mole^{-1}$
Boltzmann constant	k	$1.38066 \times 10^{-23} J/K$
Elementary charge	q	$1.60218 \times 10^{-19} C$
Electron rest mass	m_0	$0.91095 \times 10^{-30} kg$
Electron volt	eV	$1eV = 1.60218 \times 10^{-19} J$
Permeability in vacuum	μ_0	$1.25663 \times 10^{-8} H/cm$ $(4\pi \times 10^{-9})$
Permittivity in vacuum	ε_0	$8.85418 \times 10^{-14} F/cm$ $(1/\mu_0 c^2)$
Planck constant	h	$6.62617 \times 10^{-34} Js$
Reduced Planck constant	$\hbar$	$1.05458 \times 10^{-34} Js$ $(h/2\pi)$
Speed of light in vacuum	c	$2.99792 \times 10^{10} cm/s$
Standard atmosphere		$1.01325 \times 10^{5} Pa$
Thermal voltage at 300K	kT/q	$0.0259V$
Wavelength of 1eV quantum	λ	$1.23977 \mu m$

List of Figures

List of Tables

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SKILLS

- Experienced in processing technology (Ar sputter, RIE etching, Photolithography, etc.) and work in clean rooms.
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